



PowerPC Tools

Development Tools for PowerPC Microprocessors

Fifth Edition
September, 1996

© International Business Machines Corporation 1996
Printed in the United States of America
9-96
All Rights Reserved

This notice applies to the PowerPC Tools catalog, dated September 1996. The following paragraphs do not apply in any country or state where such provisions are inconsistent with local law: The information in this publication is subject to change without notice. The publication is provided "AS IS." International Business Machines Corporation (hereafter "IBM") does not make any warranty of any kind, either expressed or implied, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Information in this document is provided solely to enable system and software implementers to use PowerPC microprocessors. Unless specifically set forth herein, there are no express or implied patent, copyright or any other intellectual property rights or licenses granted hereunder to design or fabricate PowerPC integrated circuits or integrated circuits based on the information in this document. IBM does not warrant that the contents of this publication, whether individually or as one or more groups, will meet your requirements or that the publication is error-free. This publication could include technical inaccuracies or typographical errors. Changes may be made to the information herein; these changes may be incorporated in new editions of the publication.

Notice to U.S. Government Users—Documentation Related to Restricted Rights—Use, duplication or disclosure is subject to restrictions set forth in GSA ADP Schedule Contract with IBM Corporation.

The following terms are registered trademarks of the IBM Corporation: 400, AIX, AIX/6000, AIXwindows, IBM and the IBM logo, OS/2, PowerPC 601, PowerPC 603, PowerPC 604, POWERserver, RISC System/6000.

The following terms are trademarks of the IBM Corporation: 400Series, 401 Core, 401GF, 403GA, 403GB, 403GC, C Set ++, IBM High C/C++, IBM Microelectronics, OS Open, POWER Architecture, POWER2 Architecture, PowerPC and the PowerPC logo, PowerPC Architecture, PowerPC 602, PowerPC 603e, PowerPC 604e, PowerPC 620, POWERstation, POWER Team, PowerBench, ProFrame, RISCWatch, RISCTrace, RS/6000.

*PowerPC microprocessors are hereinafter sometimes referred as "PowerPC".
All other trademarks and registered trademarks are the property of their respective companies.*

Requests for copies of this publication should be made to the office shown below. IBM may use, disclose or distribute whatever information you supply in any way it believes appropriate without incurring any obligation to you.

*IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531
Tel: (800) POWERPC
Tel: (800) 769-3772*

*The IBM home page can be found at: <http://www.ibm.com>
The IBM Microelectronics Division home page can be found at: <http://www.chips.ibm.com>
Fax Service 415-855-4121
Fax Document #20018*

*Published for IBM by:
Warthman Associates
240 Hamilton Avenue
Palo Alto, California 94301
(415) 322-4555
(415) 322-4555 FAX
writers@warthman.com*

Preface and Quick-Find Matrix

This catalog contains a series of two-page entries describing tools for PowerPC software and hardware developers. For an overview of these tools, try one of the following:

- *Quick-Find Matrix* (starting on the next page)—It cross-references tool types to vendors, and shows the first page number on which one or more such cross-referenced tools are described.
- *Contents* (immediately after the Quick-Find Matrix)—It lists each tool by vendor and broad category, showing the page number of each tool.
- *Glossary* (immediately preceding the Index)—It defines the terms used in the Quick-Find Matrix column headings, the catalog's major section names, and the product types used to categorize individual products.
- *Index* (at the back of the book)—It lists each tool, vendor, and tool type, showing its page number.

IBM has gathered this information directly from the tool vendors. If you would like more information about a tool, please contact the vendor directly. The contact information for each vendor is given at the end of each two-page entry. For tools sold by IBM, a complete listing of sales offices is available on the Web at <http://www.chips.ibm.com/orders/index.html>.

If you are a tool developer and have a product specifically tailored to development for PowerPC processor-based computers, IBM invites you to request inclusion of your product, free of charge, in a future edition of this book. To arrange this, please contact IBM at:

Desktop-System Tools

IBM Desktop Solutions
6xxtools@austin.ibm.com

Embedded-System Tools

IBM Embedded Solutions
(919) 254-1810
empower400@vnet.ibm.com

The contributed entries for the catalog were edited and produced by:

Embedded-System Tools: Thomas Collopy, IBM Microelectronics.

Desktop-System Tools: Ricardo Gariazzo, IBM Microelectronics.

General Editors and Production: Alan Sommerer and Forrest Warthman, Warthman Associates.

Preface and Quick-Find Matrix

Company	Analyzers	Boards	Chips	Code, Libraries, Models, Test Suites	Compilers, Interpreters, Translators	Debuggers, Disassemblers	Emulators, Simulators	Information Resources	Multimedia Tools	Operating Systems, User Interfaces	Real-Time Tools	Services, Support, Training	Utilities
Absoft Corporation				42	38*	38*							38*
Accelerated Technology Inc.						180				180	180		180
Adobe Systems, Inc.					232		232						
Apogee				142*	142*	142*							
Apple				146	146	146						320	146
Applied Microsystems						72	72						72
Applied Testing and Technology				234									
Arnewsh, Inc.		298											
BBN Systems and Technologies, Inc.	76					74*							
Case Tools, Inc.						78							
CETIA/THOMSON-CSF		300											
Chorus Systems				216		216	216			216	216		216
Chronology	254												
Cogent Computer Systems, Inc.		302											
Corelis	258	304		256			80*						
Creative Electronic Systems (CSE)		306*											
Cygnus Support				148	148	148							148
Diab Data				82	82								82
dli Digital Logic Instruments	260*												
Embedded Performance/Biomation	264												
Embedded System Products, Inc.						182				182	182		
ENEA DATA										184	184		
Eureka Technology							266						
FirePower Systems, Inc.		310	310										
FirmWorks				158				324*				322	158
Fortner Research LLC						44							
Gordian												328	
Grammar Engine, Inc.	84						84*						
Green Hills Software	96			88*	88*	98*				218			88*

* An asterisk indicates the first of multiple products offered by a company, in that product type.

Preface and Quick-Find Matrix

Company	Analyzers	Boards	Chips	Code, Libraries, Models, Test Suites	Compilers, Interpreters, Translators	Debuggers, Disassemblers	Emulators, Simulators	Information Resources	Multimedia Tools	Operating Systems, User Interfaces	Real-Time Tools	Services, Support, Training	Utilities
	Page Numbers												
Harris Computer Systems Corporation	48			186		46*				46*	46*		186
Hewlett-Packard	268*					268*					272		
Huntsville Microsystems, Inc.						102	102						
IBM Corporation	108	312*	2*	108	56*	54*	106	330*		162*	108	332	54*
Idealogy												336	
Industrial Programming										190	190		
Integrated Systems, Inc.						192				192	192		192
Jasik Design						60							
JMI Software Systems						194				194	194		194
JYACC, Inc.													172
KADAK Products Ltd.										196	196		196
Lauterbach Datentechnik	110*	112				110*	110*						
Logic Modeling/Synopsis				282			282						
Lucent Technologies	114				114	114							
Lynx										198	198		
MetaWare					116	116					116		116
Metrowerks Inc.				62	62	62							62*
Micro Digital				200						200	200		
MicroAPL Ltd.					118								
Microsoft				120	120	120							120
Microtec				202	122	122*				202*	124*		122
Microware Systems Corporation					126*	126*			236	204	126*		204*
Motorola Inc.				66*	66*	66*		174					66*
Object Technology, Inc.				130	130	130							130
OC Systems, Inc.					154	154							154
PIPELINE					238*								
PLX Technology			28										
Power Micro Research												338	
PowerTV, Inc.									206	206	206		206

* An asterisk indicates the first of multiple products offered by a company, in that product type.

Preface and Quick-Find Matrix

<i>Company</i>	<i>Analyzers</i>	<i>Boards</i>	<i>Chips</i>	<i>Code, Libraries, Models, Test Suites</i>	<i>Compilers, Interpreters, Translators</i>	<i>Debuggers, Disassemblers</i>	<i>Emulators, Simulators</i>	<i>Information Resources</i>	<i>Multimedia Tools</i>	<i>Operating Systems, User Interfaces</i>	<i>Real-Time Tools</i>	<i>Services, Support, Training</i>	<i>Utilities</i>
Precise Software Tech										208	208		208
Quad Design Technology				284									
Questra												340	
Rational Software Corporation				132	132	132	132						132
Sand Microelectronics							286					342	
Softex				176									
Software Development Systems, Inc.				226	226	134*	134				134		226
STEP Engineering	136					136	136						
Synopsis/Logic Modeling				282			282						
Tadpole Technology												344	
TECSI										210	210		
Tektronix	288*					288*							
Thermalloy, Inc.													294
Thomson Software Products				68*	68*	68*					138		68*
Total Impact		316											
U S Software	212			244*		212				212	212*		244
V3 Corporation			30										
VLSI			32*										
w-Cube Software Corporation										248			248
Warthman Associates								346				346	
Wind River Systems, Inc.						228				228	228		228
Xionics Document Technologies Inc.			250	250	250								

* An asterisk indicates the first of multiple products offered by a company, in that product type.

Contents

Preface and Quick-Find Matrix	iii
Contents	vii
Processors and Support Chips	1
IBM Microelectronics	2
PowerPC 401 CPU Core	2
PowerPC 401GF Embedded Controller	4
PowerPC 403GA Embedded Controller	6
PowerPC 403GB Embedded Controller	8
PowerPC 403GC Embedded Controller	10
IBM27-82660 PCI/Memory Chip Set	12
PowerPC 601 RISC Microprocessor	14
PowerPC 602 RISC Microprocessor	16
PowerPC 603 RISC Microprocessor	18
PowerPC 603e RISC Microprocessor	20
PowerPC 604 RISC Microprocessor	22
PowerPC 604e RISC Microprocessor	24
PowerPC 620 RISC Microprocessor	26
PLX Technology	28
PCI 9060ES	28
V3 Corporation	30
V292PBC	30
VLSI Technology	32
TollGate/VAS 96021	32
GoldenGate II Core Logic	34
Software Generation and Debug Tools (Native)	37
Absoft Corporation	38
Absoft C/C++ for AIX, Windows NT and Power Macintosh	38
Absoft FORTRAN 77 for AIX, Windows NT and Power Macintosh	40
IMSL Math and Stat Libraries v3.0	42
Fortner Research LLC	44
LS FORTRAN and LS Object Pascal	44

Software Generation and Debug Tools (Native) (continued)

Harris Computer Systems Corporation.....	46
NightView Source-Level Debugger	46
NightTrace Analyzer.....	48
NightSim Application Scheduler	50
NightProbe Data Monitoring Tool	52
IBM Corporation.....	54
IBM POWERbench and AIX SDE WorkBench/6000 Version 2	54
XL Fortran for AIX Version 3	56
AIX XL Pascal Compiler/6000 Version 2.....	58
Jasik Designs	60
The Debugger V2 and MacNosy	60
Metrowerks	62
Metrowerks CodeWarrior	62
CodeManager	64
Motorola, Inc.	66
Motorola UNIX SDK PowerPC Edition	66
Thomson Software Products.....	68
Ada Development Environment for AIX Operating System	68
 Software Generation and Debug Tools (Cross).....	 71
Applied Microsystems Corporation	72
NetROM.....	72
BBN Systems and Technologies, Inc.	74
TotalView.....	74
TimeScan	76
CaseTools, Inc.	78
UDB.....	78
Corelis	80
PowerEM Emulators	80
Diab Data, Inc.	82
Diab Data Compiler Suites (D-CC, D-C++, D-F77)	82
Grammar Engine Inc.	84
FlashICE	84
PromICE	86

Software Generation and Debug Tools (Cross) (continued)

Green Hills Software, Inc.....	88
Green Hills Ada.....	88
Green Hills C/C++	90
Green Hills FORTRAN.....	92
Green Hills PASCAL	94
MULTI Execution Profiler	96
MULTI Debug Servers for VxWorks, pSOS+ and Custom RTOSs	98
MULTI Source Level Debugger	100
Huntsville Microsystems, Inc.	102
HMI-200 Series In-Circuit Emulator	102
IBM Corporation.....	104
IBM High C/C++	104
PowerPC Virtual Simulator	106
RISCWatch.....	108
Lauterbach Datentechnik.....	110
TRACE32 BDM/ROM Debugger.....	110
TRACE32-ICE	112
Lucent Technologies Bell Laboratories.....	114
FlashPort	114
MetaWare Incorporated	116
High C/C++ PowerPC Embedded Development Toolset.....	116
MicroAPL Ltd.	118
PortAsm.....	118
Microsoft Corporation	120
Microsoft Visual C++	120
Microtec	122
Optimizing C/C++ Compilers	122
XRAY Debugger	124
Microware Systems Corporation.....	126
Ultra C/Ultra C++	126
Motorola, Inc.....	128
Motorola C/C++ SDK PowerPC Edition for MacOS	128
Object Technology Inc.....	130
ENVY/ <i>Embedded</i> Smalltalk.....	130
Rational Software Corporation	132
Rational Ada, C, C++	132

Software Generation and Debug Tools (Cross) (continued)

Software Development Systems, Inc.....	134
SingleStep	134
STEP Engineering.....	136
STEP Exceed-400	136
Thomson Software Products.....	138
The AdaWorld Cross-Development Environment.....	138

Software Generation and Debug Tools (Native and Cross) 141

Apogee Software, Inc.	142
Apogee-C and Apogee-C++.....	142
Apogee-FORTRAN 77	144
Apple Computer, Inc.....	146
Essentials•Tools•Objects	146
Cygnus Support	148
Cygnus Developer's Kit for PowerPC Architectures.....	148
IBM Corporation.....	150
C for AIX Version 3.....	150
C Set ++ for AIX Version 3.....	152
OC Systems, Inc.....	154
PowerAda and PowerAda/LynxOS	154

Operating Systems and Development Environments (Desktop) 157

FirmWorks.....	158
Power Firmware System ROM Code.....	158
IBM Corporation.....	160
Configuration Management Version Control (CMVC)	160
AIX Version 3 for RISC System/6000	162
AIXwindows Environment/6000	164
AIX Version 4.2	166
AIX Version 4 Licensing	168
Windows NT	170
JYACC, Inc.	172
JAM.....	172
Motorola, Inc.....	174
Motorola Hardware Abstraction Layer (HAL) Kit for Windows NT	174

Operating Systems and Development Environments (Desktop) (continued)

Softex.....	176
PowerPC Boot Firmware	176
Real-Time Operating Systems	179
Accelerated Technology, Inc.	180
Nucleus PLUS	180
Embedded System Products, Inc.	182
RTXC.....	182
Enea OSE Systems.....	184
OSE Delta Real-Time Operating System	184
Harris Computer Systems Corporation	186
PowerUX Operating System	186
IBM Corporation.....	188
OS Open.....	188
Industrial Programming, Inc.	190
MTOS-UX/PPC	190
Integrated Systems, Inc.	192
pSOSystem	192
JMI Software Systems, Inc.	194
C EXECUTIVE and PSX.....	194
KADAK Products Ltd.	196
AMX PPC32 Real-Time Multitasking Kernel.....	196
Lynx Real-Time Systems.....	198
LynxOS.....	198
Micro Digital Inc.	200
smxPPC	200
Microtec	202
VRTX/OS	202
Microware Systems Corporation.....	204
OS-9.....	204
PowerTV, Inc.....	206
PowerTV.....	206
Precise Software Technologies Inc.	208
Precise Real-Time Executives.....	208
TECSI S.A.....	210
RealTime Craft.....	210

Real-Time Operating Systems (continued)	
U S Software	212
SuperTask!	212
Cross-Development Environments (Embedded)	215
Chorus Systems	216
CHORUS/ClassiX	216
Green Hills Software, Inc.	218
MULTI Development Environment	218
Microtec	220
SPECTRA	220
XRAY MasterWorks	222
Microware Systems Corporation	224
FasTrak	224
Software Development Systems, Inc.	226
SDS C and C++ Compilers	226
Wind River Systems, Inc.	228
Tornado	228
Application-Specific Tools	231
Adobe Systems, Inc.	232
Printer Controller Reference Port	232
Applied Testing and Technology, Inc.	234
PowerPC Embedded ABI Test Suite (PEATS)	234
Microware Systems Corporation	236
DAVID Audio/Visual Interactive Decoder	236
PIPELINE	238
PowerPage Level 2	238
PowerPage PCL 5C	240
PowerPage PCL 5e	242
U S Software	244
USNET	244
GOFAST Floating-Point Libraries	246
w-CUBE Software Corporation	248
FDS-Mate	248
Xionics Document Technologies, Inc.	250
Modular Multifunction Peripheral Controller Design	250

Hardware Development Tools	253
Chronology Corporation.....	254
TimingDesigner.....	254
Corelis.....	256
SCANTEST.....	256
UI-MPC601 Universal Interface.....	258
dli-digital logic instruments gmbh.....	260
dli Personal Line Logic Analyzer Family.....	260
dli Professional Line High-Performance Logic Analyzer Family.....	262
Embedded Performance/Biomation.....	264
CLAS 4000 Logic Analyzer.....	264
Eureka Technology, Inc.	266
Synthesizable and Simulation Models for PowerPC Bus Interface.....	266
Hewlett-Packard Company.....	268
HP 16500 Series Modular Logic Analysis System.....	268
HP 16505A Prototype Analyzer.....	270
HP E2449B Inverse Assembler.....	272
HP E2455A Preprocessor Interface for the PowerPC 603 and 603e Microprocessors.....	274
HP E2468A Preprocessor for PowerPC 403GA and 403GC Embedded Controllers.....	276
HP E2465A Preprocessor Interface.....	278
HP E3494A and HP E3477A Processor Probes.....	280
Logic Modeling.....	282
SmartModel Library and Hardware Modeling Systems.....	282
Quad Design Technology.....	284
Signal Integrity Analysis Tools for High-Speed Designs.....	284
Sand Microelectronics, Inc.....	286
PowerPC 601 VHDL Model.....	286
Tektronix, Inc.	288
3000 Series Logic Analyzers.....	288
TLA500, DAS/NT and DAS/XP.....	290
TLS216.....	292
Thermalloy, Inc.	294
Thermal Management Solutions.....	294
Boards	297
Arnewsh, Inc.	298
SBC603.....	298

Boards (continued)	
CETIA, Inc./Thomson-CSF	300
PowerEngine VMTR2x and CVME60x	300
Cogent Computer Systems, Inc.	302
CMA Universal Development Platform	302
Corelis Inc.	304
SBC-403	304
Creative Electronic Systems SA	306
RTPC 8067 Development Platform and RIO2 Line of Target Platforms	306
PPCM 8403 Custom Oriented Processor Board	308
FirePower Systems, Inc.	310
Powerized Systems	310
IBM Microelectronics	312
PowerPC 403GA Evaluation Board Kit	312
PowerPC Platform Long Trail Reference Design	314
Total Impact	316
Total Power NuBus, Total Power PCI, and Total Freedom	316
Services and Documentation	319
Apple Computer, Inc.	320
Introduction to RISC and PowerPC	320
FirmWorks	322
Open Firmware System ROM and Device Driver Consulting	322
Writing FCode Programs for PCI	324
Open Firmware Command Reference	326
Gordian	328
Design and Prototype Development Services	328
IBM Corporation	330
PowerPC Reference Platform Specification	330
PowerPC Educational Courses	332
PowerPC Microprocessor User's Manuals	334
Idealogy, Inc.	336
Hardware Design Services	336
Power Micro Research	338
Power Micro Research	338

Services and Documentation (continued)	
Questra Consulting.....	340
PowerPC Design and Development Services.....	340
Sand Microelectronics, Inc.....	342
ASIC and System Board Design Services.....	342
Tadpole Technology.....	344
PowerPC Design Service.....	344
Warthman Associates.....	346
Documentation Services.....	346
Various Vendors.....	348
PowerPC Information Resources.....	348
Glossary	351
Sales Offices	355
Index	357

Processors and Support Chips

PowerPC 401™ CPU Core

Embedded Microprocessor

IBM Microelectronics

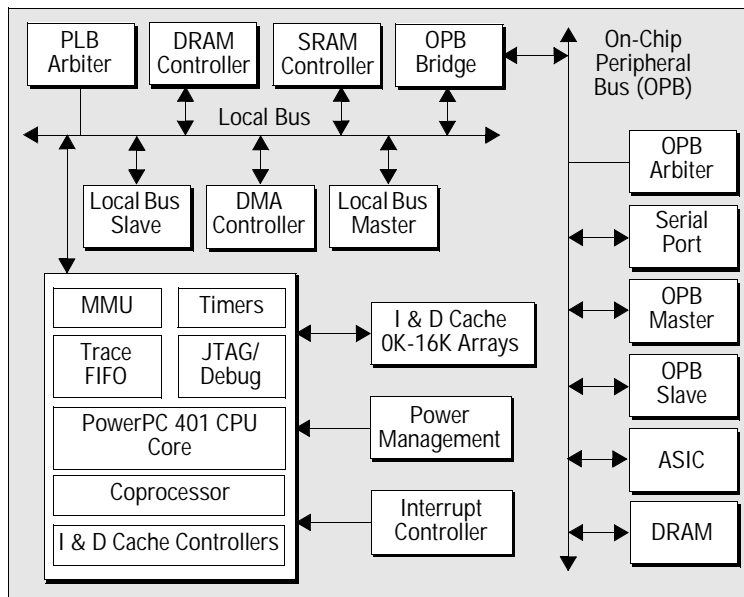
At the center of all PowerPC 401 solutions is our PowerPC 401 CPU Core, a 32-bit RISC microprocessor in IBM's Core+ ASIC program. This core is a high-performance, low-cost, low-power engine that provides the same high-speed pipelined operations inherent in all PowerPC™ chips. The 401 Core is well-positioned to meet the demands of applications in communications and consumer markets.

The PowerPC 401 CPU Core is embedded in a 401xx Core that also contains the functional elements required by your product specifications. These elements can include an MMU, cache controllers, coprocessor, timers and debug logic. If needed, one of multiple I and D cache array sizes will be included in your choice. The functional elements you choose are tightly coupled to the 4.5 mm² 401 Core.

The 401 Core implements the flexible and powerful PowerPC Architecture™. PowerPC products provide performance scalability from low-cost embedded controllers to high-end microprocessors, and the benefit of code portability and reusability.

The 401 Core is a member of the PowerPC 400Series, which is supported by the PowerPC Embedded Tools™ Program. In this program, IBM and over 40 third-party vendors offer a full range of development tools for embedded applications, including compilers, debuggers, real-time operating systems and logic analyzers.

Models are available for use on Synopsys VHDL System Simulator® (VSS), Cadence Verilog® and Leapfrog® and Mentor Graphics simulation platforms.



Processors and Support Chips

Features

- Compatible with PowerPC User Instruction Set Architecture.
- 176 K Dhrystones/Sec @ 100 MHz.
- Power Dissipation (Estimated)
 - Typical: 33.0 mW @ 25 MHz (2.7V).
 - Wait: 3.0 mW @ 25 MHz (2.7V).
 - Sleep: 0.01 mW @ 25 MHz (2.7V).
- 4.5 mm² in 0.5 μ m CMOS process, (0.39 μ m L_{eff}), three levels of metal.
- 32-bit x 32 general-purpose registers.
- Hardware multiply and divide.
- Up to 100 MHz.
- Non-blocking flush operations.
- Support for 0 K–16 K byte arrays.
- Separate I and D controllers.
- *Virtual Mode MMU*
 - Variable page sizes (1 KB-16 MB).
 - 64-entry fully-associative TLB.
- *Real Mode MMU*
 - Programmable cacheability.
 - Programmable copy-back/write-thru.
 - True little-endian operation.
- *Timers*
 - Support for external timer clock.
 - 64-bit time-base.
 - Programmable interval timer.
 - Fixed interval timer.
 - Watchdog timer.

Options

- *Coprocessor*
 - Select extended functionality such as floating point, fast multiply, etc.
- *JTAG/Debug*
 - IEEE 1149.1 port for in-circuit debug.
- *Trace FIFO*
 - Enables real-time non-invasive trace.
 - Exclusive traceback capability.
- *Cache Controllers*
 - Fill-first, data forwarding.

Integrating the 401xx Core

The 401xx Core has a processor local bus (PLB) that provides an interface to high performance peripherals, and an on-chip peripheral bus (OPB) that connects to lower-performance peripherals.

Availability

- Available now.

Contact

United States and Canada

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531
Tel: (800) PowerPC
Fax: (800) POWERfax

IBM homepage:
<http://www.ibm.com>

IBM Microelectronics homepage:
<http://www.chips.ibm.com>

Fax Service: (415) 855-4121

Japan

IBM
800, Ichimiyake
Yasu-cho, Yasu-gun
Shiga-ken, Japan 520-23
Tel: (81) 775-87-4745
Fax: (81) 775-87-4735

Europe

IBM
La Pompignane BP 1021
34006 Montpellier, France
Tel: (33) 6713-5757 (French)
Tel: (33) 6713-5756 (Italian)
Fax: (33) 6713-5750*
*from Paris add 16

IBM
Informations Systeme GmbH
Laatzener Str. 1
30539 Hannover, Germany
Tel: (49) 511-516-3444 (English)
Tel: (49) 511-516-3555 (German)
Fax: (49) 511-516-3888

PowerPC 401GF™ Embedded Controller

Embedded Microprocessor

IBM Microelectronics

The PowerPC 401GF Embedded Controller is designed around the 32-bit RISC PowerPC 401 Core for development in communications, consumer and printer markets. It supports the PowerPC User Instruction Set Architecture, making it the new price and performance leader in IBM's extended family of scalable and portable embedded processors.

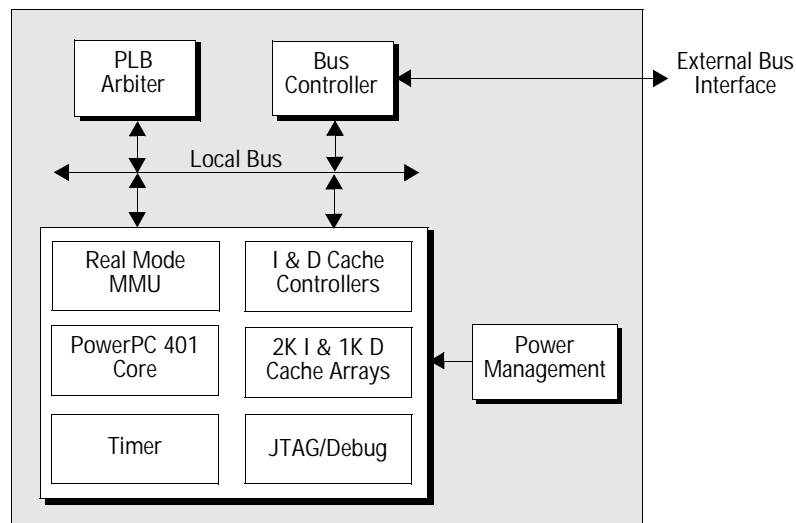
The 401GF maintains high-level PowerPC performance with a three-stage execution pipeline, combined with barrel rotator, operand forwarding and branch prediction logic. The 401GF I/O bus interface enables the best performance from the CPU while allowing you to design peripherals and memory control logic.

If low power consumption is important in your application, consider having the 401GF powered by an operating voltage ranging between 3.3 volts down to 2.5 volts. With IBM's unique power management logic, active power consumption is 50 mW at 25 MHz and 2.5 V. Sleep-mode power is as low as 0.015 mW.

Over 40 third-party vendors are in IBM's PowerPC Embedded Tools™ Program for support of PowerPC development. This program offers a full range of embedded development tools, including compilers, debuggers, real-time operating systems, emulators, logic analyzers, and evaluation boards.

Features

- *401 Core*
 - Compatible with PowerPC User Instruction Set Architecture.
 - 32-bit x 32 general purpose registers.
 - Hardware multiply and divide.
 - Unaligned load/store.
- *Timers*
 - 64-bit time-base.
 - Programmable interval timer.
 - Fixed interval timer.
 - Watchdog timer.



Processors and Support Chips

- *Bus Controller*
 - Multiplexed address/data bus.
 - Programmable read/write burst.
 - Target word first capability.
 - Bus clock out.
 - Support for 8-, 16- and 32- bit devices.
 - External bus master support.
 - JTAG port for Test/Debug (IEEE 1149.1).
- *Real Mode MMU*
 - Programmable cacheability.
 - Programmable copy-back/write-thru.
 - True Little-Endian operation.
- *Cache Controllers*
 - Separate I and D cache controllers.
 - Critical data forwarding.
 - Fill first handling of cache misses.
 - Non-blocking flush operations.
 - Store queue.
 - 2K I and 1K D cache arrays.
 - Array Built In Self Test (ABIST).
- *Power Management*
 - Custom circuitry to minimize power.
 - Hardware-based dynamic clocking.
 - On-chip oscillator.
 - Software-controlled sleep modes.

Specifications

- *Technology*—0.5 μ m CMOS, three levels of metal.
- *Core Size*—4.5 mm².
- *Frequency (CPU:I/O)*—1:1, 2:1, 3:1, 4:1.
- *Performance*
 - 176K Dhrystones/s (100 DMIPS)@100 MHz.
 - 132K Dhrystones/s (75 DMIPS)@75 MHz.
 - 88K Dhrystones/s (50 DMIPS)@50 MHz.
 - 44K Dhrystones/s (25 DMIPS)@25 MHz.
- *Voltage Requirements*
 - 2.5V \pm 0.1V (supports 3.3V I/Os) @ 25 MHz.
 - 3.3V \pm 5% (supports 5 I/Os) @ 50/75/100 MHz.
- *Power Dissipation (Est., 25 MHz @ 2.5V)*
 - Typical: 50.0 mW.
 - Doze: 15.0 mW.
 - Nap: 7.0 mW.
 - Sleep: 0.015 mW.
- *Max Case Temp Range*— -40° C to 120° C.
- *Packaging*—80-pin TFP, 63 Signal I/Os.

Availability

- Available now.

Contact

United States and Canada

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531
Tel: (800) PowerPC
Fax: (800) POWERfax

IBM homepage:
<http://www.ibm.com>

IBM Microelectronics homepage:
<http://www.chips.ibm.com>

Fax Service: (415) 855-4121

Japan

IBM
800, Ichimiya-ke,
Yasu-cho, Yasu-gun
Shiga-ken, Japan 520-23
Tel: (81) 775-87-4745
Fax: (81) 775-87-4735

Europe

IBM
La Pompidu BP 1021
34006 Montpellier, France
Tel: (33) 6713-5757 (French)
Tel: (33) 6713-5756 (Italian)
Fax: (33) 6713-5750*
*from Paris add 16

IBM
Informations Systeme GmbH
Laatzener Str. 1
30539 Hannover, Germany
Tel: (49) 511-516-3444 (English)
Tel: (49) 511-516-3555 (German)
Fax: (49) 511-516-3888

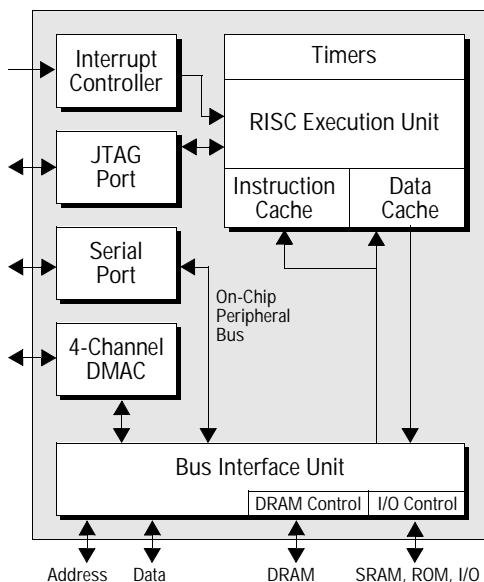
PowerPC 403GA™ Embedded Controller

Embedded Microprocessor

IBM Microelectronics

The PowerPC 403GA 32-bit RISC Embedded Controller combines high performance and functional integration with low power consumption. On-chip caches and integrated device control functions reduce system chip count and design complexity, while improving system throughput.

The 403GA embedded controller executes programs at sustained speeds approaching one instruction per cycle. The RISC processor core is tightly coupled to the internal 2KB instruction and 1KB data caches, reducing overhead for data transfers to and from main storage. Instruction queue logic manages branch prediction, branch folding, and instruction prefetching to minimize pipeline stalls. The 403GA embedded controller implements the PowerPC Architecture™ in IBM's advanced 0.5 μm CMOS technology.



The 403GA embedded controller provides low-power 3.3V operation, with built-in stand-by mode and dynamic power management, in a low-cost 160-pin plastic quad flat pack (PQFP).

Bus Interface

- Direct-connect peripheral / ROM and DRAM interfaces.
- Support for 8-, 16-, and 32-bit devices.
- Addressing for 512 MB of main storage.
- External bus master support using the internal DRAM controller.
- IEEE 1149.1 (JTAG) interface, test and debug support.

Serial Port

- RS-232 serial communications.
- Programmable to 1.5 Mb/s.
- Four independent DMA channels.
- Buffered, fly-by, memory-to-memory, and burst modes.
- Programmable for 8-, 16-, and 32-bit transfers.
- Data chaining.

Interrupt Controller

- Low latency interrupt handling (three cycles typical, 37 cycles worst case including cache miss effects).
- Six external interrupt inputs (five regular, one critical).
- Dual-level interrupt structure for robust debug.

Instruction Fetch, Branch and Dispatch Unit

- Four instruction prefetch queue.
- Branch folding and static branch prediction.
- Dispatches up to two instructions per cycle.

Processors and Support Chips

Power Management Capability

- Static low-power design.
- Dynamic power management and stand-by mode.
- Support for connections to 3.3V and 5V peripherals.

Memory Protection

- Device protection.
- Address protection.

Timers

- 56-bit time base.
- 32-bit programmable interval timer.
- Fixed interval timer.
- Watchdog timer for system error recovery.

Instruction and Address Caches

- Separate 2KB instruction and 1KB data caches.
- Two-way set-associative.
- Fetch-thru instruction cache.
- Write-back data cache.

Specifications

Technology	0.5 μ m CMOS process, 3-layer metal
Transistors	~585,000
Temperature	0° C to 85° C
Frequency	25 MHz and 33 MHz
Signal I/O	126
Power Supply	3.3V \pm 5% (support for 5V I/Os)
Performance	72K Dhrystones/s @ 33 MHz
Performance/Power	155 MIPS/Watt (Dhrystone 2.1)
Power Dissipation	200 mW at 25 MHz
Packaging	Plastic quad flat pack (160 pins)

Availability

- 25 MHz and 33 MHz versions are available now.

Contact

United States and Canada

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531
Tel: (800) PowerPC
Fax: (800) POWERfax

IBM homepage:
<http://www.ibm.com>

IBM Microelectronics homepage:
<http://www.chips.ibm.com>

Fax Service: (415) 855-4121

Japan

IBM
800, Ichimiyake
Yasu-cho, Yasu-gun
Shiga-ken, Japan 520-23
Tel: (81) 775-87-4745
Fax: (81) 775-87-4735

Europe

IBM
La Pompignane BP 1021
34006 Montpellier, France
Tel: (33) 6713-5757 (French)
Tel: (33) 6713-5756 (Italian)
Fax: (33) 6713-5750*
*from Paris add 16

IBM
Informations Systeme GmbH
Laatzener Str. 1
30539 Hannover, Germany
Tel: (49) 511-516-3444 (English)
Tel: (49) 511-516-3555 (German)
Fax: (49) 511-516-3888

PowerPC 403GB™ Embedded Controller

Embedded Microprocessor

IBM Microelectronics

The PowerPC 403GB Embedded Controller combines the high performance of a 32-bit RISC processor with ultra-low power consumption. The 403GB implements the performance-leading PowerPC Architecture™ in IBM's advanced 0.5 μm CMOS technology. The architecture's scalability and flexibility enable the chip to be binary compatible with all IBM PowerPC microprocessors and embedded controllers. The superscalar 403GB executes programs at sustained speeds approaching one instruction per cycle.

The 403GB is a recent addition to the IBM 400 Series of embedded controllers that provides on-chip caches and peripheral integration to reduce total system power, chip count, and design complexity, and improve system reliability and throughput. Power consumption is minimized by a specially designed low-power circuit library, a static core design, 3.3V operation, and dynamic clocking. The 28MHz 403GB is packaged in a low-cost, industry standard 128-pin thin quad flat pack (TQFP), enabling the chip to be ideally suited for price-sensitive 32-bit applications.

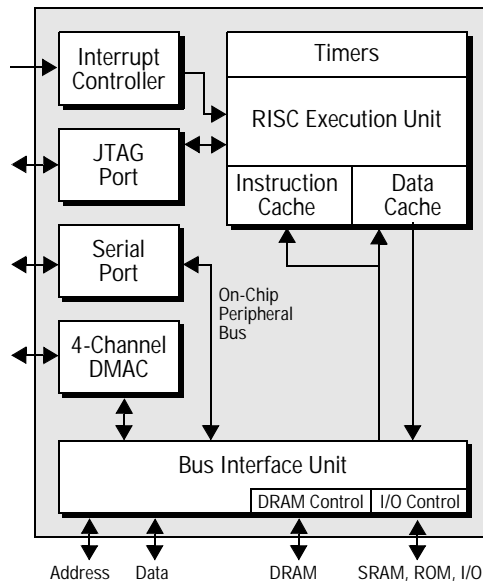
The PowerPC 403GB is supported by IBM and over 40 third-party vendors in the PowerPC Embedded Tools™ program, offering a full range of embedded development tools, including compilers, debuggers, real-time operating systems, emulators, logic analyzers, and evaluation boards.

DMA Controller

- Two independent DMA channels.
- Buffered, fly-by, memory-to-memory modes.
- Programmable for 8-, 16-, and 32-bit transfers.
- Data chaining.

Bus Interface

- Direct-connect peripheral/SRAM/ROM and DRAM interfaces.
- Support for 8-, 16-, and 32-bit devices
- Addressing for 192 MB of main storage.
- External bus master support using the internal DRAM controller.
- IEEE 1149.1 (JTAG) interface, test and debug support.



Interrupt Controller

- Low latency interrupt handling (three cycles typical).
- Six external interrupt inputs (five regular, one critical).
- Dual-level interrupt structure for robust debug.

Processors and Support Chips

Power Management Capability

- Static low-power design.
- Dynamic power management and stand-by mode.
- Support for connections to 3.3V and 5V peripherals.

Instruction Fetch, Branch and Dispatch Unit

- Four instruction prefetch queue.
- Branch folding and static branch prediction.
- Dispatches up to two instructions per cycle.

Memory Protection

- Device protection.
- Address protection.
- Instruction and data caches.
- Separate 2KB instruction and 1KB data caches.
- Two-way set-associative.
- Fetch-thru instruction cache
- Write-back data cache.

Timers

- 56-bit time base.
- 32-bit programmable interval timer.

- Fixed interval timer.
- Watchdog timer for system error recovery.

Specifications

Technology	0.5 μ m CMOS process, 3-layer metal
Transistors	~500,000
Temperature	0° C to 85° C
Frequency	28 MHz
Signal I/O	104
Power Supply	3.3V \pm 5% (support for 5V I/Os)
Performance	61K Dhrystones/s @ 28 MHz
Performance/Power	167 MIPS/Watt (Dhrystone 2.1)
Power Dissipation	210 mW at 28 MHz
Packaging	Plastic quad flat pack (128 pins)

Availability

- Available now.

Contact

United States and Canada

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531
Tel: (800) PowerPC
Fax: (800) POWERfax

IBM homepage:
<http://www.ibm.com>

IBM Microelectronics homepage:
<http://www.chips.ibm.com>

Fax Service: (415) 855-4121

Japan

IBM
800, Ichimiyake
Yasu-cho, Yasu-gun
Shiga-ken, Japan 520-23
Tel: (81) 775-87-4745
Fax: (81) 775-87-4735

Europe

IBM
La Pompidu BP 1021
34006 Montpellier, France
Tel: (33) 6713-5757 (French)
Tel: (33) 6713-5756 (Italian)
Fax: (33) 6713-5750*
*from Paris add 16

IBM
Informations Systeme GmbH
Laatzener Str. 1
30539 Hannover, Germany
Tel: (49) 511-516-3444 (English)
Tel: (49) 511-516-3555 (German)
Fax: (49) 511-516-3888

PowerPC 403GC™ Embedded Controller

Embedded Microprocessor

IBM Microelectronics

The 32-bit RISC PowerPC 403GC is a recent addition to the IBM PowerPC 400Series of Embedded Controllers, which provide on-chip caches and peripheral integration to reduce total system power, chip count, and design complexity, and improve system reliability and throughput. Power consumption on the 403GC is minimized by a custom-designed low-power circuit library, a static core design, 3.3V operation, and dynamic clocking. The chip is binary compatible with all IBM PowerPC microprocessors and embedded controllers.

The PowerPC 403GC includes an integrated MMU optimized for embedded applications, with a fully associative TLB. Each entry provides a translation for a memory page that can be one of several sizes. TLB replacement is managed by optimizing software. Each page can be assigned to a protection zone whose access attributes can be changed by updating a single register.

Bus Interface

- Direct-connect peripheral/SRAM/ROM and DRAM interfaces.
- Support for 8-, 16-, and 32-bit devices.
- Addressing for 512 MB of main storage.
- External bus master support using the internal DRAM controller.
- IEEE 1149.1 (JTAG) interface, test and debug support.

Interrupt Controller

- Low latency interrupt handling (three cycles typical, 37 cycles worst case including cache miss effects).
- Six external interrupt inputs (five regular, one critical).
- Dual-level interrupt structure for robust debug.

DMA Controller

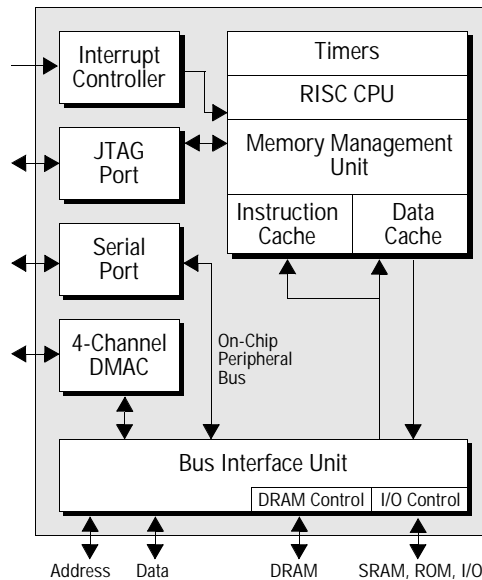
- Four independent DMA channels.
- Buffered, fly-by, memory-to-memory, and burst modes.
- Programmable for 8-, 16-, and 32-bit transfers.
- Data chaining.

Instruction and Data Caches

- Separate 2KB instruction and 1KB data caches.
- Two-way set-associative.
- Fetch-thru instruction cache.
- Write-back data cache.

Serial Port

- RS-232 serial communications.
- Programmable to 1.5 Mb/s.



Processors and Support Chips

Instruction Fetch, Branch and Dispatch Unit

- Four instruction prefetch queue.
- Branch folding and static branch prediction.
- Dispatches up to two instructions per cycle.

Power Management Capability

- Static low-power design.
- Dynamic power management and stand-by mode.
- Support for connections to 3.3V and 5V peripherals.

Timers

- 64-bit time base.
- 32-bit programmable interval timer with auto-reload.
- Fixed interval timer for system maintenance.
- Watchdog timer for system error recovery.

Memory Management Unit

- MMU is precache (cache tags are physical addresses).
- 8 page sizes (1K - 16M by powers of 4).

- 64 entry fully associative TLB with software replacement.
- 16 protection zones.

Specifications

Technology	0.5 μ m CMOS process, 3-layer metal
Transistors	~635,000
Temperature	0° C to 85° C
Frequency	25 MHz or 33 MHz
Signal I/O	126
Power Supply	3.3V \pm 5% (support for 5V I/Os)
Performance	72K Dhrystones/s @ 33 MHz
Performance/Power	155 MIPS/Watt (Dhrystone 2.1)
Power Dissipation	200 mW at 25 MHz
Packaging	Plastic quad flat pack (160 pins)

Availability

- Available now.

Contact

United States and Canada

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531
Tel: (800) PowerPC
Fax: (800) POWERfax

IBM homepage:
<http://www.ibm.com>

IBM Microelectronics homepage:
<http://www.chips.ibm.com>

Fax Service: (415) 855-4121

Japan

IBM
800, Ichimiyake
Yasu-cho, Yasu-gun
Shiga-ken, Japan 520-23
Tel: (81) 775-87-4745
Fax: (81) 775-87-4735

Europe

IBM
La Pompignane BP 1021
34006 Montpellier, France
Tel: (33) 6713-5757 (French)
Tel: (33) 6713-5756 (Italian)
Fax: (33) 6713-5750*
*from Paris add 16

IBM
Informations Systeme GmbH
Laatzener Str. 1
30539 Hannover, Germany
Tel: (49) 511-516-3444 (English)
Tel: (49) 511-516-3555 (German)
Fax: (49) 511-516-3888

IBM27-82660 PCI/Memory Chip Set

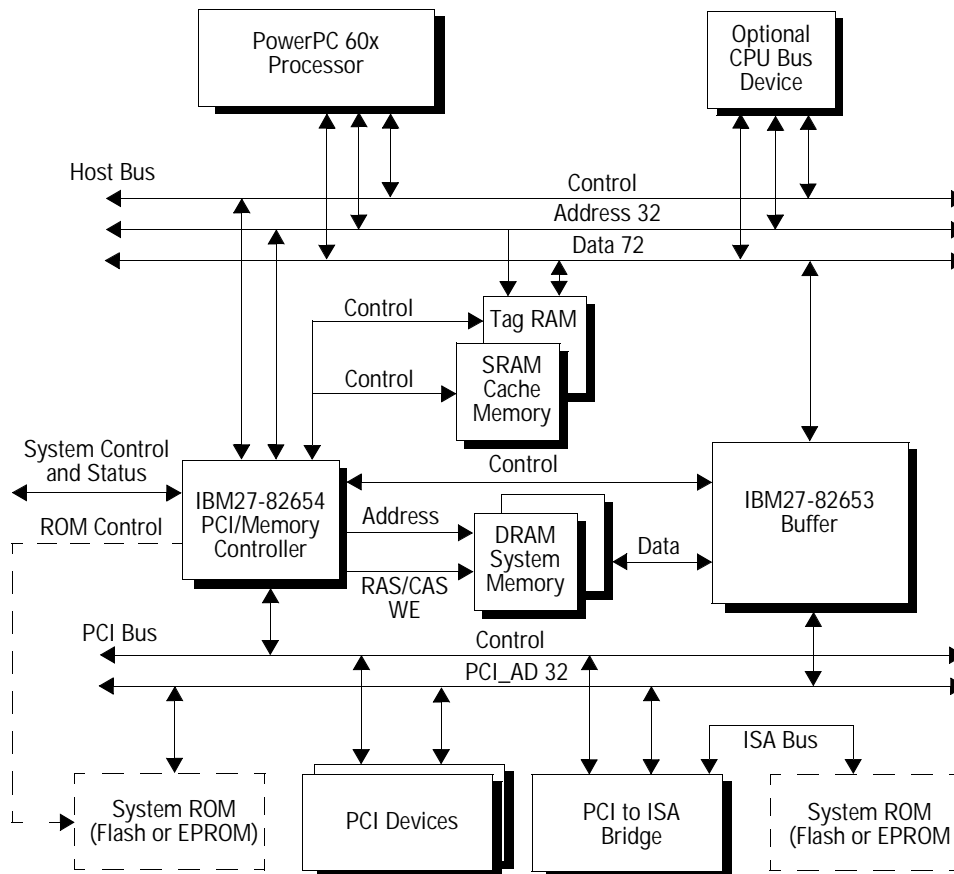
Controller

IBM Microelectronics

The IBM27-82660 PowerPC to PCI Bridge (the 660 Bridge) interfaces the PowerPC 60x bus to the PCI bus, DRAM, and ROM; controls SRAM and tag RAM to form an L2 cache; and provides the system central resource. The 660 Bridge is PowerPC Reference Platform compliant, and includes the IBM27-82663 data buffer and the IBM27-82664 controller.

General Features

- PowerPC Reference Platform 1.0 and 1.1.
- Extensive programmability.
- Flexible and programmable error handling.
- Low-cost plastic quad flat packs.
- Dual split bus structure CUP-PCI.
- Bi-endian operation (swaps and munges).



Processors and Support Chips

Typical Performance	Read	Write
70 ns Page DRAM	8-4-4-4	4-4-4-4
60 ns EDO DRAM	7-3-3-3	3-3-3-3
Sync 9 ns SRAM Read	3-1-1-1 2-1-1-1-...	2-1-1-1
Async 15 ns SRAM Read	3-2-2-2 3-2-2-2 ...	3-2-2-2
PCI-to-Memory Read	5-1-1-1-1-1-1-1 6-1-1-1-1-1-1-1 ... 6-	
PCI-to-Memory Write	5-1-1-1-1-1-1-1 3-1-1-1-1-1-1-1 ... 3-	

CPU

- PowerPC 601, 602 and 604 families.
- Up to 2 CPUs at 66 MHz on the CPU bus.
- Address pipelining.
- MCP# and TEA#/INT# error reporting.
- No-DRTRY#/Fast-L2 mode support.

L2 Cache Controller

- Look aside, direct mapped, write through.
- 256k, 512k or 1M SRAM support.
- Sync or asynch SRAM and tagRAM.
- Can be disabled.

PCI

- PCI 2.0/2.1, 33 MHz, 3.3v/5v.
- Memory accesses snooped to L1 and L2.
- ISA master support.
- PCI resource locking.
- Type 0 and type 1 configuration cycles.

DRAM

- ECC or parity DRAM error checking.
- Page mode or EDO DRAM.
- Up to 1G DRAM with 168-pin DIMMs.
- Up to 512M DRAM with 72-pin SIMMs.
- Up to 8 memory banks (8 RAS#, 8 CAS#, and two WE#).
- Extensive programmability and flexibility.
- Onboard refresh timer/counter.

ROM

- Up to 2M of ROM on PCI or I/O bus.
- Flash ROM read, write, and lock-out.
- 8 to 64 bit conversion on reads.
- Single-beat and burst reads.

Availability

- Available now.

Contact

United States and Canada

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531
Tel: (800) PowerPC
Fax: (800) POWERfax

IBM homepage:
<http://www.ibm.com>

IBM Microelectronics homepage:
<http://www.chips.ibm.com>

Fax Service: (415) 855-4121

Japan

IBM
800, Ichimiya,ke,
Yasu-cho, Yasu-gun
Shiga-ken, Japan 520-23
Tel: (81) 775-87-4745
Fax: (81) 775-87-4735

Europe

IBM
La Pompignane BP 1021
34006 Montpellier, France
Tel: (33) 6713-5757 (French)
Tel: (33) 6713-5756 (Italian)
Fax: (33) 6713-5750*
*from Paris add 16

IBM
Informations Systeme GmbH
Laatzener Str. 1
30539 Hannover, Germany
Tel: (49) 511-516-3444 (English)
Tel: (49) 511-516-3555 (German)
Fax: (49) 511-516-3888

PowerPC 601® RISC Microprocessor

Microprocessor

IBM Microelectronics

The PowerPC 601 microprocessor is the first implementation of the PowerPC family of Reduced Instruction Set Computer (RISC) microprocessors. It is a 32-bit implementation of the PowerPC Architecture™ and achieves high performance through concurrent execution of up to three instructions in three parallel execution units: the fixed-point unit, floating-point unit and instruction-fetch and branch unit.

The IBM Microelectronics 100 MHz PowerPC 601 processor is a higher-performance processor that is functionally identical to the original PowerPC 601 processor. The 100 MHz processor was developed in a 0.5μ CMOS technology with a high-performance 2.5v, .25μm Leff device and multilevel 1.8μm pitch wiring capability to achieve a higher performance, lower power, and smaller die-size processor.

The 100 MHz PowerPC 601 processor is packaged in the same 304-pin Ceramic Quad Flat Pack with improved electrical characteristics to minimize noise. Input, output, and ground pin locations are identical to the original PowerPC 601 processor. Positive power supply pins are divided between 2.5V pins for internal circuits and either 5.0V or 3.3V pins for the driver and receiver circuits.

Input and output signal levels are identical to the original PowerPC 601 processor through the development of special driver and receiver circuits that interface with the 2.5V internal circuits. A more sensitive clock receiver circuit has been developed to interface with the higher-performance clock signals. The clock rate of the PowerPC 601 100 MHz microprocessor may be extended to 120 MHz by matching system operating conditions with the processor specifications. Contact your local IBM Microelectronics Field Application Engineer.

Features

- *Instruction Queue and Dispatch*
 - Dispatches up to three instructions/cycle.
 - 8-word instruction-fetch bus from cache.
- *Instruction Fetch and Branch Processing*
 - Early exposition of branches effectively producing zero-cycle branches.
 - Four-entry translation shadow buffer.
- *Integer Execution*
 - Most instructions execute in one cycle.
 - Hardware multiply and divide.
 - Thirty-two 32-bit general-purpose registers.
- *Floating-Point Execution*
 - IEEE-754 single- and double-precision.
 - Hardware support for all data types.
 - Single-cycle multiply-add instruction.
 - 32-bit and 64-bit general-purpose registers.
- *Memory Management*
 - 52-bit virtual and 32-bit real addressing.
 - Four block address-translation registers.
 - 256-entry two-way set associative TLB.
 - Big- or little-endian addressing.
- *Cache*
 - 32 KB, combined, 8-way associative.
 - Full set of cache control instructions.
 - Physically tagged and addressed.
 - Selectable (via MMU) store-in, store-through or non-cached modes.
 - Non-blocking.
- *Memory Queue*
 - 2-entry read queue, 3-entry write queue.
 - Hardware memory coherency via bus snooping.

Processors and Support Chips

- *Bus Interface Unit*
 - General-purpose interface for wide range of system configurations.
 - 32-bit address bus, 64-bit data bus.
 - Powerful diagnostic and test interface.
 - Secondary cache support.
 - Operates at integer multiples of processor cycle-time.
 - Graphics coprocessor support.
 - Multiprocessor support.
 - MP primitive instruction support through atomic operations.

Specifications

Frequency	55/66/80 MHz	100 MHz	120 MHz
Technology	0.6 μ m CMOS process, 4-layer metal	0.5 μ m CMOS process	0.5 μ m CMOS process, 5-layer metal
Die Size	10.95 mm x 10.95mm	8.6 mm x 8.6 mm	8.6 mm x 8.6 mm
Transistors	2.8 million	2.8 million	2.8 million
Temperature	0° to 85° C	10° to 85° C	Matched to processor specification
Performance	74 SPECint92 @ 66MHz 83 SPECfp92 @ 66MHz 90 SPECint92 @ 80MHz 100 SPECfp92 @ 80MHz	112 SPECint92 (est.) 125 SPECfp92 (est.)	135 SPECint92(est.) 150 SPECfp92 (est.)
Signal I/O	184	184	184
Power Supply	3.6V \pm 5%	5.0V \pm 5% and 2.5V \pm 5%	Matched to processor specification
Power Dissipation	7W @ 66 MHz 8W @ 80 MHz	4W	6.8W (est.)
Packaging	304-pin C4 CQFP	304-pin C4 CQFP	304-pin C4 CQFP

Availability

- Available now.

Contact

Contact

United States and Canada

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531
Tel: (800) PowerPC
Fax: (800) POWERfax

IBM homepage:
<http://www.ibm.com>

IBM Microelectronics homepage:
<http://www.chips.ibm.com>

Fax Service: (415) 855-4121

PowerPC 602™ RISC Microprocessor

Microprocessor

IBM Microelectronics

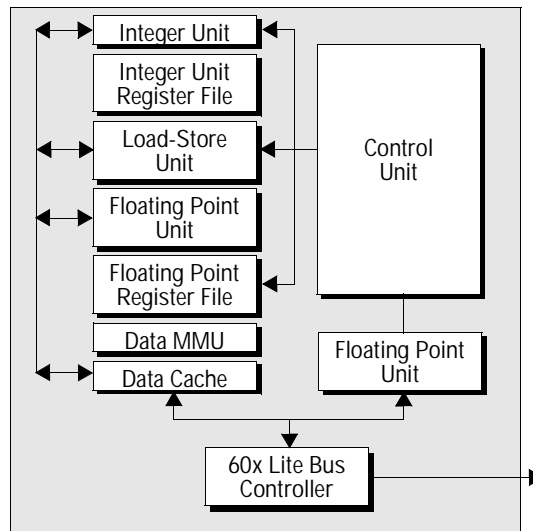
The PowerPC 602 is a 32-bit implementation of the PowerPC family of Reduced Instruction Set Computer (RISC) microprocessors. It is intended for use in portable and small form factor uniprocessor applications such as PDAs. It achieves its performance through concurrent execution of up to two instructions per cycle in its four parallel execution units: the fixed-point unit, floating point unit, branch processing unit, and the load/store unit. The low-power design of the PowerPC 602 microprocessor, and the power management features it incorporates, offer competitive advantages in performance-oriented, power-sensitive portable applications.

The PowerPC Architecture™ is derived from the IBM Performance Optimized With Enhanced RISC (POWER™) architecture. The PowerPC Architecture shares all the benefits of the POWER Architecture, but is optimized for single-chip implementation. The PowerPC architecture is a major component of the PowerOpen™ environment.

The PowerPC Architecture offers a complete range of processor solutions for computing needs from embedded applications through multi-processor mainframe systems. Its unique combination of high performance, wide operating systems applicability, and small die size has resulted in its unprecedented success in the RISC computing market.

Features

- *Control Unit*
 - Dispatches one instruction per cycle.
 - Supports superscalar execution.
 - Branch folding implemented.
 - Retires up to one instruction per cycle.
- *Load/Store Unit*
 - One cycle cache access.
 - Speculative cacheable loads (for no data dependencies).



Processors and Support Chips

- *Integer Unit*
 - One cycle add, subtract, shift, or rotate.
 - Hardware multiply and divide.
 - 32 x 32-bit general purpose registers.
- *Floating-Point Unit*
 - IEEE-754 compliant single-precision operations.
 - 32 x 32-bit floating point registers.
- *Cache Unit*
 - Separate 4K instruction and data caches, 2-way set associative.
 - 3-state coherency protocol.
 - Physically addressed tag and cache arrays Copy-back or write-thru data cache.
 - Data coherency in hardware.
- *Memory Management Unit*
 - Separate 32-entry instruction and data TLBs.
 - Separate instruction and data BATs (4 each), offer protection and translation for 128K-4MB of memory.
 - 32-bit PowerPC Architecture compliant mode.
 - Additional protection-only-mode offers protection of up to 4MB per TLB.
- *Bus Interface Unit*
 - General purpose interface for a wide range of system configurations.
 - Multiplexed 32-bit address and 64-bit data bus.
- Powerful diagnostic and test interfaces through the Common On-Chip Processor (COP) and IEEE 1149.1 (JTAG) interface.
- *Power Management Unit*
 - Static low-power design.
 - Dynamic power management.
 - Hardware support for power saving modes.
 - Internal clock multiplier for operation at 2x and 3x of bus clock.

Specifications

Technology	0.5 μ m CMOS process, 4-layer metal
Die Size	7.04 mm x 7.04mm
Transistors	~1 million
Temperature	0° to 105° C
Performance (est.)	40SPECint92 @ 66 MHz 48SPECint92 @ 80 MHz
Signal I/O	98
Power Supply	3.3V \pm 0.3V
Power Dissipation	Less than 1200 mW @ 66 MHz, 3.3V
Packaging	Plastic quad flat pack (144 pins)

Availability

- Available now.

Contact

United States and Canada

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531
Tel: (800) PowerPC
Fax: (800) POWERfax

IBM homepage:
<http://www.ibm.com>

IBM Microelectronics homepage:
<http://www.chips.ibm.com>

Fax Service: (415) 855-4121

PowerPC 603® RISC Microprocessor

Microprocessor

IBM Microelectronics

The PowerPC 603 microprocessor is a 32-bit implementation of the PowerPC family of Reduced Instruction Set Computer (RISC) microprocessors. The PowerPC 603 microprocessor provides both industry leading RISC performance and power management to the notebook and energy sensitive desktop markets. High performance is achieved through concurrent execution of up to five instructions in five parallel execution units: the fixed-point unit, floating point unit, branch unit, system unit, and load/store unit. Low-power is delivered through a low power static design and dynamic power management with three power saving modes. It is this industry segment leading combination of high performance and low power that offers a competitive edge to the system developers using the PowerPC 603 microprocessor.

The 100 MHz version extends the performance leadership of the PowerPC 603 microprocessor in notebooks and energy sensitive desktops. The design, enhanced for higher speed and performance, contains twice the cache size of the original PowerPC 603 microprocessor and extends its speed from 80 MHz to 100 MHz.

The PowerPC Architecture™ is derived from IBM's Performance Optimized With Enhanced RISC (POWER™) architecture. The PowerPC Architecture shares all the benefits of POWER and is optimized for single-chip implementations.

Features

- *Power Management Unit*
 - Static low-power design.
 - Dynamic power management.
 - Support for power saving modes.
 - Processor clock multiplier of 1x, 1.5x, 2x, 2.5x, 3x, 3.5x, and 4x from bus clock.
- *Instruction Fetching and Branch Unit*
 - 6-instruction prefetch queue.
 - Static branch prediction.
- *Dispatch Unit*
 - Dispatches 2 instructions per cycle.
 - 4-stage pipeline: fetch, dispatch, execute, and complete.
- *Fixed-Point Execution Unit*
 - One cycle add, subtract, shift, or rotate.
 - Hardware multiply and divide.
 - Thirty-two 32-bit General Purpose Registers.
- *Floating-Point Unit*
 - Optimized for single-precision multiply/add.
 - IEEE-754 standard single- and double-precision floating point arithmetic.
 - Thirty-two 32-bit General Purpose Registers.
- *System Unit*
 - Executes Condition Register logical, special register transfer, and other system instructions.
 - Execute integer add/compare instructions.
- *Memory Management Unit*
 - 52-bit virtual and 32-bit real addressing.
 - 8 Block Address Translation registers.
 - 64-entry, 2-way data and instruction TLB Fast-trap mechanism for software reload TLB.
 - Support Big/Little-endian addressing.
- *Bus Interface Unit*
 - General purpose interface (32-bit address and 64- or 32-bit data bus.)
 - Powerful diagnostic and test interface through the Common On-Chip Processor (COP) and IEEE 1149.1 (JTAG) interface.

Processors and Support Chips

- *Cache Unit*
 - 16k, 4 way or 8k, 2 way set associative instruction cache.
 - 16k, 4 way or 8k, 2 way set associative data cache 3-state coherency.
- Physically tagged and addressed.
- Copy-back data cache.
- Data coherency in hardware.
- *Load/Store Unit*
 - One cycle cache access.

Specifications

Frequency	66 and 80 MHz	100 MHz
Technology	0.5 μ CMOS, four levels of metal	0.5 μ CMOS, four levels of metal
Die Size	7.4 mm x 11.5 mm	8.4 mm x 11.67 mm
Transistors	1.6 million	2.6 million
Temperature	0° to 105° C	0° to 105° C
Performance	75 SPECint92, 65 SPECfp92 @ 80 MHz 62 SPECint92, 54 SPECfp92 @ 66 MHz	120 SPECint92, 105 SPECfp92 @ 100 MHz (est.)
Signal I/O	165	165
Power Supply	3.3V \pm 5%	3.3V \pm 5%
Power Dissipation	2.5W @ 80 MHz 2.2W @ 66.67 MHz	3W @ 100 MHz
Packaging	C4 ceramic quad flat pack (240 pins)	C4 ceramic quad flat pack (240 pins) Ball grid array (16 x 16)

Availability

- Available now.

Contact

United States and Canada

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531
Tel: (800) PowerPC
Fax: (800) POWERfax

IBM homepage:
<http://www.ibm.com>

IBM Microelectronics homepage:
<http://www.chips.ibm.com>

Fax Service: (415) 855-4121

PowerPC 603e™ RISC Microprocessor

Microprocessor

IBM Microelectronics

The PowerPC 603e microprocessor is a 32 bit implementation of the PowerPC family of Reduced Instruction Set Computer (RISC) microprocessors. The PowerPC 603e is especially suitable for the notebook, mobile and power conscious desktop computing segments. The extremely low typical power consumption of 3.3 watts at 200MHz makes it ideal for battery powered portables while delivering impressive performance of desktop system productivity applications.

The combination of PowerPC Architecture™ and state-of-the-art CMOS manufacturing process technology enable the 603e to feature a 2.5 volt core logic design as well as delivering 3.3 volts for I/O support.

Enhancements to this generation of the PowerPC 603e microprocessor family include:

- Higher clock frequencies delivering higher levels of performance.
- Additional bus divider ratios making it easier to design in.
- A new performance enhancing feature supporting misaligned little endian accesses for certain operating system environments.

Features

- *Power Management Unit*
 - Static low-power design.
 - Dynamic power management.
 - Processor:bus clock ratio of half integer increments up to 6:1.
- *Instruction Fetching and Branch Unit*
 - 6-instruction prefetch queue.
 - Static branch prediction.

- *Dispatch Unit*
 - Dispatches 2 instructions per cycle.
 - 4-stage pipeline: fetch, dispatch, execute, and complete.
- *Load/Store Unit*
 - One cycle cache access.
 - Executes cache and TLB instructions.
 - Alignment and number denormalization.
 - Hit under reload instruction.
- *Fixed-Point Execution Unit*
 - One cycle add, subtract, shift, or rotate
 - Hardware multiply and divide.
 - Thirty-two, 32-bit general purpose registers.
- *Floating-Point Execution Unit*
 - Optimized for single-precision multiply/add.
 - IEEE-754 standard single-and double-precision floating point arithmetic.
 - Thirty-two, 64-bit floating point registers.
- *System Unit*
 - Executes condition register logical, special register transfer, and other system instructions.
 - Executes integer add/compare instructions.
- *Memory Management Unit*
 - 52-bit virtual and 32-bit real addressing.
 - 8 Block Address Translation registers.
 - 64-entry, 2-way data and instruction TLB.
 - Fast-trap mechanism for software reload TLB.
 - Support Big/Little-endian addressing.

Processors and Support Chips

- *Cache Unit*
 - 16K, 32 byte line, 4-way set associative instruction cache.
 - 16K, 32 byte line, 4-way set associative data cache.
 - 3-state coherency (MEI).
 - Physically tagged and addressed.
 - Copy-back data cache.
 - Hardware support for data coherency.
- *Bus Interface Unit*
 - General purpose interface for a wide range of system configurations.
 - 32-bit address and selectable 64- or 32-bit data bus.
 - Powerful diagnostic and test interface through the Common On-Chip Processor (COP) and IEEE 1149.1 (JTAG) interface.
 - Parity checking on bus.
 - Fast reset due to Level Sensitive Scan Design (LSSD).

Available

- Available now.

Specifications

Technology	0.5 μ m/0.25 Leff CMOS, 5-layer metal
Die Size	7.5 mm x 10.5 mm
Transistors	2.6 million
Temperature	0° to 105° C
Performance (est.)	4.1 SPECint95, 3.0 SPECfp95 @ 150/60, 1M L2 w/60ns DRAM 4.3 SPECint95, 3.2 SPECfp95 @ 160/64, 1M L2 w/60ns DRAM 4.5 SPECint95, 3.3 SPECfp95 @ 166/66, 1M L2 w/60ns DRAM 4.6 SPECint95, 3.3 SPECfp95 @ 180/60, 1M L2 w/60ns DRAM 5.1 SPECint95 3.7 SPECfp95 @ 200/66, 1M L2 w/sync SDR
Signal I/O	165
Power Supply	3.3V \pm 5% I/O 2.5V \pm 5% core
Power Dissipation Typical/Max (est.)	3.2/4.5W @ 166 MHz 3.3/6.0W @ 200 MHz
Packaging	C4 ceramic quad flat pack (204 pins) Ball grid Array (256 pins)

Contact

United States and Canada

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531
Tel: (800) PowerPC
Fax: (800) POWERfax

IBM homepage:
<http://www.ibm.com>

IBM Microelectronics homepage:
<http://www.chips.ibm.com>

Fax Service: (415) 855-4121

PowerPC 604® RISC Microprocessor

Microprocessor

IBM Microelectronics

The PowerPC 604 microprocessor family delivers the performance needed to support the new graphically rich, compute and multimedia intensive applications of today and provides the platform for growth well into the future. By combining a PowerPC microprocessor and these new and innovative applications on a desktop, home and small business users can begin to realize the value and benefits the PC was destined to deliver.

For PC server and low-end workstation users, the 32-bit implementation of the PowerPC 604 microprocessor family reaches new levels of performance by issuing instructions at a rate of 4 instructions per cycle thus achieving balanced execution of integer and floating point operations.

The PowerPC 604 microprocessor is software and bus compatible with the PowerPC 603e microprocessor, which is specifically designed for energy conscious mobile and low-end desktop systems. This compatibility thus enables a full line of PowerPC microprocessor solutions for the mobile thru workstation platforms for home and business.

Features

- *Advanced Superscalar CPU Design*
 - Speculative execution past 2 unresolved branches
 - 16-entry reorder buffer
 - 2-entry reservation stations per execution unit
 - Register renaming on general purpose (GPR), floating point (FPR), and condition registers (CR)
 - 6 stage pipeline to achieve high speed, including fetch, decode, dispatch, execute, completion and writeback
- *Dynamic Branch Prediction*
 - Branch prediction in fetch, decode and dispatch stages
 - 64-entry, fully associative branch target address cache
 - 512-entry branch history table
 - Enhanced instruction prefetching supporting speculative execution
 - Instructions can be executed out-of-order and are completed in order to support precise exceptions
- *Memory Management*
 - 52-bit virtual and 32-bit real addressing
 - 4 instruction, 4 data block address translation registers
 - 128-entry, 2-way set associative instruction TLB
 - 128-entry, 2-way set associative data TLB
- *Multiprocessing Support*
 - Coherent cache access (MESI)
 - Bus snooping
 - Separate data cache tag array
- *Dispatch Unit*
 - 8-instruction buffer
 - Dispatches 4 instructions per cycle
- *Six Execution Units*
 - 1 branch
 - 3 integer
 - 1 Floating point unit (IEEE-754 single and double precision)
 - 1 load/store
- *Caches*
 - 16K bytes, 4-way set associative instruction cache
 - 16K bytes, 4-way set associative data cache

Processors and Support Chips

- Non-blocking, write-thru or copy-back data cache
- Byte parity on both caches
- Software cache disable, locking and invalidate
- *Bus Interface Unit*
 - 32-bit address and 64-bit data buses with byte parity
 - 60x bus compatible (split transaction, pipelined)
 - An optional mode optimized for fast secondary cache
 - Up to 66 MHz bus clock
 - On-chip PLL to generate 1x, 1.5x, 2x or 3x processor clock from the bus clock
- *Software and System Support*
 - Performance monitor functions
 - Instruction and data address breakpoints
 - Nap mode power management
 - IEEE 1149.1 (JTAG) interface

Availability

- Available now.

Specifications

Technology	0.5 μ m CMOS, 4-layer metal
Die Size	12.4 mm x 15.8 mm
Transistors	3.6 million
Temperature	0° to 105° C
Performance (est.)	4.7 SPECint95, 4.4 SPECfp95 @ 120 MHz 5.2 SPECint95, 4.8 SPECfp95 @ 133 MHz 5.2 SPECint95, 4.4 SPECfp95 @ 150 MHz 5.7 SPECint95, 4.9 SPECfp95 @ 166 MHz4 6.2 SPECint95, 5.3 SPECfp95 @ 180 MHz
Signal I/O	171, CMOS/TTL compatible
Power Supply	3.3V
Power Dissipation Typical/Max (est.)	3.2/4.5W @ 166 MHz 3.3/6.0W @ 200 MHz
Packaging	C4 ceramic quad flat pack (204 pins), Ball grid array (256 pins)

United States and Canada

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531
Tel: (800) PowerPC
Fax: (800) POWERfax

Contact

IBM homepage:
<http://www.ibm.com>

IBM Microelectronics homepage:
<http://www.chips.ibm.com>

Fax Service: (415) 855-4121

PowerPC 604e™ RISC Microprocessor

Microprocessor

IBM Microelectronics

The PowerPC 604e microprocessor is a 32-bit implementation of the PowerPC family of Reduced Instruction Set Computer (RISC) microprocessors. It is a functionally equivalent, enhanced microarchitecture derivative of the PowerPC 604 microprocessor using split voltages of 2.5 VDC for core logic and 3.3 VDC for I/O. The PowerPC 604e microprocessor is targeted at the workstation, PC server and power user desktop segments. The suite of operating environments available to systems designed in accordance with the PowerPC microprocessor Common Hardware Reference Platform Specification includes: Mac OS™, Windows NT™, AIX™ and Solaris™.

Enhancements to the PowerPC 604e microprocessor, over its predecessor, the PowerPC 604 microprocessor include:

- Size of instruction and data caches have been doubled.
- Higher clock frequencies with increased bus divider ratio.
- A new performance enhancing feature which supports misaligned little endian accesses for certain operating system environments.
- A built-in performance monitor.

Features

- *Dispatch Unit*
 - Dispatch up to 4 instructions per cycle.
 - 8-instruction dispatch buffer.
- *Completion Unit*
 - Completes up to 4 instructions plus 1 store and 1 branch per cycle integer unit.
 - 2 Simple Fixed Point units.
 - 1 Complex Fixed Point unit.

- *Load/Store Unit*
 - Hardware supported mis-aligned little endian accesses.
 - Hardware controlled load-multiple and store-multiple registers and byte strings.
 - Data alignment to byte addresses.
 - Out of order loads and stores.
- *Integrated Floating Point Unit*
 - IEEE-754 standard single-and double-precision floating point arithmetic.
- *Cache*
 - Separate instruction and data caches, each 32K bytes, 4-way set associative.
 - 32-byte cache line.
 - Physically indexed, physical tags.
 - Hardware invalidate all cache lines.
 - Write-in and write-through data cache.
 - Data cache line-fill buffer forwarding.
 - Software cache disable.
- *Branch Prediction and Processing*
 - 512-entry branch history table.
 - 64-entry branch target address cache, fully associative.
 - Branch prediction for unresolved branches.
- *Memory Management Structure*
 - 32-bit real memory support for up to 4 GB.
 - 64-entry 2-way instruction and data TLB.
 - Hardware controlled TLB miss handling.
- *Multiprocessor Support*
 - Bus snooping.
 - 4-state MESI data cache coherency control.
 - Dual port data cache tags.
 - Software controlled Instruction cache coherency, programmable coherent instruction fetch mode.

Processors and Support Chips

- *Bus Interface*
 - 32-bit real address.
 - 64-bit data.
 - Processor Clock: Bus Clock ratios of 1:1, 3:2, 2:1, 5:2, 3:1, 7:2, 4:1, 5:1, 6:1.
- *Performance Monitor*
 - Four programmable event counting registers.
 - Programmable trigger or interrupt signal.
- *Testability*
 - IEEE 1149.1 (JTAG) compatible chip interface.
 - Level Sensitive Scan Design (LSSD).

Availability

- Available now.

Specifications

Technology	0.5 μ m/0.25 Leff CMOS, 5-layer metal
Die Size	144 mm ²
Transistors	5.1 million
Frequency	166, 180, 200 MHz
Temperature	0° to 105° C
Performance (est.)	6.5 SPECint95, 6.1 SPECfp95 @ 166/66, 1M L2 w/Sync DRAM 6.9 SPECint95, 6.1 SPECfp95 @ 180/60, 1M L2 w/Sync DRAM 7.8 SPECint95, 6.5 SPECfp95 @ 200/66, 1M L2 w/Sync DRAM
Signal I/O	171
Power Supply	2.5V \pm 5% core 3.3V \pm 5% I/O
Power Dissipation (est. typical)	14W @ 166 MHz
Packaging	C4 ceramic quad flat pack, Ball grid array, PGA

Contact

United States and Canada

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531
Tel: (800) PowerPC
Fax: (800) POWERfax

IBM homepage:
<http://www.ibm.com>

IBM Microelectronics homepage:
<http://www.chips.ibm.com>

Fax Service: (415) 855-4121

PowerPC 620™ RISC Microprocessor

Microprocessor

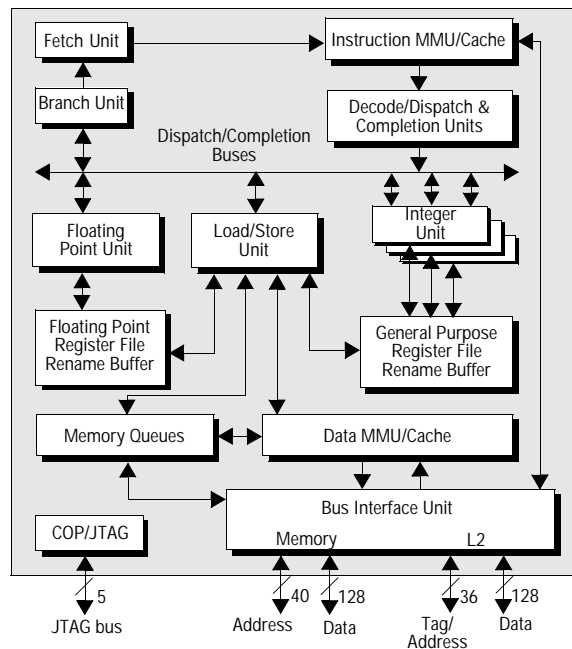
IBM Microelectronics

The PowerPC 620 RISC microprocessor is the first chip in a new product line of servers and high-end workstations in the PowerPC microprocessor family. It features a high bandwidth memory subsystem for symmetric multiprocessing, transaction processing and numerically intensive computing. It is the first 64-bit implementation of the PowerPC Architecture supporting both 32- and 64-bit applications.

The PowerPC 620 microprocessor has a center frequency of 133 MHz and uses a 5-stage pipeline: fetch, dispatch, execute, complete and writeback. Its superscalar design controls independent branch, integer, floating-point and load/store execution units. Instructions are dispatched to the execution units in program order, executed out-of-order, and completed in-order to support precise expectations.

Features

- *64-Bit Advanced Superscalar Processor*
 - Fetch and dispatch up to four inst/cycle.
 - Speculative execution past four unresolved branches.
 - Register renaming for integer, floating-point registers.
- *Six Execution Units*
 - Branch unit with four reservation stations.
 - Three integer units with two reservations stations each.
 - Floating-point unit supporting IEEE-754 single- and double-precision with two reservation stations.
 - Load/store unit with three reservation stations.



Processors and Support Chips

- *Static/Dynamic Branch Predictions*
 - Branch prediction in fetch and dispatch stages.
 - 256-entry branch target address cache.
 - 2048-entry branch history table.
- *Caches*
 - 32KB, 8-way set associative instruction cache.
 - 32KB, 8-way set associative non-blocking data cache.
 - Write-thru or write-back data cache modes.
 - Parity protection on both caches.
- *Memory Management and MP Support*
 - 80-bit virtual, 64-bit effective addressing.
 - 128-entry, 2-way set associative shared TLB.
 - 20-entry, fully associative segment lookaside buffer.
 - 16 segment registers for 32-bit mode support.
 - Separate 64-entry, fully associative effective-to-real address translators for instructions and data.
 - Four instruction, four data block address translation registers.
 - Coherent data cache (4-state MESI protocol).
- *L2 Cache Interface*
 - 128-bit CMOS/GTL data interface.
 - Unified instruction and data secondary cache.
- Direct-mapped, physically indexed, physically tagged.
- Capacity configurable from 1-128MB.
- Interface clocked at 1/2, 1/3, or 1/4 the processor clock.
- On-chip phase-lock-looped.
- *Software and System Support*
 - Performance monitor functions.
 - Power management.
 - IEEE 1149.1 (JTAG) interface and on-chip LSSD.
 - Array built-in self test and on-chip debug support.

Specifications

Technology	0.5 μ static CMOS, four levels of metal
Die Size	17.1 mm x 18.2 mm
Transistors	~7 million
Performance (estimated)	225 SPECint92 300 SPECfp92 @ 133 MHz
Power Supply	3.3V \pm 0.3V
Power Dissipation	30W @ 133 MHz
Signal I/O	482
Packaging	25 x 25 Ball Grid Array

Availability

- Available now.

Contact

United States and Canada

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531
Tel: (800) PowerPC
Fax: (800) POWERfax

IBM homepage:
<http://www.ibm.com>

IBM Microelectronics homepage:
<http://www.chips.ibm.com>

Fax Service: (415) 855-4121

PCI 9060ES

Controller

PLX Technology

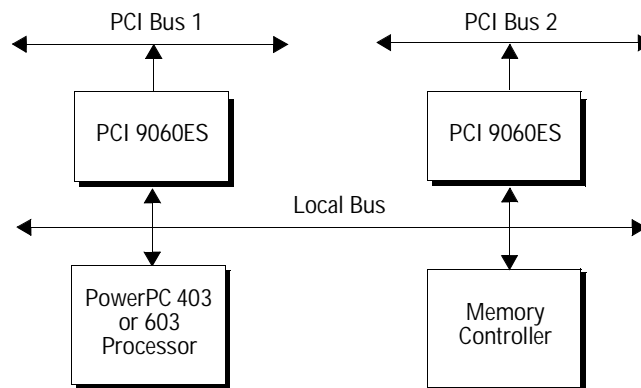
The PCI9060ES provides a compact high performance PCI bus master interface for adapter boards and embedded systems. The chip's local bus may connect directly to IBM's PowerPC 403 or 603 processors.

The PCI9060ES allows the 403 or 603 processors and other intelligent controllers to perform direct bus master transfers on the PCI bus. The PCI9060ES also enables the local processor to configure other PCI devices in the system, an important feature for embedded systems.

The PCI9060ES supports both memory-mapped and I/O-mapped accesses to the local bus from the PCI bus. Two independent bi-directional FIFOs support zero wait-state Direct Slave burst transfers between host and local memory and Direct Bus Master transfers between a Local Bus Master and the PCI bus.

Features

- PCI Bus Master and Bus Slave transfers up to 132 megabytes/sec supporting three architectures:
 - PCI direct master adapter
 - PCI slave adapter
 - PCI embedded system
- Two bi-directional FIFOs (each 16 Lwords deep) for zero wait-state burst operation; one for Direct Master interface and one for Direct Slave interface.
- Supports both multiplexed and non-multiplexed local buses, 32 or 16 bit.
- Supports PCI bus accesses as both a PCI bus Master and Slave.
- Local bus can run asynchronously to the PCI clock.
- Four 32-bit mailbox and two 8-bit doorbell registers.
- Supports little endian/big endian swapping.
- Low-power CMOS in 208 Pin Plastic QFP Package.



Processors and Support Chips

Common Applications

The three most common applications for the chip are direct master adapter, direct slave adapter, and embedded system. The figure shows one possible design application.

- *Direct master adapter*—The PCI 9060ES typically connects an intelligent I/O controller (e.g. LAN, disk control, graphics) or processor to the PCI bus. It is called “direct” master because the data passes directly between the PowerPC 403 or 603 processor and the PCI bus, without an intermediate stop in the local adapter memory. The processor performs a local bus master cycle and the PCI 9060ES automatically translates this into a PCI bus master cycle. FIFOs in the PCI 9060ES allow the PCI bus and the adapter local bus to operate asynchronously and also enable zero wait-state burst transfers on the PCI bus. A direct master adapter may also require a slave. Typically, the slave mode is used by the host to configure or initialize the controller or processor’s registers. Data transfer is usually performed in direct master mode.
- *Direct slave adapter*—A direct slave adapter transfers data to and from the host as a target only. The PCI 9060ES provides the interface between the PCI host and the adapter’s memory controller. when the host

accesses the adapter, the PCI 9060ES translates the PCI cycles into local bus cycles. FIFOs in the PCI 9060ES enable asynchronous operation and efficient burst transfers.

- *Embedded system*—The PCI 9060ES generates the PCI bus under control of the embedded PowerPC 403 or 603 processor. The PCI9060ES, in conjunction with the embedded processor and BIOS, acts as the PCI system host and generates the Type 0 and Type 1 configuration cycles required to configure PCI devices.

Typically, most of the data transfer in a PCI embedded system involves the PCI devices, as master, accessing the embedded system memory as a target. This is because most of the PCI controllers available are designed to transfer data as masters. Therefore, for data transfer, the PCI 9060ES slave mode is used. The PCI 9060ES contains deep bi-directional FIFO in the slave path to ensure zero wait-state burst transfers between the PCI device and the embedded system local bus. Occasionally, the embedded processor will access a PCI device for initialization or configuration. Typically, it accesses these devices through the direct master mode.

Availability

- Available now.

Contact

PLX Technology, Inc.
625 Clyde Avenue
Mountain View, CA 94043
Tel: (415) 960-0448
Fax: (415) 960-0479
Web: <http://www.plxtech.com>

V292PBC

Controller

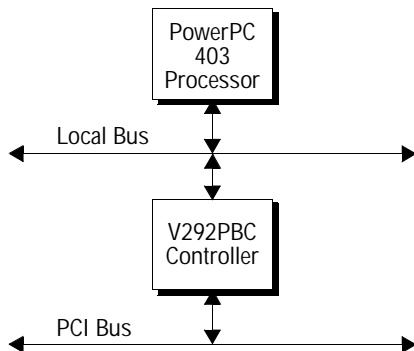
V3 Corporation

The V292PBC provides a flexible, high-performance, and economical way to add PCI connectivity to applications like imaging and networking. Whether you're creating a system with the PowerPC 403 or 401 processor as the PCI master, or designing an intelligent add-in card, the V292PBC from V3 Semiconductor is an ideal choice.

The V292PBC PCI bridge has 576 bytes of FIFO storage to give you plenty of buffering to handle continuous transfers of large data streams without tying up the local or PCI buses. The DYNAMIC BANDWIDTH ALLOCATION™ feature of the FIFOs allows you to adjust the “draining” and “filling” of the read and write FIFOs to most efficiently meet the requirements of the data streams. For example, each FIFO can be dynamically programmed to request the local or PCI bus based on FIFO traffic. You can balance your bus utilization to maximize overall system performance. Also, the priority of reads, writes, and FIFO flushes can be independently programmed to maintain strict data coherency.

Features

- I20-compliant messaging unit.
- Interface between IBM's PowerPC 403 or 401 processors and the industry standard PCI Bus.
- Fully compliant with PCI 2.1 specification.
- Configurable for primary master, bus master, or target operation.
- Up to 1K byte burst access support on both local and PCI interfaces.
- 576-bytes of programmable FIFO storage with DYNAMIC BANDWIDTH ALLOCATION™.
- Up to 33MHz PCI operation, independent of local processor speed.
- Two channel DMA controller.
- On-the-fly byte order (endian) conversion.
- 16 bi-directional mailbox registers with doorbell interrupts.
- Optional power-on serial EEPROM initialization.
- Support for real mode DOS “holes”.
- Low-power, high-performance CMOS technology in a low-cost 160 pin plastic quad flat pack.
- Up to 40 MHz versions available.



Processors and Support Chips

Availability

- Available now.

Contact

V3 Corporation
2348 Walsh Ave.
Suite G
Santa Clara, CA 95051
Tel: (408) 988-1050
Fax: (408) 988-2601

TollGate/VAS 96021

Controller

VLSI Technology

TollGate is an integrated, cost-effective bridge controller specifically designed for PowerPC microprocessor-based computers. It is a simple drop-in solution.

TollGate consists of two major functional blocks. One is the interface block between PCI and ISA bus. The second is the interface block between PCI and IDE bus.

The PCI and ISA bus interface supports both the master and slave transfer mode. It integrates 82C37A-compatible DMA controllers, 82C59A-compatible interrupt controllers, 74LS612-compatible memory mappers, 82284 clock generator, and 82288 ISA bus controller to give you a full range of ISA bus function support.

The PCI and IDE bus interface supports both master and slave transfer modes. By designing to the SFF8038i specification and PCI IDE controller specification, and including the switching capability between native and compatibility modes of the IDE interface, it is fully compatible with a full range of IDE drives.

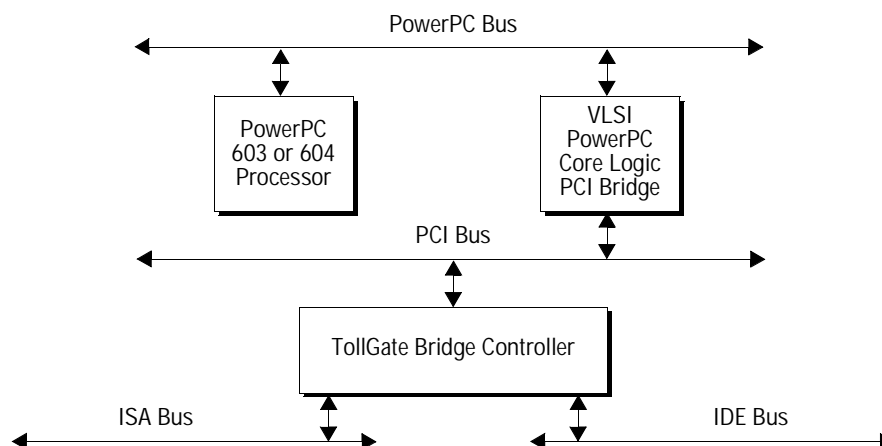
The TollGate controller functions are very flexible to the user's design needs. Most of its functions such as timing, resource selections, etc. are programmable via a set of internal device specification configuration registers.

Features

- 0.6-micron CMOS technology.
- 208 pins MQFP (metric quad flat pack).
- Easy integration into PowerPC processor roadmap with full x86 ISA bus support.

Specifications

- Meets PCI rev 2.1 specification for PCI bus interface.
- Allows up to 33 MHz operation on PCI bus.
- Supports PCI-to-ISA and ISA-to-PCI bus master cycle translations.
- Supports ISA, PCI bus concurrency.
- Translates DMA transfers for PCI slaves.
- Controls synchronization between PCI and ISA bus resources.



Processors and Support Chips

- Supports programmable memory regions to provide fast, positive address decode for PCI and ISA master.
- Implements subtractive decode for unclaimed access requests.
- Supports PCI-to-ISA posted memory writes.
- Supports PCI address/data parity generation, checking and error reporting.
- Supports PCI arbiter with host bridge, 5 PCI masters, IDE, SIO, and disabled features (fixed, rotating or combination).
- Provides power-on reset options for selecting various operation modes and ALT_RST pulse width (4-256 ISA CLKS).
- Provides external keyboard chip-select logic.
- Synchronous ISA bus operation up to 8.25 MHz.
- Allows support for external real-time clock.
- Allows keyboard controller to be addressed by the ISA, SD bus or on the XD bus.
- Supports 16 M ROM space on PCI bus.
- Integrates:
 - Two 82C37A DMA controllers
 - Two 74LS612 memory mappers (extended to support up to 4 GB)
 - Two 82C59A interrupt controllers
 - 82C54 timer
 - SA[19:0] and LA[23:17] address buffers
 - Clock generator
 - 82288-type ISA bus controller
 - Hidden ISA refresh controller
- Port A, B and NMI logic
- PCI bus interface controller
- PCI and ISA data buffers and steering logic
- XD bus control
- Programmable for 10- or 16-bit internal I/O addressing.
- IRQ[15:0] are individually programmable to be either PC/AT (edge-triggered) or PCI-compatible (level-sensitive).
- Supports IDE native mode and compatibility mode.
- Meets the SFF Committee Information Specification for Bus Master Programming Interface for IDE ATA Controllers (SFF8038i).
- Compliant with Intel programming interface rev 1.0.
- Supports scatter/gather function for IDE.
- Supports IDE pre-fetch and post-write buffer with multi-threading design.
- IDE interrupt programmable for different ISA IRQ.
- IDE bus master for the PIO-supported drive.
- Dual-channel bus master IDE capable of PIO mode 0-4 and DMA mode 0-2 (ATA-2).

Processors Supported

- PowerPC 603 and 604 microprocessors.

Availability

- Q4 96.

Contact

VLSI Technology
1109 McKay Drive
San Jose, CA 95131
Tel: (408) 434-3100
Fax: (408) 434-7584
Web: <http://www.vlsi.com>

GoldenGate II Core Logic

Controller

VLSI Technology

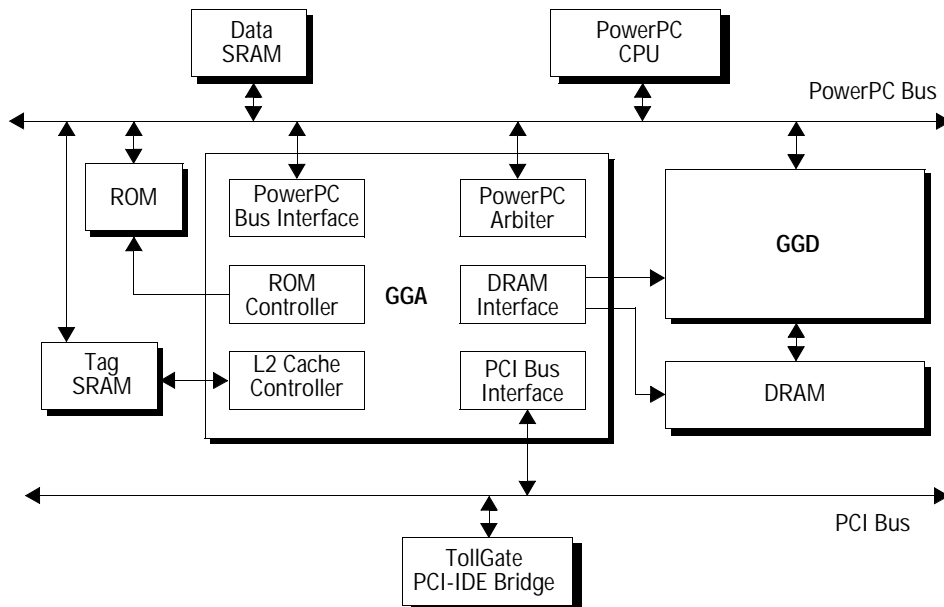
VLSI's GoldenGate II is a cost-effective core logic solution for PowerPC Platform-compliant systems supporting the PowerPC 603, 603e, 604 or 604e microprocessors. The two-chip GoldenGate II core logic incorporates a memory controller, a secondary (L2) cache controller, and provides a logical connection between the PowerPC microprocessor and the PCI bus.

The GoldenGate II-A chip, referred to as GGA, contains all the controls, address path and PCI data path. The GoldenGate II-D chip, referred to as GGD, is a three-way, 64-bit wide data path that connects the PowerPC bus to the DRAM (through a write-back buffer) and to GGA.

The PowerPC interface is operated at up to 66 MHz on the memory interface and the secondary cache interface. The PCI interface

optionally operates either synchronously with the PowerPC bus clock, at up to 33 MHz, or independently (asynchronous) from the PowerPC clock.

An internal memory controller supports flexible memory types and configurations. External buffers are not required. 64-bit burst read and cached ROM cycles are able to provide high ROM-access performance for system initialization. The L2 cache controller supports programmable copy-back and write-through cache mechanisms with a variety of cacheable sizes. The PCI bus provides various industry-standard peripheral connections to the microprocessor. All PCI master accesses of the system memory transactions are snooped by corresponding PowerPC bus cycles generated by GoldenGate II.



Processors and Support Chips

Features

- PowerPC Platform-compliant system controller.
- Two highly-integrated chips:
 - GoldenGate II-A—Address path and system controller (240 MQFP).
 - GoldenGate II-D—Data path controller (208 MQFP).
- High-performance PowerPC 603, 603e, 604 and 604e processor interface.
- Up to 66 MHz PowerPC bus operation.
- Integrated phase-locked loop.
- 3.3 V, 0.5 μ technology.
- Software-selectable CHRP- or PReP-compliant address map.
- Integrated secondary (L2) cache controller:
 - Supports fast-page mode DRAM, EDO DRAM, burst EDO DRAM and synchronous DRAM (SDRAM, PC-SDRAM), FPM-, EDO-, and BEDO-DRAM.
 - 64-bit memory organization.
 - Up to 768 MB of DRAM addressability in one to six 64-bit banks.
 - Supports 1 Mb x 4, 16 Mb x 1, 4 Mb x 4, 2 Mb x 8, 16 Mb x 4, and 8 Mb x 8 DRAM chips.
- Supports symmetrical or asymmetrical DRAM addressing.
- DRAM bank type, size and address are programmable for each bank.
- Programmable timing parameters for access times from 40 ns to 80 ns; independent of odd and even banks.
- Integrated ROM interface controller:
 - Supports two independent ROM banks with 8-, 16-, 32- and 64-bit wide interface.
 - Supports burst cache line-fill transactions from ROM and flash ROM writes.
 - Optional redirection of ROM accesses to the PCI bus to boot from PCI-based ROM.
- Integrated PCI interface controller:
 - Compliant with PCI 2.1 specification.
 - Concurrent operation of PowerPC and PCI buses.
 - Up to 33 MHz PCI bus operation, synchronous or asynchronous with the PowerPC bus.

Availability

- Available now.

VLSI Technology

1109 McKay Drive
San Jose, CA 95131
Tel: (408) 434-3100
Fax: (408) 434-7584
Web: <http://www.vlsi.com>

Contact

Processors and Support Chips

Software Generation and Debug Tools (Native)

Absoft C/C++ for AIX®, Windows NT™ and Power Macintosh™

Compilers, Debuggers, Utilities

Absoft Corporation

Absoft Corporation offers a variety of C/C++ development tools including the Absoft C/C++ for AIX compiler/debugger and the Absoft C/C++ Software Development Kit (SDK) for Windows NT or Power Macintosh.

Absoft C/C++ for AIX

Absoft C/C++ for AIX includes three native compilation systems: ANSI C, K&R C and C++. Support for templates, exceptions and STL is included. All compilers are Plum Hall validated and provide excellent diagnostics. They are link-compatible with Absoft F77.

Absoft C/C++ for AIX also includes the Absoft Fx, a screen oriented, multi-language (F77, C, C++, assembly) source-level debugger for AIX or Motif. You can display program variables in a variety of formats, modify variables while debugging, and display multiple program elements with a single command. Arrays can be indexed with expressions, and interactive source and symbol browsers provide fast access to functions and data. Breakpoints, variable monitors, and single-stepping at both the source and instruction level provide complete control over program execution.

Absoft C/C++ SDK

The Absoft C/C++ SDK for both Windows NT and Power Macintosh includes these common features:

- ANSI C, K&R C and C++ native compilers (PowerPC 601, PowerPC 603, PowerPC 604, and PowerPC 620 microprocessor compatible).
- Supports templates, exceptions and STL.
- Plum Hall validated.
- Designed for porting workstation code to the desktop.
- Excellent compiler diagnostics.
- SDK includes:
 - linker.
 - graphical debugger with browsers.
 - make.
 - application framework.
- No runtime royalties or fees.

In addition to the common features listed above, the Windows NT version includes:

- Direct support for full Win32 API, and can build DLLs.
- Automatically builds native Windows GUI for each compiled application.
- Fully source compatible with Absoft C/C++ SDK for Power Macintosh.

In addition to the common features listed above, the Power Macintosh version includes:

- Full Toolbox support.
- Automatically builds native Macintosh GUI for each compiled application.
- Link compatible with Absoft F77.
- Compatible with all MPW tools and languages.
- Includes two graphics libraries.

Software Generation and Debug Tools (Native)

Hosts Supported

- Absoft C/C++ for AIX: RS/6000™.
- Absoft C/C++ SDK:
 - PowerPC-based platforms running Windows NT.
 - Power Macintosh.

Availability

- Available now.

Contact

Absoft Corporation

Attn: Wood Lotz
2781 Bond Street
Rochester Hills, MI 48309
Tel: (810) 853-0050
Fax: (810) 853-0108
Web: <http://www.absoft.com>

Absoft FORTRAN 77 for AIX®, Windows NT™ and Power Macintosh™

Compilers, Debuggers, Utilities

Absoft Corporation

Absoft Corporation offers a variety of FORTRAN development tools including the Absoft FORTRAN 77 for AIX compiler/debugger and the Absoft FORTRAN Software Development Kit (SDK) for Windows NT or Power Macintosh.

Absoft FORTRAN 77 for AIX

Absoft FORTRAN 77 for AIX is a VAX/VMS globally optimizing compiler (PowerPC 601, PowerPC 603, PowerPC 604, and PowerPC 620 microprocessor compatible) validated under ANSI X3.9 with MIL-STD 1753 extensions. The compiler supports Cray POINTER, a variety of Sun, HP, and IBM extensions, and includes VAX/VMS and UNIX subroutine libraries. F77 is link-compatible with Absoft C/C++.

The Absoft Fx, a screen oriented, multi-language (F77, C, C++, assembly), source-level debugger for AIX or Motif is also included. You can display program variables in a variety of formats, modify variables while debugging and display multiple program elements with a single command. Arrays can be indexed with expressions, and interactive source and symbol browsers provide fast access to functions and data. Breakpoints, variable monitors, and single-stepping at both the source and instruction level provide complete control over program execution. Fx provides support for the full syntax of the FORTRAN language.

Absoft FORTRAN 77 SDK

The Absoft F77 Software Development Kit (SDK) for both Windows NT and Power Macintosh includes these common features:

- ANSI 77.
- MIL-STD 1753.
- VAX/VMS compatible compiler (PowerPC 601, PowerPC 603, PowerPC 604, and PowerPC 620 microprocessor compatible).
- Supports Cray POINTER, HP, and Sun extensions.
- SDK includes:
 - linker.
 - graphical debugger.
 - make.
 - application framework (written in FORTRAN—source included).
 - VAX/VMS and UNIX subroutine libraries and several utilities.
- No runtime royalties or fees.

In addition to the common features listed above, the Power Macintosh version includes:

- Full Toolbox support.
- Automatically builds native Macintosh GUI for each compiled application.
- Link compatible with Absoft C/C++, Metrowerks C/C++, Apple C/C++.
- Compatible with all MPW tools and languages.
- Includes two graphics libraries.
- Includes latest version of MPW.
- 450+ pages of illustrated documentation with examples.
- Applications can be retargeted, complete with GUI, to Windows 95 or Windows NT on an Intel platform, or to Windows NT on a PowerPC platform via a simple recompile.

Software Generation and Debug Tools (Native)

In addition to the common features listed above, the Windows NT version includes:

- Direct support for full Win32 API, and can build DLLs in FORTRAN.
- Automatically builds native Windows GUI for each compiled application.
- Link compatible with Microsoft C/C++.
- 450+ pages of illustrated documentation with examples.
- Fully source compatible with Absoft F77 SDK for Windows 95, Windows NT, and Power Macintosh.
- Applications can be retargeted, complete with GUI, to Windows 95 or Windows NT on an Intel platform, or to Macintosh via a simple recompile.

Hosts Supported

- Absoft FORTRAN 77 for AIX: RS/6000.
- Absoft FORTRAN 77 SDK:
 - PowerPC-based platforms running Windows NT.
 - Power Macintosh.

Availability

- Available now.

Contact

Absoft Corporation

Attn: Wood Lotz
2781 Bond Street
Rochester Hills, MI 48309
Tel: (810) 853-0050
Fax: (810) 853-0108
Web: <http://www.absoft.com>

IMSL Math and Stat Libraries v3.0

Libraries

Absoft Corporation

Absoft Corporation is the licensed distributor of IMSL F77 Math and Stat Libraries for Power Macintosh and Windows NT/PowerPC systems.

Absoft is distributing the latest version (v3.0) of IMSL's Mathematical and Statistical (including Special Functions) libraries. This is the full mainframe version, not a sub-set. Fully validated as native applications on Windows NT/PowerPC or Power Macintosh, these libraries consist of 900+ highly-optimized, well-test special function routines. The IMSL libraries require the Absoft F77 compiler.

Software Generation and Debug Tools (Native)

Availability

- Available now.

Contact

Absoft Corporation

Attn: Wood Lotz
2781 Bond Street
Rochester Hills, MI 48309
Tel: (810) 853-0050
Fax: (810) 853-0108
Web: <http://www.absoft.com>

LS FORTRAN and LS Object Pascal

Compiler

Fortner Research LLC

Fortner Research LLC offers two compilers for Power Macintosh computers, LS FORTRAN and LS Object Pascal.

The LS FORTRAN compiler is source-code compatible with Fortner Research's LS FORTRAN compiler for the Macintosh. Supporting a 32-bit clean programming model, it compiles existing FORTRAN 77 source code into native code for the Power Macintosh microprocessor. Expect a dramatic increase in compile speed and execution speed for large programs on the Power Macintosh.

Also available for use on the Power Macintosh is LS Object Pascal, which is fully compatible with Apple's MPW 3.3 Pascal for Macintosh. LS Object Pascal compiles existing Macintosh applications into native code for the Power Macintosh microprocessor. Supports all operating system traps and calls associated with Macintosh System 7.1. Performs global optimizations, profiling, and advanced source code diagnostics.

LS FORTRAN Features

- ANSI FORTRAN 77
- Native PowerPC compiler
- Background execution
- VAX, Cray, Data General, and Microsoft PC extensions
- MPW support
- Supports C and Pascal function calls and sharing of global data
- Built-in debugging
- Free runtime license

LS Object Pascal Features

- Support for integer, longint, char, Boolean, real, single, double, extended, comp, enumerated, subrange, and string data types.
- Unlimited code or data sizes.
- Support for cycle, leave, exit, and type coercion.
- Bit-manipulation routines included.
- Complete access to the Macintosh Toolbox.
- 100% compatible with MPW Object Pascal.
- Built-in source code debugger.

Software Generation and Debug Tools (Native)

System Requirements

- Macintosh or Power Macintosh.
- CD-ROM drive.
- For LS FORTRAN:
 - 5 MB memory partition.
 - 15 MB hard drive space.
- For LS Pascal:
 - 3 MB memory partition.
 - 10 MB hard drive space.

Technical Support

- Free technical support via telephone and electronic services.

Availability

- LS FORTRAN version 1.1 available now.
- LS Object Pascal version 1.0 available now.

Contact

Fortner Research LLC

100 Carpenter Drive
Sterling, VA 20164
Tel: (800) 252-6479
Tel: (703) 478-0181
Fax: (703) 689-9593
Email: info@fortner.com

NightView™ Source-Level Debugger

Debugger, Real-Time Tool

Harris Computer Systems Corporation

NightView is a graphical, non-intrusive, source-level monitoring and debugging tool specifically designed for real-time applications. NightView is part of the Harris Computer Systems Corporation (HCSC) NightStar™ software development environment. NightView is available on the Night Hawk® family of high-performance computers, the Power Hawk™ 610 entry-level computer, and other platforms based on the PowerPC 604 microprocessor running HCSC's PowerUX™ operating system. The NightStar environment enables system builders to reduce software development time and increase productivity when developing real-time applications on these systems.

Designed for Real-Time

HCSC recognizes that many real-time customers require tools for debugging sophisticated systems of different programs executing across multiple processors—not just single-stream applications. Environments such as flight simulation, vehicle and weapons testing, energy management, data acquisition and process control require interaction between multiple programs across multiple processors. The ability to monitor and manipulate programs as a group is critical in these environments.

NightView allows the user to monitor, manipulate and simultaneously debug a group of programs running on multiple PowerPC 604 processors in a Night Hawk multiprocessing environment, with virtually no overhead.

Monitorpoints and agentpoints provide access to program state without interrupting or stopping execution.

Context-Sensitive Debugging

NightView makes it possible to debug applications written in different languages concurrently. All variables and expressions in each program are referenced in the appropriate language. For example, customers can monitor and debug multiple applications written in any combination of FORTRAN, C, and Ada.

Monitorpoints

Monitorpoints display expression values at selected points of execution. Each time the program executes through the monitorpoint, the values of the specified expressions are saved in shared memory. NightView then periodically reads the data and displays the values on the screen.

Agentpoints

Agentpoints allow the programmer to manipulate a process while it is running. By controlling where agentpoints are placed, the programmer can restrict debugger overhead to the places where it is best for the program.

Flexibility

NightView users can write custom debugger commands, including command parameters, to meet their unique requirements. Users can

Software Generation and Debug Tools (Native)

make temporary changes to the program and can test the changes without having to recompile.

NightStar Integration

NightView is designed to work with other tools in the NightStar environment. NightView can be used to set "tracepoints" in a program at execution time, rather than embedding them in the source code. NightTrace™, another NightStar tool, can then be used to view the trace data.

Graphical Display

NightView supports a graphical user interface (GUI) based on OSF/Motif™ and the X Window System™ standards, which helps users

visualize debugger and program concepts. A command-line interface to ASCII terminals is also available.

Extensive On-Line Help

The entire NightView manual is available on-line. Help messages explain error messages and are cross-referenced to related commands. Help is available in the window interface simply by clicking the mouse on the relevant area of a window.

Processors Supported

- PowerPC 604 microprocessor.

System Requirements

- PowerUX operating system.

Contact

Harris Computer Systems Corporation

Real-Time Systems Division
2101 W. Cypress Creek Road
Ft. Lauderdale, FL 33309
Tel: (800) 666-4544 ext. 5469
Tel: (954) 973-5469
Email: nhnews@mail.hcsc.com
Web: <http://www.hcsc.com>

NightTrace™ Analyzer

Analyzer, Real-Time Tool

Harris Computer Systems Corporation

NightTrace is a graphical tool for analyzing the dynamic behavior of multiprocess and/or multiprocessor applications. NightTrace is tailored to the complex needs of real-time developers and can graphically display the interplay between many real-time programs and processes across multiple computer processors.

NightTrace is part of the Harris Computer Systems Corporation (HCSC) NightStar™ software development environment for the Night Hawk family of high-performance computers and other platforms based on the PowerPC 604 microprocessor running HCSC's PowerUX™ operating system. The NightStar environment enables systems builders to reduce software development time and increase productivity when developing real-time applications on Night Hawk systems.

Designed for Real-Time

Real-time applications are typically very sophisticated and involve many programs across multiple processors working together as one unit. NightTrace is the first real-time software development tool of its kind to monitor and graphically display the interdependencies across multiple processes and/or processors.

Multiprocess-Multiprocessor

NightTrace can analyze multiple processes, simultaneously running on multiple PowerPC 604 processors. The NightTrace event logging mechanism then automatically combines the results into a single stream of logged data events.

Graphical and Interactive

Any desired events and states can be displayed graphically along a time line to clearly show the relative timing of different events and provide an overall picture of the running application. The entire sequence of application events can be replayed in slow motion. NightTrace can locate specific events and zoom in on them with a very fine degree of granularity for precise observation.

High Configurability

The graphical information NightTrace provides about each application is completely user-configurable. Any information may be displayed in several different formats. Configurations may be saved and later recalled, and several different configurations can be viewed at the same time.

Software Generation and Debug Tools (Native)

NightView Integration

NightTrace is designed to work with NightView™, another tool in the NightStar tool set. NightView can be used to set "tracepoints" (similar to breakpoints) in a program at execution time, rather than embedding them in the source code. NightTrace can then be used to analyze the information logged from these tracepoints.

Kernel Support

Event information such as interrupts, exceptions, context switches, system calls and device accesses can be combined with event information from user applications to form a clear and complete picture of the activities of the kernel at any point during the application's run.

Text Summaries

Information on a given event or state can be summarized to provide statistical performance information about user applications and the kernel itself. Summaries can be customized and configured in several ways to give insight into application performance and behavior patterns.

Processors Supported

- PowerPC 604 microprocessor.

System Requirements

- PowerUX operating system.

Availability

- Available now.

Contact

Harris Computer Systems Corporation

Real-Time Systems Division
2101 W. Cypress Creek Road
Ft. Lauderdale, FL 33309
Tel: (800) 666-4544 ext. 5469
Tel: (954) 973-5469
Email: nhnews@mail.hcsc.com
Web: <http://www.hcsc.com>

NightSim™ Application Scheduler

User Interface, Real-Time Tool

Harris Computer Systems Corporation

NightSim is a graphical tool for building and monitoring real-time applications that require scheduled process execution patterns. It provides a graphical user interface (GUI) to two of Harris Computer Systems Corporation (HCSC) facilities—the Frequency Based Scheduler (FBS) and the Performance Monitor.

The FBS is a high-resolution task scheduler that enables the user to run processes in cyclical patterns. NightSim allows users to easily configure sets of processes to run on an FBS and save the resulting configurations to be reused.

The Performance Monitor facility gathers CPU utilization data for the processes running on an FBS. NightSim provides a flexible way to access this performance data and display it in real time on the screen or save it to a file for later analysis.

NightSim is part of HCSC's NightStar™ software development environment. NightSim is available on the Night Hawk® family of high-performance computer systems, the Power Hawk™ 610 entry-level computer, and other platforms based on the PowerPC 604 microprocessor running HCSC's PowerUX™ operating system. The NightStar environment enables systems builders to reduce software development time and increase productivity when developing real-time applications on these systems.

Graphical User Interface

NightSim supports a GUI based on the X Window System™ standard, so it runs on any X Window System device. The interface is also OSF/Motif™ compliant, so it can be learned quickly by developers.

Interactive Control of the FBS

The NightSim GUI provides a powerful environment for working with the FBS interactively. The scheduler window shows all configuration parameters for the FBS and the processes it controls, as well as status information once the FBS is activated. Many of the parameters can be modified “on the fly,” while the application continues uninterrupted.

Multiple Windows and Configuration Files
NightSim allows multiple windows for working with different schedulers or alternate scheduler configurations. Configurations can be created and modified before activating an FBS, and can be saved and loaded from disk files. This allows rapid testing and comparison of different configurations

Simplified Hardware Interface

NightSim handles the interface to hardware such as real-time clocks so that users don't have to deal with the underlying operating system for scheduling operations.

Software Generation and Debug Tools (Native)

Extensive Performance Statistics

NightSim monitors up to 14 different performance statistics, such as minimum and maximum cycle-times, for each process. With these statistics, users can optimize CPU utilization, for example, by balancing the load across multiple processors.

Flexible Performance Monitoring Display

NightSim has several predefined sets of statistics, such as "Minimum Fields," which allow quick selection of a subset of the available performance data. In addition, NightSim allows the display to be fully customized. To highlight important data, users can define their own sets of statistics, select which processes to monitor and choose sort criteria for the ordering of the data.

Performance Monitoring

NightSim monitors performance for either interactive or deferred use. Interactive monitoring provides immediate feedback and control. Deferred monitoring saves performance data to disk for later analysis.

Processors Supported

- PowerPC 604 microprocessor.

System Requirements

- PowerUX operating system.

Availability

- Available now.

Contact

Harris Computer Systems Corporation

Real-Time Systems Division
2101 W. Cypress Creek Road
Ft. Lauderdale, FL 33309
Tel: (800) 666-4544 ext. 5469
Tel: (954) 973-5469
Email: nhnews@mail.hcsc.com
Web: <http://www.hcsc.com>

NightProbe™ Data Monitoring Tool

Debugger, Real-Time Tool

Harris Computer Systems Corporation

NightProbe is a graphical tool for real-time monitoring, altering, and recording of program data within one or more executing programs without significantly affecting the execution of those programs. It can be used in a development environment as a tool for debugging, or in a production environment to create a "control panel" for program input and output.

NightProbe is part of Harris Computer Systems Corporation (HCSC) NightStar™ software development environment. NightSim is available on the Night Hawk® family of high performance computer systems, the Power Hawk™ 610 entry-level computer, and other platforms based on the PowerPC 604 microprocessor running HCSC's PowerUX™ operating system. The NightStar environment enables systems builders to reduce software development time and increase productivity when developing real-time applications on these systems.

Because NightProbe is separate from the program being monitored, it can be run on a different PowerPC 604 processor (running under the same PowerUX operating system) from the target program. This minimizes NightProbe's impact on the target program's performance. It also allows NightProbe to be used on a wide range of programs and applications.

Real-Time Sampling of Program Data

NightProbe samples the program data in real time. Because NightProbe is fast and non-intrusive, using NightProbe to debug a program will not interfere with the behavior of the program. NightProbe can be used to record data in a form that can be graphed and analyzed by NightTrace™, another NightStar tool.

Program Data Modified During Execution

NightProbe has the ability to write to the program address space, so the values of the variables can be changed or modified during execution. Developers can create prototypes by substituting values for components that have not yet been implemented. Developers also can create control panels to monitor and control programs in production systems.

Flexible Spreadsheet Display

A spreadsheet display window provides a flexible mechanism for displaying data in whatever organization the application requires. It is also the interface for modifying data values.

Non-Intrusive Performance

Because NightProbe accesses the address space of executing programs, no modifications or recompilation of source code are necessary. This also means NightProbe can be used in a production environment where source code is unavailable.

Symbol Table Browser

NightProbe locates data by browsing the symbol table in the executables. It then lists all the static variables in the program and allows developers to select variables of interest using a Motif™-style interface. Developers do not need to type in the names of variables or even know ahead of time what they are.

NightProbe supports scalar and structured data types in Ada, C, and FORTRAN. It works with both ELF and COFF object file formats which allows it to be used with a wide variety of programs.

Software Generation and Debug Tools (Native)

Graphical User Interface

NightProbe supports a graphical user interface (GUI) based on the X Window System™ standard and is OSF/Motif™ compliant. NightProbe runs on any X Window System device and can be learned quickly by developers familiar with NightStar tools or the Motif interface.

Processors Supported

- PowerPC 604 microprocessor.

System Requirements

PowerUX operating system.

Availability

- Available now.

Contact

Harris Computer Systems Corporation

Real-Time Systems Division
2101 W. Cypress Creek Road
Ft. Lauderdale, FL 33309
Tel: (800) 666-4544 ext. 5469
Tel: (954) 973-5469
Email: nhnews@mail.hcsc.com
Web: <http://www.hcsc.com>

IBM POWERbench™ and AIX® SDE WorkBench/6000 Version 2

Debugger, Utilities

IBM Corporation

IBM's POWERbench and AIX Software Development Environment (SDE) WorkBench/6000 Version 2 provide a comprehensive programming environment for C, C++, FORTRAN or COBOL developers for the construction, test and maintenance phases of software development. With the participation of third-party vendor tools already integrated with the POWERbench, it provides an integrated development environment covering the entire life cycle of software development. The SDE includes a set of integrated productivity programming tools such as: editor, debugger, program builder, static analyzer, development manager, tool manager, integrated file transfer, mail, help, and configuration management and version control support.

Three POWERbench products are available:

- The C++ POWERbench Version 2 is an integrated package of the SDE WorkBench/6000 Version 2 with the C Set ++/6000 Version 2.
- The FORTRAN POWERbench Version 1 is an integrated package of the SDE WorkBench/6000 Version 2 with the XL FORTRAN Compiler/6000 Version 3.
- The COBOL POWERbench Version 1 is an integrated package of the SDE WorkBench/6000 Version 2 with Micro Focus COBOL Version 3.1 for AIX, Micro Focus Toolbox Version 3.1 for AIX, and optional Micro Focus Dialog System Version 2.2 for Motif (1).

SDE WorkBench/6000 Version 2

The basic component of the POWERbench is the SDE WorkBench/6000 Version 2 that provides every POWERbench with a UNIX LAN-

based distributed integration framework and a set of the following productivity development tools common across multiple languages:

- The LAN-based distributed integration framework enables developers to perform the following functions:
 - Access and use files across the network.
 - Utilize CPU facilities on the network. Another computer's resources can run part or all of POWERbench.
 - Distribute communication. Different integrated tools can run on different computers across the network, and they communicate transparently.
 - Distribute the display. A tool's user interface can be supported on a remote system.
 - Coordinate the efforts of several software developers working on a single project.
 - Integrate existing or new tools into the development environment using SDE Integrator/6000 Version 2.
- An integrated set of basic tools most frequently used during software development:
 - Program Editor supports three editor choices: vi, GNU Emacs (not shipped with the AIX operating system) or SoftLPEX. SoftLPEX is a multi-color, syntax-directed editor supporting C, C++, FORTRAN and COBOL.
 - Program Builder helps create and execute necessary Make files. It maintains and displays compile errors enabling developers to navigate through and correct them.
 - Program Debugger features an integrated GUI to the dbx debugger on AIX.

Software Generation and Debug Tools (Native)

- Static Analyzer features the ability to automatically find information, such as uses and definition of function calls, and references to local and global variables.
- Development Manager gives the developer a file-oriented view that enables quick and easy location of files.
- Configuration Management tool support for the Source Code Control System (SCCS) component of AIX and the Revision Control System (RCS) Version 5 Release 5 available from various external sources. The IBM Configuration Management Version Control (CMVC) Client/6000 Version 1 (5765-069) and IBM CMVC/6000 Version 2 (5765-207) have integration support for each POWERbench to provide integrated change control and tracking capabilities.
- Tool Manager provides control and customization of all integrated tools such as removal or registration of tools.
- Integrated Mail provides a graphical interface to the AIX mail facility, and enables other integrated tools to utilize mail for team notification and communication.
- Integrated File Transfer Protocol (FTP) provides a graphical interface to the TCP/IP FTP and enables other integrated tools to invoke the services of FTP.

SDE Integrator/6000 Version 2

The SDE Integrator/6000 Version 2 is a companion product used to integrate additional or existing tools that enable developers to utilize SDE WorkBench/6000 services. Version 2 comes with the following enhancements:

- Compatibility with HP Encapsulator Ver. 3.0.
- Simplified Use Model: message, subprocess and terminal object.
- CIClient supports UNIX shell interface
- Computer Based Training on tools integration.

Machine and Programming Requirements

Requires a RISC System/6000 POWERstation or POWERserver configured with at least one supported display with keyboard.

- AIX Version 3.2 for RISC System/6000 (5756-030) with additional fixes from AIX Version 3.2.5 for RISC System/6000.
- IBM AIXwindows Environment/6000 Version 1 Release 2 (5601-257).

Ordering Information

- C++ POWERbench Ver. 2 (5696-733)
- FORTRAN POWERbench Ver. 1 (5696-551)
- COBOL POWERbench Ver. 1 (5696-761)
- SDE WorkBench/6000 Ver. 2 (5696-524)
- SDE Integrator/6000 Ver. 2 (5696-523)

Availability

- Available now.

Contact

IBM Corporation

To order, contact IBM Direct:
Tel: (800) IBM-4YOU
Email: askibm@info.ibm.com
Web: <http://ibm-direct.e-com.ibm.com>

For licensing information, contact:
IBM RISC System/6000 Division
AIX OEM & Licensing/MS 9581
11400 Burnet Road
Austin, TX 78758
Tel: (512) 838-4075
Fax: (512) 838-3461

XL Fortran for AIX® Version 3

Compiler

IBM Corporation

XL Fortran for AIX Version 3 Release 2 supports profile-directed feedback, which allows the optimizer to better understand program behavior before actually attempting to optimize it. The feedback functions results in better program execution performance. In addition, the compiler generates code that fully exploits the RS/6000 family of processors (including POWER, POWER2, and PowerPC platforms) and generates common code that runs on all RS/6000 processors.

The introduction of the AIX 4.1 operating system makes it possible to increase disk I/O performance with a disk stripping technique. Scratch files over 2GB can be created and accessed with proper setup of the logical volume manager.

Implicit connected files can now be customized through the use of an environment variable.

The improved GUI-based debugger, xldb, provides machine-level and source-level debugging, which allows sophisticated programmers to analyze programs at the system level. In addition, debugged objects with full path name can be generated to make debugging Fortran programs on AIX easier and more efficient.

IBM XL Fortran for AIX Version 3 Release 2 runs on AIX versions 3.2.5 and AIX Version 4.1 operating systems. Some new features available on AIX 4.1 can be fully exploited:

- Ability to de-install.
- New linker and loader.

XL Fortran for AIX conforms to the following standards:

- Fortran 90 (ISO/IEC 1539-1991 (E) and ANSI X3.198-1992).
- ANSI X3.9-1978 (Full ANSI FORTRAN 77).

- ISO 1539-1980 (E), programming languages, Fortran.
- FIPS PUB 69-1.
- ANSI/IEEE Standard 754-1985 for binary floating point arithmetic.
- SAA® Fortran CPI.

Fortran 90

XL Fortran is a full implementation of the new ISO and ANSI Fortran 90 standard. It is a modernization of the FORTRAN language with many new functions. Fortran 90 is also a superset of the F77 standard thus preserving investment in F77 FORTRAN code. The Fortran 90 language standard provides you with a broad range of powerful features. Scientific and engineering application programmers, in particular, will find that these features may enhance their code and improve run-time performance.

The powerful new functionality of Fortran 90 includes:

- Pointers.
- CASE construct.
- Named DO and IF constructs.
- EXIT and CYCLE statements for DO constructs.
- Free form source.
- Attribute specification in type declaration statements.
- Optional and keyword arguments.
- Intent of dummy arguments.
- Interface blocks.
- Internal procedures.
- Recursive procedures.
- Defined assignment and defined operators.
- Non-advancing input/output.
- New intrinsic procedures.

Software Generation and Debug Tools (Native)

Language Extensions

XL Fortran gives you functionality beyond the implemented standards, thus reducing the effort and cost of porting Fortran code. These language extensions include:

- 64-bit integers and logicals.
- INTSIZE and REALSIZE compiler options to set default sizes of data types.
- Additional intrinsic functions such as the Cray conditional vector merge functions.

The key Fortran 90 features include:

- Array Operations
- Derived Types
- Dynamic Memory Allocation
- Modules

Optimization

The XL Fortran compiler includes an optimizing back end that is also used by other members of the XL family of languages. These optimization techniques will enable faster execution of applications written with XL Fortran. Compiler optimization techniques include:

- Instruction scheduling
- Common expression elimination
- Strength reduction
- Code motion
- Inlining
- Value numbering
- Straightening
- Reassociation
- Constant propagation

- Global register allocation
- Dead code elimination
- Store motion
- Interprocedural analysis
- High order loop transformations
- Scheduling tuning

Machine and Programming Requirements

Requires a RISC System/6000 or other system supported by AIX configured with at least one supported display and keyboard or one ASCII terminal. The following is also required:

- Minimum of 16 MB of RAM (64 MB recommended).
- 14 MB of DASD for the Licensed Program Materials.

This product will exploit all available RISC System/6000 hardware architectures, including PowerPC platforms. These licensed programs require AIX Version 3.2.5 for RISC System/6000 (5756-030) or AIX Version 4.1 (5765-393).

Ordering Information

- AIX XL Fortran Compiler/6000 Version 3 Release 2 (5765-176).

Note: The AIX XL FORTRAN Compiler/6000 Version 3 Release 2 licensed program includes the run-time component.

Availability

- Available now.

Contact

IBM Corporation

To order, contact IBM Direct:
Tel: (800) IBM-4YOU
Email: askibm@info.ibm.com
Web: <http://ibm-direct.e-com.ibm.com>

For licensing information, contact:
IBM RISC System/6000 Division
AIX OEM & Licensing/MS 9581
11400 Burnet Road
Austin, TX 78758
Tel: (512) 838-4075
Fax: (512) 838-3461

AIX® XL Pascal Compiler/6000 Version 2

Compiler

IBM Corporation

AIX XL Pascal Compiler/6000 Version 2 offers a productive application development environment that allows for the development and execution of applications for the new IBM RISC System/6000(00) family of POWERstations and POWERservers. This product will exploit all available RISC System/6000 hardware architectures, including PowerPC. The AIX XL Pascal Run-Time Environment/6000 program supports the execution of applications developed with the compiler.

These products adhere to industry standards and are intended to protect a customer's application development investment by facilitating the portability of applications across systems.

Features and Benefits

The AIX XL Pascal Compiler/6000 is an optimizing compiler that executes under AIX Version 3.2.5 for RISC System/6000. If no optimization is requested, compilation is faster. When optimization is requested, the compiler produces optimized object code by performing a variety of optimizations upon the program, which may include:

- Flow of control optimization, such as:
 - Elimination of unreachable code.
 - Straightening.
 - Elimination of unnecessary branches.
- Value Numbering.
- Reassociation (subscript optimization in loops).

- Dead code elimination (i.e. removal of code that computes unused results).
- Common subexpression elimination.
- Constant folding.
- Code motion for loop invariants.
- Strength reduction.
- Elimination of induction variables.
- Elimination of redundant load/store sequences.
- Store motion (moving stores out of loops).
- Global register allocation.
- Instruction scheduling.
- Exploitation of machine idioms.

The AIX XL Pascal Run-Time Environment/6000 library routines include support for the following types of functions that may be invoked by an AIX XL Pascal Compiler/6000 program:

- Text file data transformations between the character form found in text files and the internal data formats.
- Data file access and support functions.
- String manipulation functions.

Standards Conformance

The AIX XL Pascal Compiler/6000 aids migration and co-existence by conforming with various Pascal standards, including:

- ANSI/IEEE 770x3.97-1983, American National Standard Pascal Computer Programming Language.
- ISO 7185-1983, Computer Programming Language Pascal—Level 0.

Software Generation and Debug Tools (Native)

Machine Requirements

The AIX XL Pascal Compiler/6000 is designed to execute on the RISC System/6000 POWERstations and POWERservers configured with at least one supported display and keyboard, or one ASCII terminal. The minimum hardware requirements for AIX XL Pascal Compiler/6000 are:

- RISC System/6000 with a minimum of 8 MB of memory.
- 3.16 MB of fixed-disk storage for program files.

Add 5MB of fixed-disk storage if online documentation for AIX XL Pascal Compiler/6000 is to be installed.

Programming Requirements

- AIX for RISC System/6000 Version 3.2.5 on the RISC System/6000.

Ordering Information

- AIX XL Pascal Compiler/6000 Version 2 (5765-245).

Availability

- Available now.

Contact

IBM Corporation

To order, contact IBM Direct:
Tel: (800) IBM-4YOU
Email: askibm@info.ibm.com
Web: <http://ibm-direct.e-com.ibm.com>

For licensing information, contact:
IBM RISC System/6000 Division

AIX OEM & Licensing/MS 9581
11400 Burnet Road
Austin, TX 78758
Tel: (512) 838-4075
Fax: (512) 838-3461

The Debugger V2 and MacNosy

Debugger, Disassembler

Jasik Designs

The Debugger is a low- and high-level symbolic debugger that runs in a multi-window Macintosh environment. You can trace program execution and view the values of variables for both 680x0 and PowerPC Macintosh programs. MacNosy is a global interactive disassembler that enables recovery of the source code of any Macintosh application, resource file or the ROM. The Debugger is used at Adobe, Aldus, Claris, Electronic Arts, Kodak, Metrowerks, and many others.

Features

- Symbolic debugging of any Macintosh program, ROM, or code resource (DRVRs, XCMDs, INITs, PDEFs, 4DEXs, etc.).
- Source-level debugging for Metrowerks and MPW compiled programs (C++, C, Pascal, Fortran), and an incremental build system with instant link for superfast development.
- Object inspector for MacApp 3 programs.
- Source-level debugging of THINK C™ projects.
- Includes a program (CoverTest) to interactively do code coverage analysis for SQA testing, etc.
- Simultaneous symbolic debugging of multiple tasks.
- Fast *software watchpoint* command to find clobbered variables.
- Sophisticated error checking algorithms such as *trap discipline* (argument checking), *handle zapping*, *heap* *scramble*, and *heap check* to detect program errors before they become disasters.
- Structured display of data (hypertext) with user-definable structures while debugging.
- Conditional breakpoints to help filter out redundant information.
- Continuous Animated Step Mode to watch your program execute instruction-by-instruction.
- Detailed symbolic disassembly for both 680x0 and PowerPC with symbol names, labels, cross reference maps, etc. make it possible to ferret out the secrets of the ROM, etc.
- "Training Wheels" for the PowerPC disassembler to help you learn the opcodes.

Software Generation and Debug Tools (Native)

Hosts Supported

- Any Macintosh computer with at least 4 MB of RAM, a hard disk, and System 6.0.3 or later.

Availability

- Available now.

Contact

Jasik Designs

Attn: Steve Jasik
343 Trenton Way
Menlo Park, CA 94025
Tel: (415) 322-1386
Email: macnosy@netcom.com
Web: <http://www.jasik.com/>

Metrowerks CodeWarrior®

Compiler, Debugger, Libraries, Utilities

Metrowerks®

CodeWarrior is the universal development environment of choice on the Mac OS™. Use CodeWarrior to build applications for the Mac OS, Windows 95®, Windows NT™, Magic Cap™, and the new Be™ OS. The CodeWarrior development package includes C, C++, Object Pascal and Java compilers, source-level debuggers, object-oriented frameworks, complete online documentation and source-code examples for all languages and platforms.

CodeWarrior's fast compilers not only speed application development, they also produce fast, highly optimized code. CodeWarrior's IDE (Integrated Development Environment) brings the CodeWarrior tools together in one intuitive, easy-to-use interface.

CodeWarrior simplifies every step of application development. CodeWarrior's context-sensitive editor helps you easily write, read, and understand your code. CodeWarrior's project manager completely automates the process of compiling and linking your applications, and CodeWarrior's source-level debuggers allow you to quickly find and correct your mistakes. With CodeWarrior, you will be able to write, build, and debug your applications faster and easier than ever before.

Metrowerks' object-oriented application framework, PowerPlant™, provides a solid foundation for Mac OS applications. PowerPlant Constructor™ lets you visually design the interface for your application, and the PowerPlant Library provides prefabricated classes that let you easily take advantage of the advanced features of the Mac OS. Use

PowerPlant to get your application up and running with a minimal amount of coding on your part.

Choose from a wide range of third-party development tools located on the CodeWarrior Tools CD. CodeWarrior includes Apple Computer's MPW® and MacApp® providing additional flexibility for Macintosh development. For Windows development, the Tools CD includes the Microsoft Foundation Classes.

CodeWarrior's advanced features have made it the leading development package used by both Macintosh® professionals and university students today. CodeWarrior is more than an intuitive interface, stable compilers and code optimizing tools. CodeWarrior is a complete package for single platform and multi-platform development.

CodeWarrior has three major releases each year with registered users receiving two free updates. Check out Metrowerks Worldwide at <http://www.metrowerks.com> for the latest product information.

Features

- Integrated Class Browser.
- Editor support includes color-syntax highlighting and split views.
- Support for OpenDoc development.
- Metrowerks CodeWarrior Development Environment software has been localized for the French, German, Kanji, Spanish, Brazilian Portuguese, Simplified and Traditional Chinese, and Hangul language markets. All language versions of the software except Kanji (sold separately) are

Software Generation and Debug Tools (Native)

included in the English language version of CodeWarrior. Special regional editions of CodeWarrior are available with translated, hard copy editions of the 70-page Quick Start Guide.

- CodeWarrior's C Compiler is fully ANSI compliant. The C++ compiler closely tracks the emerging ANSI C++ standard and is consistent across 68K and PowerPC machines. C++ supports multiple inheritance, templates, zero-overhead exception handling, and RTTI. Metrowerks' Pascal is an MPW Object Compatible compiler with built-in run-time library routines providing ANS compatibility. Metrowerks Pascal supports the original MacApp framework written in Pascal and modified for use with PowerPC (MacApp2PPC.)
- CodeWarrior comes with over 5,000 pages of online documentation including language user guides, system notes, library reference material, and step-by-step tutorials. Hard copy versions of *Inside CodeWarrior* and *Inside PowerPlant* reference books available separately.

- Register your product and receive excellent technical support via email, WWW, online services, phone or fax.
- Registration also gives you two additional product updates. CodeWarrior has three updates per year scheduled in January, May, and September.

System Requirements

- PowerPC 601 processor or higher.
- 8 MB of RAM (20 MB for Magic Cap development).
- System 7.1.2 or later (for Power Macintosh™).
- CD-ROM drive installation.

Availability

- Available now.

Contact

Metrowerks

MCC Building
3925 W. Braker Lane, Suite 310
Austin, TX 78759
Sales: (800) 377-5416
Voice: (512) 305-0400
Fax: (512) 305-0440
Email: sales@metrowerks.com
Web: <http://www.metrowerks.com>

CodeManager™

Utilities

Metrowerks®

Metrowerks CodeManager is a Macintosh® source-code control system based on Microsoft Visual SourceSafe™. CodeManager not only works with source files but also with any type of binary file including graphic, database, library and executable files.

CodeManager is designed for use with software projects ranging in size from individual users to large, multi-platform teams. CodeManager's security features maintain file integrity while encouraging code reuse within and across project teams. No more duplication of existing code! Security levels can be set for each project and user, providing access to all those who need it, when they need it. Files are checked in and out easily along with comment areas to describe changes between versions. Additional security levels are available to program administrators in order to prevent accidental deletion of files.

Save on storage space with reverse delta versioning that keeps the latest file and just the changes between each previous version. CodeManager organizes files into a hierarchy of projects and sub-projects while keeping track of the relationships between files and projects. Files are stored once even if used by multiple project teams.

Project analysis and reporting tools simplify project management tasks leaving more time for development. CodeManager supports version tracking by date and time or label, activity reporting, and difference listings between files. Report histories are created quickly for easy analysis. Metrowerks CodeManager allows you to review file histories, revert to earlier versions, and develop projects concurrently.

Use ToolServer™ to access CodeManager from within Metrowerks CodeWarrior®'s Integrated Development Environment or with your alternative Macintosh environment. Registered users receive two free updates providing the latest features for a complete project management system. Check out Metrowerks Worldwide at <http://www.metrowerks.com> for the latest product information.

Features

- Compatible with Microsoft Visual SourceSafe 4.0.
- Reverse delta versioning reduces file storage requirements.
- Files are organized into projects and subprojects with CodeManager maintaining relationships between files and projects.
- Project analysis and reporting tools.
- Register your product and receive excellent technical support via email, WWW, online services, phone or fax.
- Registration also gives you two additional product updates providing the latest improvements to this exciting new product.

Software Generation and Debug Tools (Native)

System Requirements

- 1.5 MB RAM partition recommended.
- 5 MB hard drive space.
- System 7 or later.
- MPW® version 3.3 or later, or ToolServer 1.1.1 or later.
- Networking software required if using non-Macintosh client.
- CD-ROM drive.

Availability

- Available now.

Contact

Metrowerks

MCC Building
3925 W. Braker Lane, Suite 310
Austin, TX 78759
Sales: (800) 377-5416
Voice: (512) 305-0400
Fax: (512) 305-0440
Email: sales@metrowerks.com
Web: <http://www.metrowerks.com>

Motorola UNIX® SDK PowerPC Edition

Compiler, Debugger, Libraries, Utilities

Motorola, Inc.

Motorola's UNIX SDK PowerPC Edition provides a powerful set of software development tools designed to exploit the full performance potential of the PowerPC microprocessor family.

The SDK contains C/C++ and FORTRAN compilers which share a common core optimizer and yield world-class performance while strictly adhering to ABI standards. The compilers can be configured to produce moderately or aggressively optimized code which is highly portable. This combination of performance and portability reduces the time to market and offers a competitive edge in application performance.

The Motorola UNIX SDK delivers world-class code optimization for any specific PowerPC microprocessor, while ensuring compatibility across the entire PowerPC family of microprocessors. The compilers can be configured to create object code optimized for one particular microprocessor, or to create a series of objects that target multiple microprocessors.

Features

- Supports all major C and C++ language variants as well as FORTRAN 77.
- Assembly and XCOFF code generation.
- Integration with Motorola source-level PowerPC debugger.
- Global optimization:
 - Local and global common subexpression elimination.
 - Priority-based graph coloring register allocation.
 - Software pipelining.
 - Loop unrolling.
 - Constant and copy propagation.
 - Aggressive load/store removal.
 - Interprocedural analysis and optimization.
 - Function inlining capability.
 - Execution profile feedback mechanism.
- Customization:
 - Control variables and variable groups.
 - Different optimization levels.
 - Internal flags for controlling intermediate debugging trace generation.
 - Diagnostic messages (can be disabled).

Software Generation and Debug Tools (Native)

Contents

- Motorola C/C++ and FORTRAN compilers.
- Motorola Portable assembler (pas).
- Motorola linker (mld).
- Motorola source level debugger.
- Associated libraries.
- Complete set of printed documentation.

Devices Supported

- All 32-bit PowerPC microprocessors.

Hosts Supported

- IBM RS/6000 systems running AIX versions 3.2.X or 4.1.
- Sun4 systems running Sun OS v4.1.3 or higher.

Technical Support

Full-time technical staff provides support via voice, fax and Internet:

- ppcinfo@risc.sps.mot.com
- <http://www.mot.com/PowerPC/>
- 1-800-347-8384 voice

Availability

- Version 1.7 available now.

Contact

Motorola, Inc.

For additional information, call 1-800-347-8384 or
Tel: 512-891-2999
Fax: 512-891-3798
Email: ppcinfo@risc.sps.mot.com
Web: <http://www.mot.com/PowerPC/>

Ada Development Environment for AIX® Operating System

Compiler, Debugger, Libraries, Utilities

Thomson Software Products

Version 5.6 of the Ada Development Environment for the AIX operating system offers a complete production-quality Ada environment suitable for the development of demanding applications on IBM RS/6000 or PowerPC workstations. The environment consists of the compiler, high-level and low-level optimizers, binder, multi-library environment (family, library and unit managers), standard Ada packages, and ISO-standard mathematical library.

The compiler supports the Ada Developer's Toolset, which consists of AdaProbe, the source-level symbolic debugger and program viewer; AdaXref, a multi-unit cross-reference generator; AdaMake, an automatic recompilation utility; and AdaReformat, a source code reformatter.

Features

- *Reorganize Compiled Ada Code Swiftly and Securely*—Ada's potential for reusable software components is possible through library import/export. A library or set of libraries can be moved or copied in object code format without the need for source code recompilation while retaining the security of the multi-library mechanism.
- *Integrate Large Projects*—The library import/export mechanism combined with full consistency checks means Ada libraries can be shared across networks.
- *Maximize Run-Time Efficiency*—The Ada run-time executive supports preemptive scheduling, non-blocking input/output, automatic deallocation for each access type on scope exit, and optimal exception handling.
- *Enhance Programmer Productivity*—The whole environment can be used through a graphical user interface under Xwindows: AdaWorld for Motif. The development environment is integrated under Workbench.
- *Reduce the Correction Cycle*—Detailed messages precisely pinpoint syntax and semantic errors, providing explanations and suggested fixes. The high-level optimizer detects at compile time many cases of using uninitialized variables; it also detects many pending run-time constraint errors. Run-time errors generate a trace-back with complete calling sequence and source-line information. The fast binder speeds up program rebuilds, reducing the time spent in the compile-rebuild-debug cycle.
- *Use Low-Level Programming Features*—The compiler supports Chapter 13 features of the Ada Reference Manual, such as representation clauses to the bit level and interfaces to Assembler and C. Ada subprograms can be called from programs written in another language.
- *Generate High-Performance Floating-Point Instructions*—Full advantage is taken of all instructions in the RS/6000 or PowerPC floating-point hardware for high-speed floating-point applications. A mathematical library, conforming to the ISO standard, provides all elementary mathematical functions.
- *Debug and View Programs*—AdaProbe, the source-level debugger and viewer, takes full account of the characteristics of the Ada language, including generics and tasking, from the dynamic as well as the static point

Software Generation and Debug Tools (Native)

of view. AdaProbe gives the user full control over the execution of the program (containing Ada as well as non-Ada modules) by providing fundamental functions: break points, single-stepping, and halting when exceptions are raised. Objects (regardless of their complexity), register contents, and memory can be displayed and modified by pointing in the source code file.

- *Recompile Automatically*—AdaMake generates the minimum command file for an application build. AdaMake works with both source files and Ada libraries and retrieves the exact set of options used in previous compilations of any given unit.

Availability

- Version 5.6 available now.

Contact

Thomson Software Products

10251 Vista Sorrento Parkway
Suite 300
San Diego, CA 92121
Tel: (619) 457-2700
Fax: (619) 452-2117
Web: <http://www.thomsoft.com/prod-ucts/ada/Ada.html>

Domestic Sales Offices

California

Thomson Software Products
10251 Vista Sorrento Parkway
Suite 300
San Diego, CA 92121
Tel: (619) 457-2700
Fax: (619) 452-2117

Texas

Thomson Software Products
2777 Stemmons Freeway
Suite 1133
Dallas, TX 75207
Tel: (214) 630-4211
Fax: (214) 630-3766

Massachusetts

Thomson Software Products
200 Wheeler Road
6th Floor
Burlington, MA 01803
Tel: (617) 270-0030
Fax: (617) 270-6882

Virginia

Thomson Software Products
779 Leesburg Pike
Suite 900N
Falls Church, VA 22043
Tel: (703) 847-6787
Fax: (703) 847-2958

Worldwide Locations

France

Thomson Software Products
66-68 Avenue Pierre Bossollette
92240 Malakoff
Tel: (1) 41.48.10.0
Fax: (1) 41.48.10.20

United Kingdom

Thomson Software Products Ltd.
Patridge House
Newton Road
Henley-on-Thames
Oxon, RG9 1EN
Tel: (0491) 579090
Fax: (0491) 571866

Sweden

Thomson Software Products AB
Marinens Vag 30
S-136 40 Haninge
Tel: (08) 707 3060
Fax: (08) 707 3080

Germany

Thomson Software Products GMBH
Kleinoberfeld 7
D-76135 Karlsruhe
Tel: (72) 1-98653-0
Fax: (72) 1-98653-98

Japan

Thomson Software Products KKE
TechnoWave 100, 16F
1-1-25 Shin-Urashima-cho
Kanagawa-ku
Yokohama 221
Tel: (45) 451-2412
Fax: (45) 451-2419

Software Generation and Debug Tools (Cross)

NetROM™

Debugger, Emulator/Simulator, Utilities

Applied Microsystems Corporation

NetROM from Applied Microsystems Corporation is an ideal tool for the embedded system programmer. NetROM is a communications gateway combined with ROM emulation. This combination provides a development tool ideally suited to today's embedded systems environment. Most embedded development today is performed on workstations or PCs which are usually connected by Ethernet. NetROM fits seamlessly into this environment. NetROM makes all serial information from the target system available on the development host by channeling it over the Ethernet. In addition, code images may be quickly updated over the Ethernet.

This rich feature set provides a productivity enhancing environment to embedded system programmers. Development can now be performed entirely from the development station. No more chasing problems with serial cables. Expensive tools such as ICEs become unnecessary.

NetROM is ideally suited for use with the embedded PowerPC. Code images for this processor tend to be large and thus can take a

long time to download over slower serial links. Using NetROM can increase the speed of loading code images by a factor of 1000. This allows the embedded PowerPC programmer more time to focus on finding the bugs in their code, rather than waiting for files to move across serial lines.

The only requirement for adding NetROM to your current or planned PowerPC development environment is an Ethernet connection to your development workstation. While debuggers which support Ethernet communication (such as XRAY or GDB) provide the best solution for use with NetROM it is not a requirement.

NetROM works with any version of the PowerPC processor family, because it emulates ROMs, not the processor itself. Yet most of the features provided by a processor emulator are available with NetROM. Also since NetROM is processor independent, switching to a different version of the PowerPC, does not require purchasing a new development tool.

Software Generation and Debug Tools (Cross)

Features

- A complete Ethernet host implementation supporting Telnet, TFTP, RARP, bootp, ping, SLIP and SNMP.
- 1 Mega-byte of emulation memory which may be organized in 8-, 16-, or 32-bit words. Wider word sizes may be supported with multiple NetROM units.
- A target serial port for connecting to embedded target UARTs.
- A pair of virtual UARTs for communicating with targets without UARTs or for additional serial data paths for targets with their own UARTs.
- A multitasking kernel to allow multiple sessions between the host workstation and the target system.
- A powerful user interface for configuration and setup.
- A socket interface for communicating with NetROM from the workstation based debugger.
- Eight control outputs for generating signals such as Reset, NMI, etc. to the target.
- Eight status input signals for detecting target events.
- Support for target system writes to emulation space for inserting breakpoints and/or target to host communication.
- Batch file support for ease of programming and setup.
- Careful design techniques to guarantee correct operation in any target system.
- Integrated RISCWatch source level debugging tools.

Availability

- Available now.

Contact

Applied Microsystems Corporation

5020 148th Avenue NE
Redmond, WA 98052
Tel: (800) 426-3925
Tel: (206) 882-2000
Fax: (206) 883-3049
Email: info@amc.com
Web: <http://www.amc.com>

TotalView™

Debugger

BBN Systems and Technologies, Inc.

TotalView™ for PowerPC microprocessors is a powerful source-level, window-oriented, single and multiprocess debugger. TotalView allows you to manage and control multiple processes, even if those processes are distributed on multiple machines. TotalView's user interface is fast and easy to learn.

Features

- Fast, easy-to-use X Windows interface.
- On-line, context sensitive help.
- Debug C, C++ and FORTRAN source.
- Debug assembler and source/assembler.
- Lightweight debugger server designed for embedded systems.
- Automatically acquire new processes.
- Attach to existing processes.
- Debug multithreaded applications.
- Debug network distributed applications.

- Debug applications without stopping them.
- Flexible multiprocessor breakpoints.
- Flexible execution control.
- Flexible signal handling options.
- "Dive" into objects to obtain more detail.
- Supports many executable file formats, including XCOFF and ELF.

User Interface

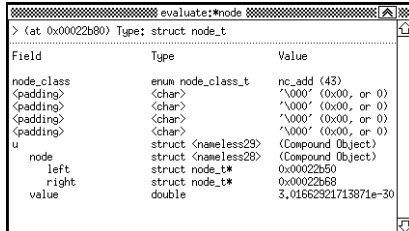
TotalView is fast and easy to use. It has a point-and-click user interface, on-line help, easy menus, requires no special make files, and imposes no restrictions on code or symbol table size.

TotalView shows you what you need to see. Just click on a variable and see the data or underlying structure; click on a function and see its source.

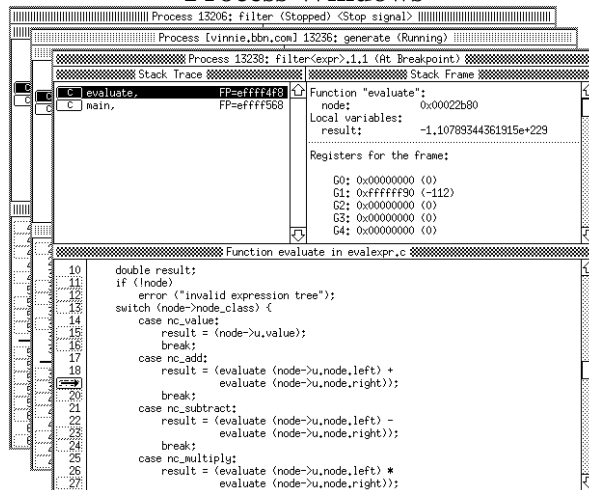
Root Window



Data Window



Process Windows



Software Generation and Debug Tools (Cross)

Remote Debugging

TotalView can debug processes which are running on remote systems. TotalView includes a debugger server which runs on a remote machine. The debugger server communicates with TotalView to give you full control over remote processes.

Multiprocess Debugging

TotalView debugs multiple processes simultaneously. It can automatically attach to newly created processes created by your program.

Multiprocessor Debugging

TotalView also simultaneously debugs multiple processes distributed over multiple processors.

Assembly Debugging

TotalView allows you to debug at the assembly level. You can see the machine instructions and registers. You can even view and debug machine instructions interleaved with your source code.

Asynchronous Debugging

TotalView runs asynchronously with your application. You can read your program's data without stopping your program.

Power Debug

Unleash the power of TotalView™ on your PowerPC embedded application!

Host Systems

- AIX on IBM RS/6000.
- AIX on PowerPC 601, 603, and 604 processors.
- Solaris 1.x and 2.x on SUN/SPARC.
- Digital UNIX on DEC Alpha/AXP.

Target Processors

- PowerPC 600 Series processors.

Other Target Processors

- AT&T DSP32C.
- DEC Alpha.
- Intel 80x86 and Pentium families.
- Intel i860 and i960.
- Motorola 68K and 88K families.
- SPARC.

Technical Support

- Telephone, email, fax.
- Full set of documentation.
- All manuals available in PostScript.

Availability

- Available now.

Contact

BBN Systems and Technologies, Inc.

c/o Marguerite Sinnett
TotalView Sales Department
10 Moulton Street
Cambridge, MA 02138 USA
Tel: (800) 856-3766
Fax: (617) 873-2685
Email: tv-sales@bbn.com

TimeScan™

Analyzer, Debugger

BBN Systems and Technologies, Inc.

TimeScan™ for PowerPC microprocessors is a performance analyzer software tool which gives insight into complex real-time applications.

TimeScan gives you a clear, easy-to-understand picture of how the different components of your software behave during execution.

Features

- Fast, easy-to-use Motif interface
- Variety of views and analyses for measuring performance and identifying problems
- User defined states
- On-line, context sensitive help
- Multi-process, heterogeneous

Event Log Library

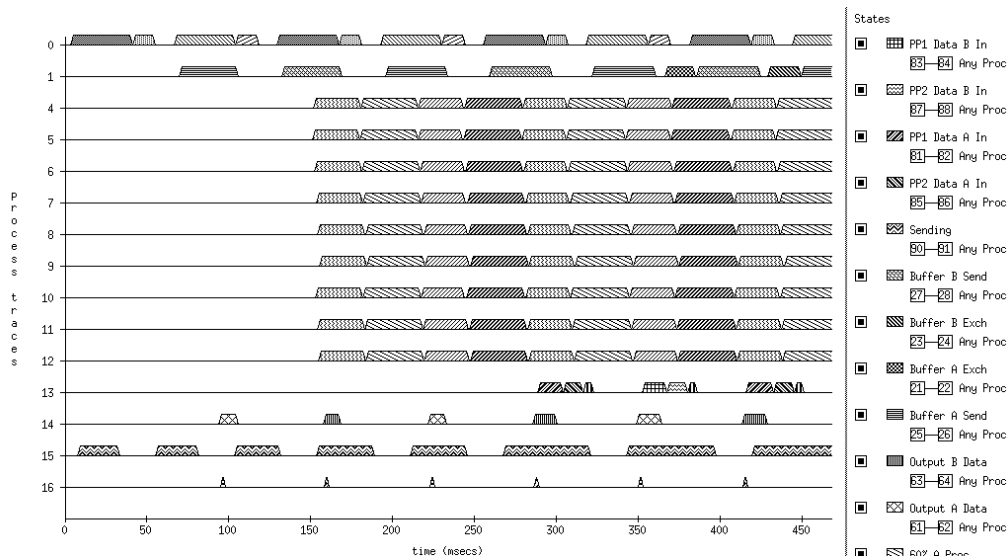
The Event Log Library is used to instrument your application and underlying software systems. It creates an event file which is passed

to the TimeScan Analysis Tool. The Event Log Library was designed to work with real-time applications. It is fast, flexible and highly portable. It can be used in multi-threaded, multi-process, multi-processor, heterogeneous and distributed applications. The Event Log Library has language bindings for C, C++ and FORTRAN applications.

TimeScan Analysis Tool

The TimeScan Analysis Tool creates clear, easy-to-understand pictures and statistics that are an invaluable aid in finding bugs and improving application performance.

TimeScan can integrate groups of trace files from multiple processors, including heterogeneous types of processors, giving you the complete picture of your application.



Software Generation and Debug Tools (Cross)

Event Oriented Display

TimeScan's event oriented display allows you to see the exact order of events in your application. Clicking on an event displays a detail box that shows you the optional data logged with that event.

State Oriented Display

TimeScan can display a state-oriented view of your application. States, defined by entry and exit events, provide a detailed view of the system in your own terms (see diagram).

Statistical Display

The value of the state oriented view is further enhanced by a variety of statistical displays and metrics. These are the tools you need to characterize overall system performance and to identify and focus in on specific performance problems.

Other Features

- Find difficult timing-related bugs such as race conditions and deadlocks.
- Locate hard-to-find performance problems.
- Verify that components of your application are executing within time limits.
- Locate rare or unusual events.
- Prepare diagrams which can be used for professional presentations.

Power Display

Unleash the power of TimeScan™ on your PowerPC embedded application!

Host Systems For Event Logging

- AIX on IBM RS/6000.
- AIX on PowerPC 601, 603 and 604 processors.
- Solaris 1.x and 2.x on SUN/SPARC.
- Digital UNIX on DEC Alpha/AXP.
- Other real-time platforms.
- Source license is available for custom applications.

Host Systems For TimeScan

- AIX on IBM RS/6000.
- AIX on PowerPC 601, 603 and 604 processors.
- Solaris 1.x and 2.x on SUN/SPARC.
- Digital UNIX on DEC Alpha/AXP.

Technical Support

- Telephone, email, fax.
- Full set of documentation.
- All manuals available in PostScript.

Availability

- Available now.

Contact

BBN Systems and Technologies, Inc.

c/o Marguerite Sinnett
TotalView Sales Department
10 Moulton Street
Cambridge, MA 02138 USA
Tel: (800) 856-3766
Fax: (617) 873-2685
Email: tv-sales@bbn.com

UDB

Debugger

CaseTools, Inc.

UDB is a universal source-code debugger for remote-target debugging of single- and multi-target embedded systems.

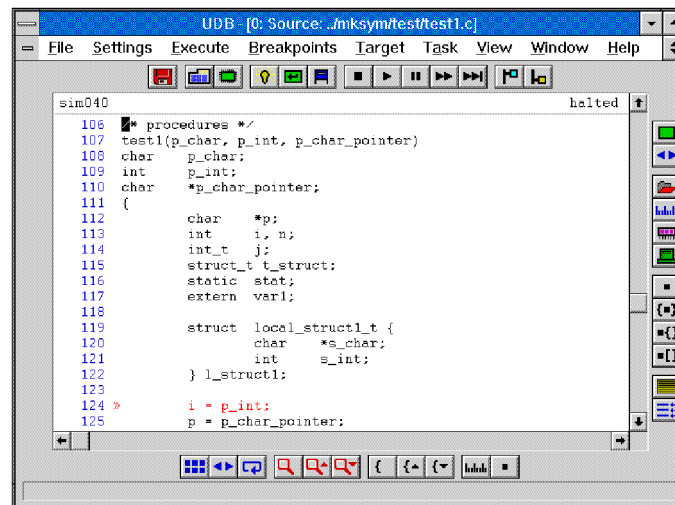
Features

- Source-level debugging.
- Assembly-level debugging.
- Multi-target and multi-tasking debugging.
- Runs on PC and UNIX based hosts.
- Runs under Windows 3.1 and Motif.
- Intuitive GUI-based user interface.
- User definable toolbars.
- Supports PowerPC, 68K, i386, i960, 29k, SPARC, MIPS and ARM processors.
- Compatible with most popular compilers and assemblers.
- Flexible host-to-target connectivity.

- Supports IBM target monitor and UMON.
- Compilers and Tools Supported for PowerPC development:
 - Diab Data
 - MetaWare
 - Microtec
 - Green Hills
 - GNU

Broad Support

UDB supports a wide range of processor architectures, supports most compiler toolsets, runs on multiple host platforms, and has a flexible I/O mechanism that allows the host and target to be connected via any desired communications link. Such capabilities assure the developer of being able to use the same debugger for future projects.



Software Generation and Debug Tools (Cross)

Tool Independence

The UDB debugger supports compilers from a wide range of vendors. Now you can use the compiler that best meets the project requirements, but maintain productivity.

Multi-Target

A larger percentage of today's projects involve multi-target hardware. UDB was designed from scratch to support both single and multi-target debugging. UDB allows each window of its multi-window GUI interface to be independently bound to a different target. As such, debugging a multi-target embedded system is just as easy as debugging a single-target embedded system.

GUI Interface

UDB has the look and feel of each native environment it supports. UDB is delivered as a true Windows application and a true Motif application. Interaction with UDB is through resizable windows, context-sensitive user programmable toolbars, menus and dialog boxes. There is no need to learn a command-line interface for interactive usage. Individual windows can display source code, disassembled code, memory, C variables, processor registers, files and log event messages.

Availability

- Available now.

Contact

CaseTools, Inc.
430 Semple Court
Aptos, CA 95003
Tel: (408) 685-0336
Fax: (408) 685-0312

PowerEM Emulators

Emulators/Simulators

Corelis

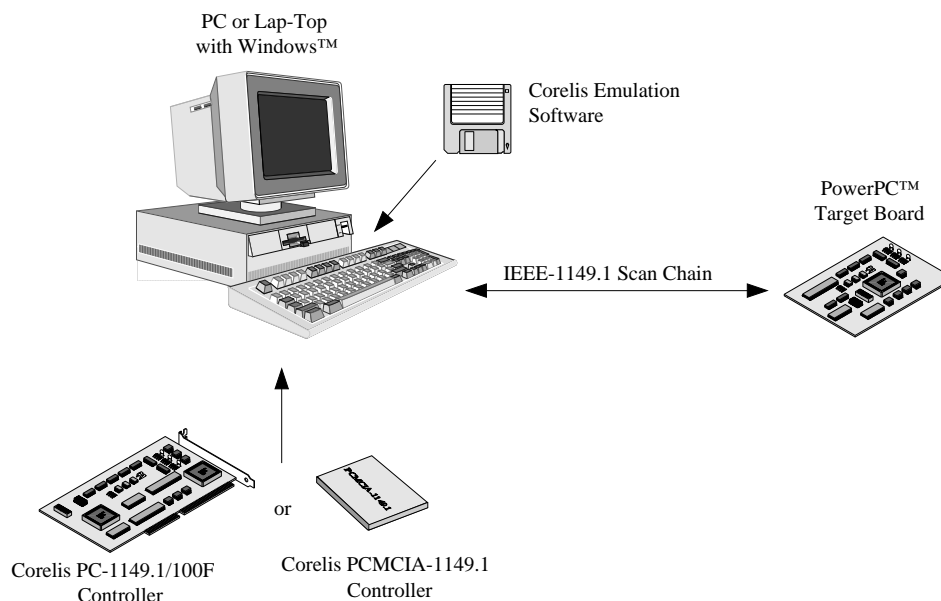
The Corelis PowerEM family of emulators utilize the industry standard IEEE-1149.1 (JTAG) Boundary-Scan Test port to access the internal debug resources available on the PowerPC family of microprocessors. Since the boundary-scan logic of the PowerPC microprocessors is separate from the core processor logic itself, this access mechanism allows complete non-intrusive access to any processor resources. Thus, no interrupts, no RAM, ROM or registers need to be assigned for debug purposes, and no ROM-based debugger or loader is required. At the same time, no peripheral resources such as serial ports are needed to communicate with the emulator/debugger.

In addition to these benefits, the use of the JTAG interface also ensures that processor access is maintained even when the processor "hangs" or otherwise runs out of control.

Windows™-based host software provides a complete symbolic C source-level debugging capability and is compatible with all popular cross-compilers.

Programs and data can be downloaded to any part of the system RAM through the JTAG port without the need for a resident loader program.

The JTAG interface is a simple, nine-wire interface that connects to the target system via a flexible ribbon cable, and does not require removing the microprocessor. The JTAG interface is controlled by a Corelis-developed boundary-scan controller board that is installed into a PC in an ISA bus slot. Alternatively, a PCMCIA-card version is available if a laptop-based emulator is desired. Direct access to the ISA or PCMCIA bus allows for very fast code download.



Software Generation and Debug Tools (Cross)

Due to the unique nature of the PowerEM emulators, the same hardware board can be used for any of the PowerPC-family of microprocessors that have IEEE-1149.1 compatibility. Thus, a developer using a PowerPC-family microprocessor can easily migrate to other PowerPC chips as they are introduced and retain any investment in hardware tools by merely installing another version of the Corelis PowerEM emulator software.

Features

- Real-time non-intrusive emulation of PowerPC 403, 603, and 604 microprocessors.
- Full symbolic and source-level debugging with an intuitive Windows GUI.
- Supports maximum processor clock speeds with zero wait states.
- High-performance IEEE-1149.1 (JTAG) controller card supports the entire PowerPC family.
- PCMCIA version for laptop emulation.
- Requires no hardware or software resources from the target system.

- High-speed program download: no need for on-board ROM.
- Examine and modify processor resources without imposing hardware between the processor and the target.
- Complete mnemonic disassembly.
- User-programmable toolbars and complete macro facility.
- On-line help system.
- Optional boundary-scan (JTAG) test tools.

Technical Support

- Full-time product-support staff, available to address technical questions and problems. Support via telephone, email and fax.
- Integrated with most commonly available PowerPC target boards.

Devices Supported

- PowerPC 403, 603, 603e, 603ev, and 604 microprocessors.

Availability

- Available now.

Contact

Corelis Inc.

12607 Hidden Creek Way
Cerritos, CA 90703
Tel: (310) 926-6727
Fax: (310) 404-6196
Email: sales@corelis.com

Sweden

Pelcon Electronics AB
Girovagen
S-175 06 Jarfalla
Sweden
Tel: 8-796-9870
Fax: 8-760-7685

Germany

Synatron
Technopark Neukeferich
Bretonischer Ring 13
D-85630 Grasbrunn
Tel: 89-460-2071
Fax: 89-460-5661

Ireland

BIC Systems
Europa House
Harcourt St.
Dublin 2, Ireland
Tel: 353-14754-223
Fax: 353-14754-778

Japan

Techno-Port Co. Ltd.
Nakagin Bldg. 10-2
Higashi-Shingashi 2-chome
Mianto-ku, Tokyo
Tel: 81-3-3434-3671
Fax: 81-3-3434-3897

Canada

Testforce Systems
5990 Vanden Abeele
St. Laurant, Quebec
Canada H4S 1R9
Tel: (514) 856-0970
Fax: (514) 856-6983

Diab Data Compiler Suites (D-CC, D-C++, D-F77)

Compilers, Libraries, Utilities

Diab Data, Inc.

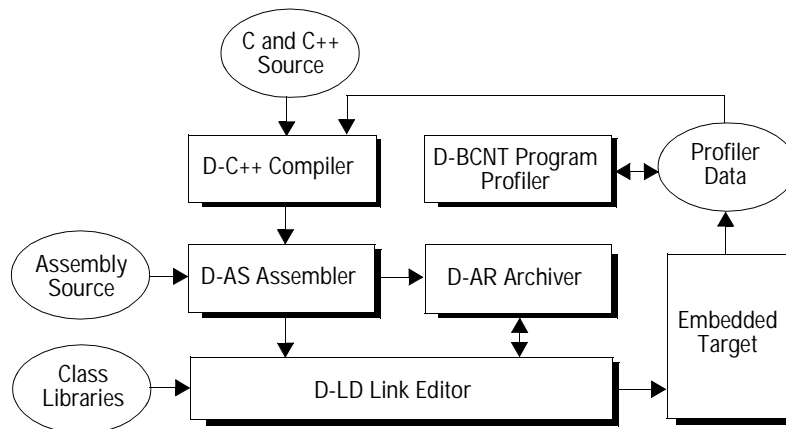
Diab Data offers C, C++, and F77 compiler suites for embedded PowerPC applications that give programmers the flexibility required to overcome the resource constraints of embedded applications. Each compiler suite includes a highly optimizing compiler, tightly integrated program profiler, program checker, assembler, linker, archiver, ANSI compliant libraries, floating-point libraries, and other utilities. Over 50 optimization techniques maximize the performance of the PowerPC pipelined architecture.

The program profiler identifies the blocks of code executed most frequently. The profile data can then be fed back to the compiler for further tuning of the application code. The profiler can also help identify bottlenecks in the application code.

Features

- Complete control of memory allocation for code and data.

- Flexible assembly macros for in-lining of assembly in C or C++ code.
- ROMable, re-entrant code and libraries.
- Flexible structure packing.
- Startup and termination module with conditional code for many I/O devices, and ROM-to-RAM initialization.
- Simulated file I/O in target RAM.
- Volatile keyword especially useful for I/O variables located at specific addresses.
- Interrupt functions.
- Nearly 150 well documented options for detailed control of the compiler.
- Intelligent defaults allowing generation of optimized code right out of the box.
- Complete C++ implementation, including exceptions, templates and RTTI.
- Choice of convention between strict ANSI C X3.159-1989, ANSI C with extensions, K&R C, or PCC C to emulate the System V.3 UNIX compiler.



Software Generation and Debug Tools (Cross)

- Hierarchical configuration files allow the customization of the compiler to fit specific requirements.
- The compiler suite can output PowerPC EABI compliant ELF / DWARF code, as well as IEEE695 and COFF. The ELF/DWARF release will be available within six months of a final EABI specification.

Examples of Optimizations

The Diab Data compiler suites provide excellent execution speed and code quality. Examples of high-payoff optimizations include:

- Global argument address assignments across functions.
- Register allocation across functions.
- Common sub-expression elimination throughout entire functions.
- Complex branch optimization.
- Partial in-lining based on execution profile.

Examples of optimizations specific to the PowerPC family include:

- Code reordering and instruction scheduling based on flow analysis of entire functions. This optimizes code execution through the pipeline.
- Use of the count registers as for and while loop counters. This reduces overhead during the execution of loops.
- Early calculation of condition codes. This reduces branch speculation.

Hosts Requirements

- Personal computers running DOS 5.0, Windows 95[®], Windows NT[™] and later.
- SPARCstations[®] running SunOS[™] 4.1.1 and later releases, and Solaris[®] 2.4.
- HP 700 series workstations running HP/UX[®] 8.07 and later releases.
- IBM RS/6000 workstation running AIX[®] 4.1.
- Silicon Graphics workstation running IRIX[™]

Third-Party Tools Support

- *Source-Level Debuggers*—SingleStep[™], VxWorks[®], Tornado[™] (under development), RISCWatch[™].
- *RTOS*—OSE[®], pSOS+[™], RTX[™], Wind[™] kernel, Chorus, C-Exec[®], Norti, Nucleus, others.
- *ICE and Related*—Applied Microsystems, Corelis, EST, Hewlett-Packard, Huntsville Micro, Lauterbach, Tektronix.
- *Simulators*—PowerPC Visual System, SingleStep.

Technical Support

- Example-rich product documentation.
- Email, phone, fax and modem links.
- All tools have a warranty. Extended warranties maintenance agreements are available.

Availability

- Available now.

Contact

Diab Data, Inc.
323 Vintage Park Drive
Foster City, CA 94404
Tel: (415) 571-1700
Fax: (415) 571-9068
Email: d-veloper@ddi.com
Web: <http://www.diabdata.com/users/diab>

P.O. Box 229
West Point, PA 19486-0229
Tel: (215)-362-1786
Fax: (215)-362-1723
Email: d-veloper@ddi.com

In Europe
Diab Data, Inc.
P.O. Box 20 123
S-104 60 Stockholm
SWEDEN
Tel: +46-8 462 03 79
Fax: +46-708 17 77 03
Email:
d-veloper@ddi.com

In Japan
Lifeboat, Inc.
3-6 Kanoa-Nishikicho
Chiyoda-Ku
Tokyo 101, Japan
Tel: +81-3-3293-4719
Fax: +81-3-3219-2866
Email:
watanabe@lifeboat.co.jp

FlashICE™

Analyzer, Emulator/Simulator

Grammar Engine Inc.

FlashICE, like Grammar Engine's PromICE, provides a fast and easy way to download code prior to testing or debugging. FlashICE adds simulation and diagnostic capabilities for developers using Flash memory. FlashICE responds to Flash commands such as sector writes and erases, and also provides feedback, error messages and positive verification for embedded algorithms for writing to Flash. In addition, FlashICE provides statistical information of wear leveling among sectors, and permits the simulation of error conditions (such as bad sectors) to test error handling capabilities.

FlashICE comes standard with Grammar Engine's exclusive Analysis Interface technology which provides a "virtual UART" that allows communication between target and host through the PromICE. This channel allows debugging without requiring the target's serial port or other target resources, and can be used to monitor program status and operation.

Features

- Simulates AMD 29F010, 29F040
- Ultra-fast downloads: 90KBytes/second (PC Parallel port)
- Unix Ethernet support available
- Support for DOS, Unix and Macintosh hosts
- Connects to any socket (DIP, PLCC, Custom cables available)
- Write, Reset and Interrupt lines for connection to target External or parasitic power
- Battery-backed memory standard
- Support for 3 Volt systems

Software Generation and Debug Tools (Cross)

Requirements

- Embedded target, host system.

Availability

- Available now.

Grammar Engine Inc.

921 Eastwind Drive
Suite 122
Westerville, Ohio 43081
Tel: (614) 899-7878
Fax: (614) 899-7888
Technical BBS: (614) 899-6230
Email: info@gei.com

Contact

For ordering: (800) 776-6423

PromICE™

Emulator/Simulator

Grammar Engine Inc.

PromICE is a powerful and affordable tool for embedded PowerPC development. Ultra-fast code downloads allow testing of code changes in seconds instead of minutes, saving valuable software development time. PromICE will download 128 KByte X 32 bit file in 6 seconds through a standard PC parallel port. Fast downloads across Unix Ethernet networks are available as well.

Our exclusive Analysis Interface provides a "virtual UART" that allows communication between target and host through the PromICE. This channel allows debugging without requiring the target's serial port or other target resources, and can also be used to monitor program status and operation.

Features

- Economical: (Emulate 128 KByte X 32 bit memory for approximately \$2,500.00)
- Ultra-fast downloads: 90KBytes/second (PC Parallel port)
- Unix Ethernet support
- Support for DOS, Unix and Macintosh hosts
- Emulates any size ROM up to 16 Mbit (2 MByte)
- Emulates a full 8 MByte of ROM for 32 bit systems
- Emulates access times as fast as 70ns
- Connects to any ROM socket (DIP, PLCC, Custom cables available)
- Write, Reset and Interrupt lines for connection to target External or parasitic power
- Battery-backed memory standard
- Support for 3 Volt systems available

Software Generation and Debug Tools (Cross)

Requirements

- Embedded target, host system.

Availability

- Available now.

Contact

Grammar Engine Inc.
921 Eastwind Drive
Suite 122
Westerville, Ohio 43081
Tel: (614) 899-7878
Fax: (614) 899-7888
Technical BBS: (614) 899-6230
Email: info@gei.com

For ordering: (800) 776-6423

Green Hills™ Ada

Compiler, Utilities, Libraries

Green Hills Software, Inc.

Green Hills Ada for PowerPC microprocessors is a member of the Green Hills family of highly optimizing compilers for 32- and 64-bit microprocessors. Green Hills Ada is a full implementation of Ada83, conforming to MIL-STD 1815A and implementing all of the optional "Chapter 13" features. Green Hills Ada is a true compiler, not a language translator.

Heritage and Performance

Green Hills Ada was created by adapting the Meridian Ada-to-C translator to produce a Green Hills compatible parse tree. This front end was then combined with the Green Hills global optimizer and code generators. The result is a family of compilers which combines Meridian's long Ada experience with the high performance traditionally associated with Green Hills compilers. Ada compilers had previously suffered a reputation for generating poor code. With the Green Hills/Meridian partnership the situation is now rectified.

Green Hills provides native and embedded Ada compilers for most UNIX systems. With these, embedded programmers can write and test large portions of their code on their host workstations. This is especially useful during early stages of development, when emulators and target systems are scarce. A simple recompile is all that is needed to use the code on the actual target. Since the native and embedded compilers use the same front end, compatibility is assured.

Features

- Big and little-endian addressing.
- Generates code which can be mixed with code from other languages.
- Generates extended debug information to support Ada specific features.

- Embedded Features Package.
- Compatible with MULTI® development environment.

Optimizations

Green Hills Ada incorporates hundreds of optimizations to give you the best possible code. Code can be optimized for speed or size on a module basis. Green Hills optimizations include:

- Constant folding.
- Register allocation by coloring.
- Variable allocation by usage.
- Entry and exit code optimization.
- Register coalescing.
- Loop rotation.
- Leaf optimization.
- Constant address elimination.
- Constant subexpression elimination.
- Tail recursion.
- Dead block and dead code elimination.
- Constant propagation.
- Pipeline optimizations.
- Peephole optimizations.
- Loop invariant analysis.
- Strength reduction.
- Loop unrolling.
- Algorithmic optimization.
- Memory optimization.
- Space optimization.
- Procedure inlining.

Green Hills provides tools to help you analyze your code and develop appropriate optimization strategies. Some optimizations, such as loop optimization, can be enabled on a function by function basis.

Software Generation and Debug Tools (Cross)

Run-Time Error Checking

Green Hills Ada can inset checks that will catch many different kinds of run-time errors. These checks are compiled into your code and provide a high degree of checking for a minimal performance penalty. Errors which can be detected include:

- Array bounds checking.
- Value too large for variable.
- Unimplemented case in CASE statement.
- Attempt to use null pointer.
- Divide by zero.
- Access of unallocated memory.
- Memory read before initialization.
- Free of unallocated memory.
- Memory leak scan.
- Variant record access compatible with tag.

Small Data Area

Global and static variables must generally be accessed at their 32-bit addresses. Substantial savings in both code size and execution time can be had if such variables are collected into a memory area from which they can be accessed with more compact addressing

modes. Green Hills compilers for the PowerPC microprocessors support such a small data area, accessing the data in it with a short offset from a reserved base register.

Embedded Features

- Multiplicity of program/data sections.
- Separate allocation of variable and constant data.
- Startup routine for initialized variables.
- Interrupt level procedures.
- Object format conversion utilities.
- Linker directive file.
- Memory leak scan.

Host System Requirements

- Most UNIX workstations including Sun, HP, DEC, RS/6000, SGI, Data General, MIPS, 386/SCO, 386/Univel.
- PC running Windows.
- VAX/VMX by arrangement.

Availability

- Available now.

Contact

North America

Green Hills Software, Inc.
510 Castillo Street
Santa Barbara, CA 93101
Tel: (805) 965-6044
Fax: (805) 965-6343

Germany

XCC Software Sales
Tel: 49.721.616474
Fax: 49.721.621384

Belgium

RTUSI
Tel: 32.2.523.24.62
Fax: 32.2.520.83.09

Italy

ETNOTEAM
Tel: 39.2.26162.1
Fax: 39.2.2611075.5

United Kingdom

Real Time Products
Tel: 44.121.333.6955
Fax: 44.21.333.5433

Japan

Advanced Data Controls
Tel: 81.3.3576.5351
Fax: 81.3.3576.1772

Spain

Marben Software
Tel: 34.1.377.09.28
Fax: 34.1.377.19.93

France

SCT Electronique
Tel: 33.61.61.12.34
Fax: 33.61.61.12.22

Sweden

Avent Computer AB
Tel: 46.893.0550
Fax: 46.894.9083

Green Hills™ C/C++

Compiler, Utilities, Libraries

Green Hills Software, Inc.

Green Hills C/C++ for PowerPC microprocessors is a member of the Green Hills family of highly optimizing compilers for 32- and 64-bit microprocessors. Green Hills C/C++ implements all of the major dialects of the C/C++ languages:

- In K+R mode the compiler implements the original C language, and supports many extensions of the language as introduced by Western Electric, Berkeley and others.
- In ANSI mode the compiler conforms to the official ANSI C language standard.
- In Permissive ANSI mode, the compiler implements ANSI mode but permits commonly used non-ANSI constructs.
- In C++ 2.0, 2.1 and 3.0 mode the compiler implements the features of the corresponding version of C++.

Green Hills provides native and embedded C/C++ compilers for most UNIX systems. A simple recompile is all that is needed to use the code on the actual target. Since the native and embedded compilers use the same front end, compatibility is assured.

Features

- Big and little-endian addressing.
- Generates code which can be mixed with code from other languages.
- Generates extended debug information to support C++ specific features.
- C/C++ run-time library.
- Embedded features package.
- Compatible with MULTI® development environment.

Optimizations

Green Hills C/C++ incorporates hundreds of optimizations to give you the best possible code. Code can be optimized for speed or size on a module basis. Green Hills optimizations include:

- Constant folding.
- Register allocation by coloring.
- Variable allocation by usage.
- Entry and exit code optimization.
- Register coalescing.
- Loop rotation.
- Leaf optimization.
- Constant address elimination.
- Constant subexpression elimination.
- Tail recursion.
- Dead block and dead code elimination.
- Constant propagation.
- Pipeline optimizations.
- Peephole optimizations.
- Loop invariant analysis.
- Strength reduction.
- Loop unrolling.
- Algorithmic optimization.
- Memory optimization.
- Space optimization.
- Procedure inlining.

To get the best possible performance you must use different optimization strategies for different parts of your program. Green Hills provides tools to help you analyze your code and develop appropriate optimization strategies. Some optimizations, such as loop optimization, can be enabled on a function by function basis.

Software Generation and Debug Tools (Cross)

Run-Time Error Checking

Green Hills C/C++ can inset checks that will automatically catch many different kinds of run-time errors. These checks are compiled into your code and provide a high degree of checking for a minimal performance penalty. Errors which can be detected include:

- Array bounds checking.
- Value too large for variable.
- Unimplemented case in CASE statement.
- Attempt to use null pointer.
- Divide by zero.
- Access of unallocated memory.
- Memory read before initialization.
- Free of unallocated memory.
- Memory leak scan.
- Variant record access compatible with tag.

Small Data Area

Global and static variables must generally be accessed at their 32-bit addresses. Substantial savings in both code size and execution time can be had if such variables are collected into a memory area from which they can be accessed with more compact addressing

modes. Green Hills compilers for the PowerPC microprocessors support such a small data area, accessing the data in it with a short offset from a reserved base register.

Embedded Features

- Multiplicity of program/data sections.
- Separate allocation of variable and constant data.
- Startup routine for initialized variables.
- Interrupt level procedures.
- Object format conversion utilities.
- Linker directive file.
- Memory leak scan.

Host System Requirements

- Most UNIX workstations including Sun, HP, DEC, RS/6000, SGI, Data General, MIPS, 386/SCO, 386/Univel.
- PC running Windows.
- VAX/VMX by arrangement.

Availability

- Available now.

Contact

North America

Green Hills Software, Inc.
510 Castillo Street
Santa Barbara, CA 93101
Tel: (805) 965-6044
Fax: (805) 965-6343

Germany

XCC Software Sales
Tel: 49.721.616474
Fax: 49.721.621384

Belgium

RTUSI
Tel: 32.2.523.24.62
Fax: 32.2.520.83.09

Italy

ETNOTEAM
Tel: 39.2.26162.1
Fax: 39.2.2611075.5

United Kingdom

Real Time Products
Tel: 44.121.333.6955
Fax: 44.21.333.5433

Japan

Advanced Data Controls
Tel: 81.3.3576.5351
Fax: 81.3.3576.1772

Spain

Marben Software
Tel: 34.1.377.09.28
Fax: 34.1.377.19.93

France

SCT Electronique
Tel: 33.61.61.12.34
Fax: 33.61.61.12.22

Sweden

Avent Computer AB
Tel: 46.893.0550
Fax: 46.894.9083

Green Hills™ FORTRAN

Compiler, Utilities, Libraries

Green Hills Software, Inc.

Green Hills FORTRAN for PowerPC microprocessors is a member of the Green Hills family of highly optimizing compilers for 32- and 64-bit microprocessors. Green Hills FORTRAN implements three major dialects of the Fortran language:

- In F77 mode the compiler implements the ANSI Fortran standard, plus the extensions implemented by the UNIX F77 compiler.
- In VMS mode the compiler is compatible with DEC's VAX/VMS Fortran compiler.
- In DOD mode the compiler implements the Fortran language specified by MIL-STD-1753.

Green Hills provides native and embedded FORTRAN compilers for most UNIX systems. Since the native and embedded compilers use the same front end, compatibility is assured.

Features

- Big and little-endian addressing.
- Generates code which can be mixed with code from other languages.
- Generates extended debug information to support Fortran specific features.
- Optical case sensitive symbols.
- C preprocessor directive.
- POINTER data type.
- Many additional data types.
- Fortran run-time library.
- Embedded Features Package.
- Compatible with MULTI® development environment.

Optimizations

Green Hills FORTRAN incorporates hundreds of optimizations to give you the best possible code. Code can be optimized for speed or size on a module basis. Green Hills optimizations include:

- Constant folding.
- Register allocation by coloring.
- Variable allocation by usage.
- Entry and exit code optimization.
- Register coalescing.
- Loop rotation.
- Leaf optimization.
- Constant address elimination.
- Constant subexpression elimination.
- Tail recursion.
- Dead block and dead code elimination.
- Constant propagation.
- Pipeline optimizations.
- Peephole optimizations.
- Loop invariant analysis.
- Strength reduction.
- Loop unrolling.
- Algorithmic optimization.
- Memory optimization.
- Space optimization.
- Procedure inlining.

To get the best possible performance you must use different optimization strategies for different parts of your program. Green Hills provides tools to help you analyze your code and develop appropriate optimization strategies. Some optimizations, such as loop optimization, can be enabled on a function by function basis.

Software Generation and Debug Tools (Cross)

Run-Time Error Checking

Green Hills FORTRAN can insert checks that will catch many different kinds of run-time errors. These checks are compiled into your code and provide a high degree of checking for a minimal performance penalty. Errors which can be detected include:

- Array bounds checking.
- Value too large for variable.
- Unimplemented case in CASE statement.
- Attempt to use null pointer.
- Divide by zero.
- Access of unallocated memory.
- Memory read before initialization.
- Free of unallocated memory.
- Memory leak scan.
- Variant record access compatible with tag.

Small Data Area

Global and static variables must generally be accessed at their 32-bit addresses. Substantial savings in both code size and execution time can be had if such variables are collected into a memory area from which they can be accessed with more compact addressing

modes. Green Hills compilers for the PowerPC microprocessors support such a small data area, accessing the data in it with a short offset from a reserved base register.

Embedded Features

- Multiplicity of program/data sections.
- Separate allocation of variable and constant data.
- Startup routine for initialized variables.
- Interrupt level procedures.
- Object format conversion utilities.
- Linker directive file.
- Memory leak scan.

Host System Requirements

- Most UNIX workstations including Sun, HP, DEC, RS/6000, SGI, Data General, MIPS, 386/SCO, 386/Univel.
- PC running Windows.
- VAX/VMX by arrangement.

Availability

- Available now.

Contact

North America

Green Hills Software, Inc.
510 Castillo Street
Santa Barbara, CA 93101
Tel: (805) 965-6044
Fax: (805) 965-6343

Germany

XCC Software Sales
Tel: 49.721.616474
Fax: 49.721.621384

Belgium

RTUSI
Tel: 32.2.523.24.62
Fax: 32.2.520.83.09

Italy

ETNOTEAM
Tel: 39.2.26162.1
Fax: 39.2.2611075.5

United Kingdom

Real Time Products
Tel: 44.121.333.6955
Fax: 44.21.333.5433

Japan

Advanced Data Controls
Tel: 81.3.3576.5351
Fax: 81.3.3576.1772

Spain

Marben Software
Tel: 34.1.377.09.28
Fax: 34.1.377.19.93

France

SCT Electronique
Tel: 33.61.61.12.34
Fax: 33.61.61.12.22

Sweden

Avent Computer AB
Tel: 46.893.0550
Fax: 46.894.9083

Green Hills™ PASCAL

Compiler, Utilities, Libraries

Green Hills Software, Inc.

Green Hills PASCAL for PowerPC microprocessors is a member of the Green Hills family of highly optimizing compilers for 32- and 64-bit microprocessors. Green Hills PASCAL implements two major dialects of the Pascal language:

- Strict mode implements the BSI/IOS Level 1 standard with no extensions permitted.
- Extended implements BSI/IOS Level 1 plus most of the extensions of the Berkeley 4.2 BSD Pascal compiler (pcc).

Green Hills also provides native PASCAL compilers for most UNIX systems. A simple recompile is all that is needed to use the code on the actual target. Since the native and embedded compilers use the same front end, compatibility is assured.

Features

- Big and little-endian addressing.
- Generates code which can be mixed with code from other languages.
- Generates extended debug information to support Pascal specific features.
- Case sensitive symbols.
- C preprocessor directive.
- Data types for float and double.
- Interactive I/O support.
- Pascal run-time library.
- Embedded features package.
- Compatible with MULTI® development environment.

Optimizations

Green Hills PASCAL incorporates hundreds of optimizations to give you the best possible code. Code can be optimized for speed or size on a module basis. Green Hills optimizations include:

- Constant folding.
- Register allocation by coloring.
- Variable allocation by usage.
- Entry and exit code optimization.
- Register coalescing.
- Loop rotation.
- Leaf optimization.
- Constant address elimination.
- Constant subexpression elimination.
- Tail recursion.
- Dead block and dead code elimination.
- Constant propagation.
- Pipeline optimizations.
- Peephole optimizations.
- Loop invariant analysis.
- Strength reduction.
- Loop unrolling.
- Algorithmic optimization.
- Memory optimization.
- Space optimization.
- Procedure inlining.

To get the best possible performance you must use different optimization strategies for different parts of your program. Green Hills provides tools to help you analyze your code and develop appropriate optimization strategies. Some optimizations, such as loop optimization, can be enabled on a function by function basis.

Software Generation and Debug Tools (Cross)

Run-Time Error Checking

Green Hills PASCAL can insert checks that will automatically catch many different kinds of run-time errors. These checks are compiled into your code and provide a high degree of checking for a minimal performance penalty. Errors which can be detected include:

- Array bounds checking.
- Value too large for variable.
- Unimplemented case in CASE statement.
- Attempt to use null pointer.
- Divide by zero.
- Access of unallocated memory.
- Memory read before initialization.
- Free of unallocated memory.
- Memory leak scan.
- Variant record access compatible with tag.

Small Data Area

Global and static variables must generally be accessed at their 32-bit addresses. Substantial savings in both code size and execution time can be had if such variables are collected into a memory area from which they can be accessed with more compact addressing

modes. Green Hills compilers for the PowerPC microprocessors support such a small data area, accessing the data in it with a short offset from a reserved base register.

Embedded Features

- Multiplicity of program/data sections.
- Separate allocation of variable and constant data.
- Startup routine for initialized variables.
- Interrupt level procedures.
- Object format conversion utilities.
- Linker directive file.
- Memory leak scan.

Host System Requirements

- Most UNIX workstations including Sun, HP, DEC, RS/6000, SGI, Data General, MIPS, 386/SCO, 386/Univel.
- PC running Windows
- VAX/VMX by arrangement.

Availability

- Available now.

Contact

North America

Green Hills Software, Inc.
510 Castillo Street
Santa Barbara, CA 93101
Tel: (805) 965-6044
Fax: (805) 965-6343

Germany

XCC Software Sales
Tel: 49.721.616474
Fax: 49.721.621384

Belgium

RTUSI
Tel: 32.2.523.24.62
Fax: 32.2.520.83.09

Italy

ETNOTEAM
Tel: 39.2.26162.1
Fax: 39.2.2611075.5

United Kingdom

Real Time Products
Tel: 44.121.333.6955
Fax: 44.21.333.5433

Japan

Advanced Data Controls
Tel: 81.3.3576.5351
Fax: 81.3.3576.1772

Spain

Marben Software
Tel: 34.1.377.09.28
Fax: 34.1.377.19.93

France

SCT Electronique
Tel: 33.61.61.12.34
Fax: 33.61.61.12.22

Sweden

Avent Computer AB
Tel: 46.893.0550
Fax: 46.894.9083

MULTI[®] Execution Profiler

Analyzer

Green Hills Software, Inc.

The MULTI execution profiler for PowerPC[™] microprocessors is a tool designed to help improve the performance of your code by (1) helping you to isolate hot spots in your program and (2) providing you with a mechanism for using that information to improve the performance of your program.

The MULTI profiler produces many different reports to enable you to look at your program in different ways. The illustration shows the calls report, which lists each function in the program sorted by the amount of time spent in that function. The source lines report does the same thing to identify the lines that use the most time, and a call graph report shows the run-time structure of the program.

A block coverage report lists each basic block in the program and shows the number of times the block was entered. This report is especially useful in testing or quality assurance to establish that the test procedures exercise all cases.

Clicking on a line of any report (or on an element of any graph) causes the corresponding source code to be displayed in the debugger window. Each line of code is annotated with the amount of time spent on that line. An alternate display breaks execution down to the assembly level. This is useful for seeing the effects of cache misses and pipeline stalls.

Profiling data can be collected using any one of several techniques: the compiler can be set to inset code to count each time the program enters a function or a basic block, an interrupt clock can sample the location of the PC at regular intervals, or the trace buffer of an in-circuit emulator can be read. Many MULTI debug server/target combinations implement the data collection function automatically.

Mechanisms exist to allow information gathered from the use of the profiler to be used to automatically apply certain optimization strategies such as inlining or loop optimization to specified functions.

Software Generation and Debug Tools (Cross)

Host System Requirements

- Most UNIX workstations including Sun, HP, DEC, RS/6000, SGI, Data General, MIPS, 386/SCO, 386/Univel.
- PC running Windows.

Availability

- Available now.

Contact

North America

Green Hills Software, Inc.
510 Castillo Street
Santa Barbara, CA 93101
Tel: (805) 965-6044
Fax: (805) 965-6343

Germany

XCC Software Sales
Tel: 49.721.616474
Fax: 49.721.621384

Belgium

RTUSI
Tel: 32.2.523.24.62
Fax: 32.2.520.83.09

Italy

ETNOTEAM
Tel: 39.2.26162.1
Fax: 39.2.2611075.5

United Kingdom

Real Time Products
Tel: 44.121.333.6955
Fax: 44.21.333.5433

Japan

Advanced Data Controls
Tel: 81.3.3576.5351
Fax: 81.3.3576.1772

Spain

Marben Software
Tel: 34.1.377.09.28
Fax: 34.1.377.19.93

France

SCT Electronique
Tel: 33.61.61.12.34
Fax: 33.61.61.12.22

Sweden

Avent Computer AB
Tel: 46.893.0550
Fax: 46.894.9083

MULTI® Debug Servers for VxWorks, pSOS+ and Custom RTOSs

Debugger

Green Hills Software, Inc.

The MULTI RTOS debug servers for PowerPC™ microprocessors provide a mechanism by which the MULTI development environment can be used to develop programs for targets which incorporate commercial or custom real-time operating systems. The popular VxWorks and pSOS+ operating systems are explicitly supported; a customizable debug server is provided for use with other RTOSs.

The debug servers bring multitask debugging to any RTOS. They allow MULTI to open several debug windows simultaneously, one for each task running on the target. The full power of the MULTI debugger can be brought to bear on each task: you can halt and continue execution, examine variables, set breakpoints and single step.

A special task window displays the essential data from the operating system's process table. The entry for each task is listed on a separate line of the display. Clicking on a task entry opens a debug window on the corresponding task. Command windows provide a channel with which the user can communicate directly with a task using the *stdin*, *stdout* and *stderr* streams.

Host I/O support allows processes on the target to access the host's file system and I/O devices using standard system calls including *open()*, *lseek()*, *read()*, *write()*, and *close()*, and to issue shell commands using *system()*.

The *probserv* debug server uses ethernet sockets to communicate with the standard pROBE+ debug process of the pSOS+ operating system. Command windows allow you to access the full functionality of the pROBE+ monitor, including event breakpoints.

The *vxserv* debug server uses ethernet sockets to communicate with the standard VxWorks debug task RdbTask. Special commands allow the programmer to load and dynamically link programs into VxWorks at run time. VxWorks tasks can be started and stopped, and can be set to halt on system events such as task creation.

The *rtserv* debug server is a special debug server designed to allow customers to interface MULTI to their own custom RTOSs.

Due to the limitations of some operating system not all features are supported on all systems.

Software Generation and Debug Tools (Cross)

Ada Development Environment

Vxser, when combined with the Green Hills Ada compiler, the MULTI development environment and the VxWorks operating system, is the key to bringing you a complete tool solution for developing Ada programs.

Host System Requirements

- Most UNIX workstations including Sun, HP, DEC, RS/6000, SGI, Data General, MIPS, 386/SCO, 386/Univel.
- PC running Windows.

Availability

- Available now.

Contact

North America

Green Hills Software, Inc.
510 Castillo Street
Santa Barbara, CA 93101
Tel: (805) 965-6044
Fax: (805) 965-6343

Germany

XCC Software Sales
Tel: 49.721.616474
Fax: 49.721.621384

Belgium

RTUSI
Tel: 32.2.523.24.62
Fax: 32.2.520.83.09

Italy

ETNOTEAM
Tel: 39.2.26162.1
Fax: 39.2.2611075.5

United Kingdom

Real Time Products
Tel: 44.121.333.6955
Fax: 44.21.333.5433

Japan

Advanced Data Controls
Tel: 81.3.3576.5351
Fax: 81.3.3576.1772

Spain

Marben Software
Tel: 34.1.377.09.28
Fax: 34.1.377.19.93

France

SCT Electronique
Tel: 33.61.61.12.34
Fax: 33.61.61.12.22

Sweden

Avent Computer AB
Tel: 46.893.0550
Fax: 46.894.9083

MULTI® Source Level Debugger

Debugger

Green Hills Software, Inc.

The MULTI source level debugger for PowerPC™ microprocessors supports programming in Ada, C, C++, Fortran, Pascal and assembly language. Its basic functions are intuitive and simple to use. Programmers can generally do useful work by simply starting MULTI and following their instincts.

MULTI can be used to debug most target systems. It can be used in conjunction with software simulators, a ROM monitor, in-circuit emulators and has been adapted to work with many commercial real-time operating systems. MULTI is available as a native program development environment for most UNIX systems. This allows programmers to use the same tools for both native and embedded development.

The MULTI debugger takes full advantage of the properties of a windowing environment. In addition, the debugger has many advanced features, including special support for multiple processes, X-Window development and embedded programming. Class and program browsing capabilities let you understand the structure of your program and of programs you inherit.

MULTI is a true C++ debugger, with support for C++ seamlessly integrated at every level. It evaluates C++ expressions and automatically mangles and demangles C++ names. Casts and coercions are performed implicitly, and ambiguities regarding overloaded operators are automatically resolved. Template debugging is fully supported.

Software Generation and Debug Tools (Cross)

Host System Requirements

- Most UNIX workstations including Sun, HP, DEC, RS/6000, SGI, Data General, MIPS, 386/SCO, 386/Univel.
- PC running Windows.

Availability

- Available now.

Contact

North America

Green Hills Software, Inc.
510 Castillo Street
Santa Barbara, CA 93101
Tel: (805) 965-6044
Fax: (805) 965-6343

Germany

XCC Software Sales
Tel: 49.721.616474
Fax: 49.721.621384

Belgium

RTUSI
Tel: 32.2.523.24.62
Fax: 32.2.520.83.09

Italy

ETNOTEAM
Tel: 39.2.26162.1
Fax: 39.2.2611075.5

United Kingdom

Real Time Products
Tel: 44.121.333.6955
Fax: 44.21.333.5433

Japan

Advanced Data Controls
Tel: 81.3.3576.5351
Fax: 81.3.3576.1772

Spain

Marben Software
Tel: 34.1.377.09.28
Fax: 34.1.377.19.93

France

SCT Electronique
Tel: 33.61.61.12.34
Fax: 33.61.61.12.22

Sweden

Avent Computer AB
Tel: 46.893.0550
Fax: 46.894.9083

HMI-200 Series In-Circuit Emulator

Debugger, Emulator/Simulator

Huntsville Microsystems, Inc.

The HMI-200 series in-circuit emulator for the IBM 403GA embedded RISC controller provides real-time emulation at full clock speeds. The unit includes complex break and trigger points, real-time trace, high speed overlay RAM, shadow RAM, and HMI's SourceGate® II source-level debugger. Communication with the host computer is supported using a high speed serial port (115.2KB) and a parallel port for fast code downloading. An optional Ethernet interface is also available.

The trace buffer records full address, data, and control signal information along with external trace bits which may be clipped onto a target system. The trace may be qualified to isolate specific data of interest and may be viewed without stopping emulation using the Freeze Trace function. A hardware implemented performance analysis system for software performance profiling and code coverage analysis is also included.

The emulator is integrated with HMI's source-level debugger, SourceGate® II. SourceGate II provides full emulator control, variable data monitoring via Watch Windows, complete source-level debugging features detailed trace information, and extensive on-line help.

Specifications

- 25 and 33 MHz clock speeds at zero-wait states.
- PQFP adapter.
- Serial and parallel interfaces. Ethernet optional.
- 16 external trace bits.
- 4 complex hardware breakpoints
- 512KB, 1MB, 2MB, or 4MB overlay RAM.
- 512KB or 2MB shadow RAM.
- 1 mSec resolution interval timer.
- 32KB trace buffer including:
 - Addresses
 - Data
 - Bus status
 - External trace bits
 - Time stamp (50ns resolution)
- Hardware implemented performance analysis.

Software Generation and Debug Tools (Cross)

Platforms Supported

SourceGate II features support for all major C and Ada compilers hosted on IBM PC, HP and Sun based platforms with full native GUI environment support for Windows, Windows NT, UNIX, Motif (HP), and OPEN LOOK (Sun).

Availability

- Available now.

Contact

Huntsville Microsystems, Inc.
P.O. Box 12415
Huntsville, AL 35815
Tel: (205) 881-6005
Fax: (205) 882-6701
Email: sales@hmi.com
Web: <http://www.hmi.com>

IBM High C/C++™

Compiler, Utilities

IBM Corporation

The IBM High C/C++ product provides the essential tools and enabling technology for creating and distributing embedded PowerPC applications. This 32-bit tool set provides eight levels of optimization to allow you to optimize for your particular embedded PowerPC application.

The IBM High C/C++ tool set provides host support for the following platforms targeted to the PowerPC embedded controllers:

- DOS and Extended DOS on Intel X86 and Pentium
- AIX on RS/6000
- SunOS 4.1 or Solaris on SPARCstation or equivalent

Attention to the evolving ANSI C++ Standard gives you cross-platform compatibility and predictability. The IBM High C/C++ tool set produces machine language that is compact, fast, and efficient, allowing large, complex applications to be developed and deployed. The compiler in the tool chain is a true compiler, not a C to C++ translator. The "Incremental strengths" feature permits specification of the level of C++ compilation, allowing migration from C to C++ in stages.

Functional Summary

- Big- and little-endian addressing
- Eight levels of global optimization
- Optional ANSI-Standard conformance
- Extensive and scalable error/warning messages
- Wide variety of compiler features available through toggles and pragmas
- Floating-point code generation using highly optimized floating-point libraries from U.S. Software
- C or C++ compiler invoked based on user-definable source-file extension
- Lint-like checking
- Source-annotated assembly listings
- Inline functions across compilation units
- No restriction on complexity of inlined functions
- Four user-selectable levels of warning messages with more than 500 diagnostic messages
- Supports ELF and DWARF

Software Generation and Debug Tools (Cross)

Flexibility Options

Choose from a large selection of toggles and pragmas to customize the compiler to meet your specific needs. You can, among many other options:

- Adjust the code size-execution speed trade-off in generated code.
- Adjust external naming conventions to agree with linkers and operating systems.
- Place code or data in specific locations for embedded applications.
- Develop on any of four different platforms.

Right Levels of Global Optimization

You can optimize programs for execution speed and/or code size, or to achieve faster compile times, with a single command-line switch. High C/C++ supports the classic optimizations including retro-allocation via the graph coloring technique.

Incremental Strengths

The "incremental strengths" feature permits specification of the level of C++ compilation, allowing you to migrate from C to C++ in stages.

System Requirements

- RS/6000 running AIX.
- SPARCstation or equivalent running SunOS 4.1 or Solaris.
- 386-486-Pentium running DOS or Extended DOS.

Processors Supported

- IBM PowerPC processors.

Availability

- Available now.

Contact

United States and Canada

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531
Tel: (800) PowerPC
Fax: (800) POWERfax

IBM homepage:
<http://www.ibm.com>

IBM Microelectronics homepage:
<http://www.chips.ibm.com>

Fax Service: (415) 855-4121

Europe

IBM
La Pompignane BP 1021
34006 Montpellier
France
Tel: (33) 6713-5757 (French)
Tel: (33) 6713-5756 (Italian)
Fax: (33) 6713-5750*
*from Paris add 16

IBM
Informations Systeme GmbH
Laatzener Str. 1
30539 Hannover
Germany
Tel: (49) 511-516-3444 (English)
Tel: (49) 511-516-3555 (German)
Fax: (49) 511-516-3888

Japan

IBM
800, Ichimiyake,
Yasu-cho, Yasu-gun
Shiga-ken, Japan 520-23
Tel: (81) 775-87-4745
Fax: (81) 775-87-4735

PowerPC Virtual Simulator

Emulator/Simulator, Simulation Model

IBM Corporation

The PowerPC Virtual Simulator (PVS) solves many of your system modeling problems and provides capability not previously available to system or embedded controller designers. It is comprised of the following:

- *Visual Simulator*—Architectural model for each PowerPC processor.
- *Timer Feature*—System timing and performance modeling.
- *I/O Models*—Behavioral Models and 'C' functions.
- *Bus Models for ASICs*—VHDL models and interface to ASIC simulators.

PVS is a client/server application designed for inter-operability. It will operate with other systems on a network that support TCP/IP and Telnet.

Visual Simulator

PVS is an instruction-level simulator for the PowerPC architecture with an integrated high-function graphical user interface.

The simulator presents a software view of the PowerPC architecture. It models the PowerPC instruction set, register space, and memory space. It also models most elements of the PowerPC operating environment architecture such as effective-to-virtual-to-real address translation, interrupts, and processor specific registers. It provides very high speed instruction execution with state-of-the-art usability that includes a 'C' source level debugger.

Timer Feature

The Timer feature is a software model that emulates the performance characteristics of a specific PowerPC processor. This tool is intended to be used by designers to tailor the subsystem in which a PowerPC microprocessor will be operating. Designers using the PVS Timer (in conjunction with the PVS simulator) are able to model the performance of their system. The Timer allows users to change many system parameters such as cache size, latency, and memory bus access. The Timer is also valuable for modeling timing sensitive code such as interrupt routines or I/O handling modules. Developers can use the architectural simulator and timer to quickly determine if their hardware and/or software designs will meet system objectives.

I/O Models and PVS API

The PVS Application Programmable Interface (API) is a set of 'C' language functions that allow you to write an I/O model that interacts with the PowerPC I/O space. The API provides functions that are called by PVS (and must be available in your I/O model) when I/O loads and stores are executed, PVS is reset, or other basic functions executed. Your I/O model performs operations based on the data passed to it and can raise an external interrupt, load/store I/O space, and read/write main storage (simulating DMAs) if desired. Your I/O model can be written at any level of abstraction using this interface.

Software Generation and Debug Tools (Cross)

Bus Models and API

The I/O model API can also be used to connect PVS to a PowerPC bus model written to run in your ASIC simulation environment. Included with PVS are VHDL models that simulate the bus signals and activity generated when you program executes on the simulator. This provides the ability to build a complete system model for verification of both your hardware designs and the software prior to the "tape out" of your silicon or board design. Contact IBM for information on models for your specific simulation environment.

Architectures Supported

- PowerPC 403GA, 601, 603, 604, and 620 microprocessors.

System Requirements

- RISC System/6000 POWERstation or POWERserver with AIX Version 3.2.5 (5756-030).

Technical Support

- Software maintenance agreement.

Availability

- Available now.

Contact

IBM Corporation
PowerPC Verification Technology
Department MEV
Rochester, MN 55901
Tel: (800) 365-4426 ext 330

RISCWatch™

Analyzer Interface, Debugger, Disassembler, Real-Time Tool, Test Suite, Utilities

IBM Corporation

RISCWatch is a hardware and software development tool for PowerPC microprocessors and the PowerPC 400Series™ of Embedded Controllers. The source level debugger and processor control features provide the application designer with the tools needed to develop and debug hardware and software quickly and efficiently.

Features

- Simple and reliable 16-pin interface to the system under development.
- Intuitive and easy-to-use windowed user interface that reduces development time.
- Command file support for automated tests and command sequences.
- C source and assembler level debugging.
- Network support for remote debugging of the system under development.
- Complete access and control of processor resources.
- Supports the Embedded ABI for PowerPC Standard (ELF/DWARF) and XCOFF for AIX.
- Hosted on IBM RS/6000, Sun, and PC/Windows.
- Real-time trace support via the RISCTrace™ feature for the PowerPC400Series.

C and C++ Source and Assembler Debugging

The C and C++ source and assembler level debugger runs in a multi-window environment enabling improved user productivity. Features include single-stepping, multiple hardware and software breakpoints, variable viewing/updating, program run, stop, and restart, user-defined screens and buttons, caller stack context switching, and a full set of watch capabilities.

Processor Control

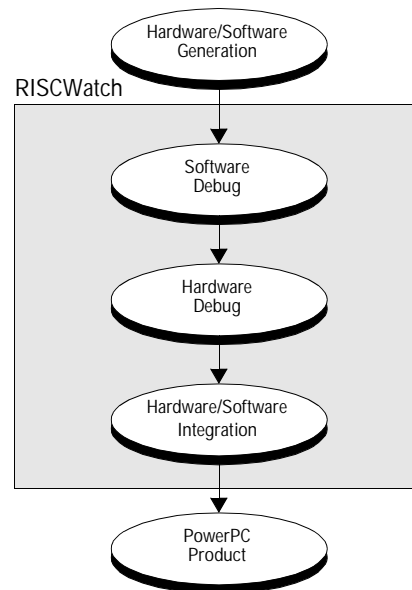
Low-level processor control functions include single-step, set breakpoints, run-to-breakpoints, reset, initialize, and processor stop.

Processor Watch

Low-level processor watch functions include displaying and modifying memory, registers, and cache. Memory can also be loaded and disassembled.

Command File Support

Command file support allows test cases to be written off-line and then run automatically. Command files can also be used for running regression tests, initializing the processor, and automating command sequences.



Software Generation and Debug Tools (Cross)

User Interface

The user-friendly multiwindowed user interface provides a rich set of predefined screens, pulldowns, and utilities. Additionally, the user-defined resource capabilities allow the developer to build custom screens and buttons tailored to individual display and control preferences.

Processor Specific On-line Help

On-line help support is included with RISCWatch. It includes help specific to each processor including register definitions and instruction help.

RISCTrace™

RISCTrace is a feature of RISCWatch. Combined with a logic analyzer, RISCTrace provides instruction tracing of code that executed in real-time including instructions executed with the instruction cache enabled. The PowerPC 400Series supports the RISCTrace feature.

Chips Supported

- PowerPC 601, 602, 603, and 604 microprocessors.
- PowerPC 403GA, 403GB, and 403GC embedded controllers.

Hosts Supported

- RISC System/6000, Sun, PC.
- 386, 486 or Pentium running DOS/Windows 3.1 with a Windows Sockets-compatible TCP/IP protocol stack.
- SPARCstation or equivalent running Solaris 2.3 or SunOS 4.1.3 with OpenWindows.

Technical Support

- Documentation.
- Phone, fax, and email links.
- Maintenance services.

Availability

- Available now.

Contact

United States and Canada

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531
Tel: (800) PowerPC
Fax: (800) POWERfax

IBM homepage:
<http://www.ibm.com>

IBM Microelectronics homepage:
<http://www.chips.ibm.com>

Fax Service: (415) 855-4121

Europe

IBM
La Pompanne BP 1021
34006 Montpellier
France
Tel: (33) 6713-5757 (French)
Tel: (33) 6713-5756 (Italian)
Fax: (33) 6713-5750*
*from Paris add 16

IBM
Informations Systeme GmbH
Laatzener Str. 1
30539 Hannover
Germany
Tel: (49) 511-516-3444 (English)
Tel: (49) 511-516-3555 (German)
Fax: (49) 511-516-3888

Japan

IBM
800, Ichimiya,
Yasu-cho, Yasu-gun
Shiga-ken, Japan 520-23
Tel: (81) 775-87-4745
Fax: (81) 775-87-4735

TRACE32 BDM/ROM Debugger

Analyzer, Debugger, Emulator/Simulator

Lauterbach Datentechnik

TRACE32 provides a complete set of tools for testing software and hardware in embedded designs. The system is configurable as a low-cost development work place as well as a complex high-end tool.

TRACE32 works with a variety of host interfaces. The communication link to the host is fiber optic interface or Ethernet. SCSI, RS232, RS422 and parallel interface are also supported. It is possible to share a TRACE32 in a LAN of PCs and workstations.

The high-level language debugger offers the same features as TRACE32-ICE and supports most third party compilers for Ada, C, C++, Modula 2 and assembly languages. The software is compatible with the TRACE32-ICE system. The windowed user interface is completely configurable.

TRACE32 Features

- Same system for different microprocessors and microcontrollers.
- Interface to all host computers also in a heterogeneous LAN.
- High-level language debugger independent of programming language and compiler.
- Multi-task debugger.
- In-circuit emulator.
- Logic-state analyzer.
- Timing analyzer.
- Performance analyzer.

BDM/ROM Debugger Features

- Software compatible with TRACE32-ICE.
- Debugging via BDM interface or EPROM simulator.
- Source window.

- Variable window.
- Stack frame window.
- Array and structure display.
- Register and peripheral display.
- Program and spot breakpoints.
- 100 KByte/sec download speed.
- Trigger input and output.
- Evaluation boards for test stage.

Platforms Supported

- PC Windows
- SCO-ODT
- SUN3, SPARC
- DEC-ULTRIX
- VAX-VMS
- ALPHA-OSF1, ALPHA-VMS
- HP9000/300/400/700
- RS6000 (in preparation)

Third-Party Compilers Supported

- GNU (XCOFF)
- MOTOROLA (XCOFF)
- Diab Data (ELF/DWARF)

PowerPC Microprocessors Supported

- PowerPC 603 and 604 microprocessors.
- PowerPC 403GA and 403GB embedded controllers.

Technical Support

- Local application engineers.
- Technical support hotline.
- Training.

Availability

- Available now.

Software Generation and Debug Tools (Cross)

Contact

A complete listing of international representatives may be found at www.lauterbach.com/replist.html

Australia

ELEKTRO OPTICS Pty. Ltd
Level 1, Nelson Street
Kenthurst N.S.W. 2156
Tel: (2) 6541873
Fax: (2) 6541539
Email: philmo@electro.oz.au
Web: <http://www.electro.oz.au>

Austria

Nowatron Elektronik GmbH
Eitnergasse 7
A-1230 Wien
Tel: (1) 8658543-0
Fax: (1) 8658543-7

Benelux

TRITEC Benelux B.V.
Antoniuslaan 1
NL-3341 GA Hendrik Ido
Ambacht
Tel: ++31 78 681 61 33
Fax: ++31 78 682 00 30
Email: development-tools@tritec.nl

China

Watertek Inc.
Dongshen electron Building
N. B3 Tucheng West Rd, Haidian
Beijing, P.R. China 100088
Tel: +86-10-2383376
Fax: +86-10-2373872
Email: xjwater@public.bta.net.cn

Denmark

NOHAU Denmark A/S
Naverland 2
DK-2600 Glostrup
Tel: 43446010
Fax: 43446020
Email: nohau-dk@inet.uni-c.dk

Egypt

WANTECH
14 Amin El-Rafie St., Appt. 9
Cairo, Egypt
Tel: (+202) 349-5931
Fax: (+202) 349-5931
Email: wantech@ritsec2.com.eg

France

LOGIC INSTRUMENT
33, Rue des Molleons
F-95230 Soisy Sous Montmorency
Tel: (1) 39899622
Fax: (1) 34280050
Email: 100772.3071@compuserve.com

Germany

Lauterbach Datentechnik GmbH
Fichtenstr. 27
D-85649 Hofolding
Tel: (08104)8943-28
Fax: (08104)8943-49
Email: info@lauterbach.com
Web: <http://www.lauterbach.com>

India

Electro Systems
4215 JK Complex First Main Rd.
Bangalore 560 021 India
Tel: 0091 803 323029
Fax: 0091 803325615
Email: guru.esa@access.net.in

Ireland

NORAL MICROLOGICS Ltd.
Logic House, Gate Street
Blackburn, Lancashire BB1 3AQ
Tel: (01254) 682092
Fax: (01254) 680847
Email: noral@noral.co.uk

Israel

ITEC Ltd.
P.O.Box 10002
Tel Aviv 61100
Tel: 972-3-6491202
Fax: 972-3-6497661
Email: itec@netvision.net.il

Italy

DELO SYSTEMS
Via Piemonte 14
I-20090 Fizzonasco Pieve E. (MI)
Tel: (02) 90 722 441
Fax: (02) 90 722 742
Email: 100757.2373@compuserve.com

South Africa

Eagle Technology
P.O. Box 4376
Cape Town 8000
Tel: 27-21-23-4943
Fax: 27-21-24-4637

South Korea

DA SAN Technology
#35-26, 3F Hae Sung B/D
Kangnam-Ku, Seoul
Tel: (02) 511-9846
Fax: (02) 511-9845

Spain

CAPTURA ELECTRONICA, SCCL
Edificio Forum de la Tecnol.
E-08042 Barcelona
Tel: (3) 291 76 33
Fax: (3) 291 76 35
Email: cape101@ibm.net

Sweden

Nohau Elektronik AB
Fosievaegen 6
S-21431 Malmoe
Tel: 040-922425
Fax: 040-968161
Email: info@nohau.se

Switzerland

JBERG Datentechnik
Zimmereiweg 2
CH-5734 Reinach
Tel: (062) 7710 886
Fax: (062) 7717 187

Taiwan

Superlink Technology Corp.
9F, 399 Ho Ping East Road
RC-10695 Taipei
Tel: 886-2-705-7090
Fax: 886-2-708-3398
Email: stc@tpts1.seed.net.tw

United Kingdom

NORAL MICROLOGICS Ltd.
Logic House, Gate Street
Blackburn, Lancashire BB1 3AQ
Tel: (01254) 682092
Fax: (01254) 680847
Email: noral@noral.co.uk

USA

Lauterbach, Inc.
945 Concord Street
Framingham, MA 01701
Tel: (508) 620 4521
Fax: (508) 620 4522
Email: info@lauterbach.com
Web: <http://www.lauterbach.com>

TRACE32-ICE

Analyzer, Debugger, Emulator/Simulator, Board

Lauterbach Datentechnik

TRACE32 provides a complete set of tools for testing software and hardware in embedded designs. TRACE32 works a variety of host interfaces. The communication link to the host is fibre optic interface or Ethernet. SCSI, RS232, RS422 and parallel interface are also supported. It is possible to share a TRACE32 in a LAN of PCs and workstations.

The TRACE32-ICE incorporates a revolutionary concept of an universal microprocessor development system. The advanced modularity of TRACE32 makes it very easy to upgrade the system to future needs.

The integrated high-level language debugger with its powerful trigger and trace capabilities supports most third-party compilers for Ada, C, C++, Modula 2 and assembly languages. The analyzer offers selective state trace as well as software performance analysis and statistic functions.

The windowed user interface is completely configurable.

TRACE32 Features

- Same system for different microprocessors and microcontrollers.
- Interface to all host computers also in a heterogeneous LAN.
- High-level language debugger independent of programming language and compiler.
- Multi-task debugger.
- In-circuit emulator.
- Logic state analyzer.
- Timing analyzer.
- BDM interface and debugger.
- EPROM emulator.
- Evaluation boards for test stage.

In-Circuit Emulator Features

- In-circuit emulator for 8-32 bit processors.
- Unlimited hardware breakpoints.
- Up to 16 MByte dual-ported emulation memory.
- Link via Ethernet LAN or fibre optic.
- Up to 4 MFrame trace buffer.
- Real-time trace and trigger up to 66 MHz.
- Integrated high-level language debugger.
- Multi-task debugger.
- Performance analysis/statistic functions.
- Timing analyzer with pattern generator and line tester.

Platforms Supported

- PC Windows
- SCO-ODT
- SUN3, SPARC
- DEC-ULTRIX
- VAX-VMS
- ALPHA-OSF1, ALPHA-VMS
- HP9000/300/400/700
- RS6000 (in preparation)

Third-Party Compilers Supported

- GNU (XCOFF)
- MOTOROLA (XCOFF)
- Diab Data (ELF/DWARF)

PowerPC Microprocessors Supported

- PowerPC 403GA and 403GB processors.

Technical Support

- Local application engineers, technical support hotline, and training.

Availability

- Available now.

Software Generation and Debug Tools (Cross)

Contact

A complete listing of international representatives may be found at www.lauterbach.com/replist.html

Australia

ELEKTRO OPTICS Pty. Ltd
Level 1, Nelson Street
Kenthurst N.S.W. 2156
Tel: (2) 6541873
Fax: (2) 6541539
Email: philmo@electro.oz.au
Web: <http://www.electro.oz.au>

Austria

Nowatron Elektronik GmbH
Eitnergasse 7
A-1230 Wien
Tel: (1) 8658543-0
Fax: (1) 8658543-7

Benelux

TRITEC Benelux B.V.
Antoniuslaan 1
NL-3341 GA Hendrik Ido
Ambacht
Tel: ++31 78 681 61 33
Fax: ++31 78 682 00 30
Email: development-tools@tritec.nl

China

Watertek Inc.
Dongshen electron Building
N. B3 Tucheng West Rd, Haidian
Beijing, P.R. China 100088
Tel: +86-10-2383376
Fax: +86-10-2373872
Email: xjwater@public.bta.net.cn

Denmark

NOHAU Denmark A/S
Naverland 2
DK-2600 Glostrup
Tel: 43446010
Fax: 43446020
Email: nohau-dk@inet.uni-c.dk

Egypt

WANTECH
14 Amin El-Rafie St., Appt. 9
Cairo, Egypt
Tel: (+202) 349-5931
Fax: (+202) 349-5931
Email: wantech@ritsec2.com.eg

France

LOGIC INSTRUMENT
33, Rue des Molleons
F-95230 Soisy Sous Montmorency
Tel: (1) 39899622
Fax: (1) 34280050
Email: 100772.3071@compuserve.com

Germany

Lauterbach Datentechnik GmbH
Fichtenstr. 27
D-85649 Hofolding
Tel: (08104)8943-28
Fax: (08104)8943-49
Email: info@lauterbach.com
Web: <http://www.lauterbach.com>

India

Electro Systems
4215 JK Complex First Main Rd.
Bangalore 560 021 India
Tel: 0091 803 323029
Fax: 0091 803325615
Email: guru.esa@axcess.net.in

Ireland

NORAL MICROLOGICS Ltd.
Logic House, Gate Street
Blackburn, Lancashire BB1 3AQ
Tel: (01254) 682092
Fax: (01254) 680847
Email: noral@noral.co.uk

Israel

ITEC Ltd.
P.O.Box 10002
Tel Aviv 61100
Tel: 972-3-6491202
Fax: 972-3-6497661
Email: itec@netvision.net.il

Italy

DELO SYSTEMS
Via Piemonte 14
I-20090 Fizzonasco Pieve E. (MI)
Tel: (02) 90 722 441
Fax: (02) 90 722 742
Email: 100757.2373@compuserve.com

South Africa

Eagle Technology
P.O. Box 4376
Cape Town 8000
Tel: 27-21-23-4943
Fax: 27-21-24-4637

South Korea

DA SAN Technology
#35-26, 3F Hae Sung B/D
Kangnam-Ku, Seoul
Tel: (02) 511-9846
Fax: (02) 511-9845

Spain

CAPTURA ELECTRONICA, SCCL
Edificio Forum de la Tecnol.
E-08042 Barcelona
Tel: (3) 291 76 33
Fax: (3) 291 76 35
Email: cape101@ibm.net

Sweden

Nohau Elektronik AB
Fosievaegen 6
S-21431 Malmoe
Tel: 040-922425
Fax: 040-968161
Email: info@nohau.se

Switzerland

JBERG Datentechnik
Zimmereiweg 2
CH-5734 Reinach
Tel: (062) 7710 886
Fax: (062) 7717 187

Taiwan

Superlink Technology Corp.
9F, 399 Ho Ping East Road
RC-10695 Taipei
Tel: 886-2-705-7090
Fax: 886-2-708-3398
Email: stc@tpts1.seed.net.tw

United Kingdom

NORAL MICROLOGICS Ltd.
Logic House, Gate Street
Blackburn, Lancashire BB1 3AQ
Tel: (01254) 682092
Fax: (01254) 680847
Email: noral@noral.co.uk

USA

Lauterbach, Inc.
945 Concord Street
Framingham, MA 01701
Tel: (508) 620 4521
Fax: (508) 620 4522
Email: info@lauterbach.com
Web: <http://www.lauterbach.com>

FlashPort™

Analyzer, Code Translator, Disassembler

Lucent Technologies Bell Laboratories

FlashPort translates applications from their binary object code versions that run on one processor to semantically and functionally identical versions that can run on incompatible processors. The initial product offering is a translator for Motorola 680x0 to IBM PowerPC architecture.

FlashPort can translate object code of applications written in assembly language, procedural languages (such as C, Pascal), or a combination of those languages. The translation does not require access or changes to the application's source code. Software developers can translate most compiled code automatically in a few days. However, applications generated from assembly code generally require more human intervention, and they can be translated in a few weeks. The degree of human intervention depends on factors such as the number of deviations from typical programming practices or platform-specific functions.

In addition to producing executable code for the target processor, FlashPort produces a complete disassembly and analysis of the input source program. From this analysis, FlashPort generates call graphs, flow graphs, data dependency, and code-reach reports.

FlashPort also supports migration of software from IBM System 360, 370 and 390 (and equivalent) machines to modern platforms, including PowerPC.

Features

- *Single Source Code Base*—Allows users to maintain one source code base during the transition from 68K to the Power, greatly reducing the cost and resources associated with creating and maintaining separate code bases for multiple architectures.
- *Time-to-Market and Managed Investment*—Allows the user to achieve the time-to-market benefits of quickly moving to new platforms, while minimizing the up-front investment of a traditional porting effort.
- *Power Performance*—Code translated with FlashPort provides performance levels near that of hand-ported code conducted by highly skilled engineers.
- *Maintainable Code*—Duplicates the debug and symbolic information from the input binary file to the translated binary. Also creates an assembly listing that is assembled by the PowerPC assembler, providing its associated debugging facilities.
- *Significant Cost Savings*—FlashPort allows migration of any application (even legacy software) off expensive platforms, producing immediate cost savings.
- *Incremental Migration*—FlashPort allows mixing of native compiled code and FlashPorted code on the target platform.
- *Multiple Platforms*—FlashPort targets code to run on multiple machines.
- *Architecturally Neutral Representation*—Creates an architecturally neutral representation of the input program in an intermediate language, making it possible to quickly and easily re-target subsequent platforms.

Software Generation and Debug Tools (Cross)

Technical Support

- *Professional Support*—In addition to providing FlashPort translation service, Lucent offers a full complement of migration, maintenance, training, and consulting services to aid in the migration process.

Availability

- Available now.

Contact

Lucent Technologies Bell Laboratories

S. Shastry, Department Head
943 Holmdel Road
Holmdel, NJ 07733
Tel: (908) 946-1140
Fax: (908) 946-9146

High C/C++™ PowerPC Embedded Development Toolset

Compiler, Debugger, Real-Time Tool, Utilities

MetaWare Incorporated

High C/C++ PowerPC Embedded Development Toolset provides essential tools and enabling technology for creating high-performance, efficient embedded-system applications for the entire family of PowerPC processors from IBM and Motorola.

The toolset includes a compiler, linker, and assembler, along with MetaWare's fast, ANSI-compliant libraries.

MetaWare's meticulous attention to the evolving ANSI C++ standard gives you cross-platform compatibility and predictability. MetaWare's long-term development strategy is to provide compatibility between the High C/C++ Toolset and the leading real-time operating systems, debuggers, and emulators. This open systems approach to embedded application development will shorten time-to-market cycles as well as development time.

Compiler

The High C/C++ compiler is a true compiler, not a C-to-C++ translator. Our "Incremental Strengths" feature lets you specify the level of C++ compilation, allowing migration from C to C++ in stages. The compiler supports big- and little-endian addressing, while producing ELF object and DWARF debug record formats.

Linker and Utilities

The linker can quickly integrate a group of separately compiled or assembled modules and a collection of object modules contained in libraries into an ELF executable, in which all references between modules are resolved.

A set of utilities is provided to work with the output files produced by the toolset. The utilities allow the user to prepare output files for downloading into target systems and to create ROM images.

Optimizing Your Code

High C/C++ supports the following advanced optimization techniques:

- Global register allocation by graph coloring.
- Global common subexpression elimination.
- Global copy propagation.
- Elimination of loop invariants.
- Induction variable analysis/strength reduction.
- Dead code elimination.
- Function inlining.
- Loop unrolling.
- Static branch prediction.
- Small-data sections for fast access of global data.
- Strong PowerPC-processor-specific code generation using load/store updates, decrement branching, and static branch predictions.

Embedded Programming Features

MetaWare supports the following features for the embedded programmer:

- Reversed endianness.
- Hex record support.
- Complete run-time library source distribution.
- Pragmas to control text and data displacement.
- Position-independent code.
- Linker command file for section layouts.
- ROMable code and constant data.

High C/C++ makes it easy for you to deal with endian-dependent data, with a feature that automatically converts data from one endian format to the other.

Debugger

MetaWare's toolset is compatible with the SDS SingleStep Debugger.

Functional Summary

- ANSI compliance and verification for C and the emerging C++ standards assures code compatibility with current and future application code.
- Support for load scheduling, delayed branch, and many other optimizations which are tightly coupled to the processor architecture to promote fast code execution.
- Big- and little-endian addressing.
- ELF and DWARF support.
- Eight levels of global optimization offer hundreds of optimizations to customize compilations to meet the unique requirements of any application.
- Extensive and scalable error/warning messages shorten the develop/debug cycle by pinpointing problem areas and even recommending remedies.
- Wide variety of compiler features available through use of toggles, pragmas, and command-line options.
- Native and emulated floating-point code generation.
- C or C++ compiler invoked based on user-definable source-file extension.

- Lint-like checking.
- Source-annotated assembly listings.
- Inline functions substituted across compilation units speeds up execution of compiled code.
- No restriction on complexity of inlined functions.
- Macro assembler and linker-archiver.
- Place code or data in specific locations for embedded application efficiency.
- Adjustable external naming conventions to agree with linkers and operating systems.

Supported Hosts

- IBM RS/6000 running AIX 3.25.
- SPARCstation or equivalent running SunOS or Solaris 2.1.
- 386, 486, Pentium running DOS or Windows 3.1, Windows 95.
- HP-PA-RISC running HP-UX 9.1.

Technical Support

- Help desk staffed by experienced support engineers.
- Annual support contracts are available.
- On-line, call-in bulletin board.
- Internet e-mail.
- World Wide Web FTP site.

Availability

- Available now.

Contact

MetaWare Incorporated

MetaWare Incorporated
2161 Delaware Avenue
Santa Cruz, CA 95060-5706
Tel: (408) 429-6382
Fax: (408) 429-9273
Email: techsales@metaware.com
Web: <http://www.metaware.com>

PortAsm™

Code Translator

MicroAPL™ Ltd.

PortAsm comes in two versions, PortAsm/68K and PortAsm/86, that respectively convert 680x0 and 80x86 assembly-language code into efficient, optimized, and maintainable PowerPC assembly-language code. They can be used either for applications written wholly in assembler, or for translating the assembler portions of applications written partly in assembler and partly in a high-level language such as C or Pascal. PortAsm/68K and PortAsm/86 can also be used to help port system-level code and drivers.

Each PortAsm product analyzes the original source code, and separates the semantic meaning of 680x0 or 80x86 instruction sequences from irrelevant side-effects such as unnecessary condition code updates. After expanding macros and tokenizing the source file, PortAsm/68K and PortAsm/86 respectively:

- Examine the 680x0 or 80x86 instructions in detail, analyzing content and program flow.
- Map 680x0 or 80x86 registers onto PowerPC registers, optimizing over blocks of code.
- Replace 680x0 or 80x86 instruction sequences with efficient PowerPC-processor equivalents.
- Reproduce only the required behavior of the 680x0 or 80x86 code, eliminating irrelevant side effects.
- Adapt the code to fit into the target runtime environment.
- Generate interface glue for calls to and from native high-level code.
- Output a translated PowerPC source file, optionally retaining comments.
- Optionally output additional debugging directives.

Features

- Produces easy-to-read PowerPC assembler source code that uses the original symbolic labels and variable names.
- Retains the original assembly code in the output file as comments, making the translation process transparent and aiding debugging (the original comments may also be retained).
- Can include hand-written PowerPC assembler in the original 680x0 (PortAsm/68K) or 80x86 (PortAsm/86) source which with conditional assembly directives makes it easy to maintain a single source base for 680x0 or 80x86 and PowerPC-processor targets.
- Powerful code generation optimizations can be selectively enabled or disabled.
- Automatic generation of interface glue for calling out to or being called from native C or Pascal code.
- Integrates into the standard build process for easy code maintenance after the initial port.
- Supports source-level debugging, using the original assembly code as source, making debugging very simple even if you have little PowerPC assembler knowledge.
- PortAsm/86 translates both 16-bit and 32-bit 80x86 code, automatically handling segmentation issues.
- PortAsm/86 is supplied with the source code to DABI, an extendable library which implements parts of the MS-DOS programming interface on the target system.

Software Generation and Debug Tools (Cross)

Supported PowerPC Target Assemblers

- IBM 'as'.
- Motorola 'pas'.
- Metaware 'asppc'.
- Apple 'ppcAsm'.
- Diab Data 'das'.

Supported Runtime Environments

- EABI/ELF standard for embedded applications (with DWARF debugging).
- XCOFF-format (AIX, MacOS, and PowerOpen compatible).
- SVR4/ELF standard (Solaris, OS/2).
- Windows NT for PowerPC.

Supported Development Environments

- IBM RISC System/6000 under AIX.
- MS-DOS.
- MacOS (MPW and Metrowerks CodeWarrior).
- Sun SPARC under Solaris and SunOS.

Availability

- Available now.

Contact

MicroAPL Ltd.

South Bank Technopark
90 London Road
London SE1 6LN, UK
Tel: +44 171 922 8866
Fax: +44 171 928 1006
Email: microapl@microapl.demon.co.uk
Web: <http://www.microapl.co.uk>

Microsoft® Visual C++®

Compiler, Debugger, Libraries, Utilities

Microsoft Corporation

The Microsoft Visual C++ development system version 4.0 provides many tools to help you accelerate application development, including:

- Component Gallery
- Microsoft Developer Studio
- Microsoft Foundation Class (MFC)
- Microsoft Visual C++ Professional Subscription

The Visual C++ Cross-Development Edition for Macintosh is available separately as an add-on to Visual C++.

C++ Implementation

Microsoft Visual C++ provides complete C++ language features:

- C++ Namespaces.
- C++ RTTI.
- C++ templates.
- C++ exceptions and Win32 structured exception-handling.
- Includes the HP® standard template library (STL).
- Debug version of the C run-time library, including source.

Component Gallery

The Component Gallery is a one-stop location for you to store and manage your reusable components, including C++ classes, OLE controls, and dozens of other third-party components that enable you to quickly add advanced features.

Microsoft Developer Studio

The Microsoft Developer Studio provides:

- A common environment for Visual C++, Visual Test, MSDN Library, and Visual SourceSafe.
- ClassView—a background no-compile browser integrated with the Project Workspace.
- Project Workspace integrates classes, files, documentation, and resources into one work area.
- Customizable toolbars, keyboard shortcuts, and tools menu.
- Property pages give you at-a-glance information on every element of your project.
- ToolTips and status bar hints provide instant information on user-interface elements.

Microsoft Foundation Class (MFC)

MFC 4.0 provides the following new functions:

- Directly accesses the built-in Microsoft Jet 3.0 database engine using DAO classes.
- Set up and use workspaces, create and manipulate tables and queries, and use and create indexes for those tables by using the SQL Data Definition Language (DDL).
- Access ODBC data sources through attached tables.
- CSyncObject and derived objects encapsulate common synchronization techniques.
- Create ActiveX controls and control containers.

Visual C++ Professional Subscription

Microsoft Visual C++ Professional Subscription includes these services:

- Receive three additional releases of Visual C++, including major releases as they become available during your subscription year.
- Latest tools and information include new components, ActiveX controls, sample code, recent Visual C++ and MFC technical notes, and updated on-line documentation.

Cross-Development Edition

The Visual C++ Cross-Development Edition for Macintosh and Power Macintosh is available separately as an add-on to Visual C++ 4.0. It enables a single set of source code to target both a Windows-based computer and the Macintosh when written to either the Microsoft Foundation Class library or the Win32 API.

- *Windows 95 or Windows NT host*
 - 486 or higher processor running Windows 95 or Windows NT Workstation version 3.51 or later.
 - Microsoft Visual C++ version 4.0.
 - 16 MB memory (20 MB recommended).
 - 70 MB hard-disk space required for Power Macintosh-based development.

- CD-ROM drive.
- VGA or higher-resolution monitor.
- Microsoft Mouse or compatible pointing device.
- Ethernet hardware supporting an Ethernet AppleTalk® or TCP/IP network connection between the PC and Macintosh. (TCP/IP network or serial cable required for Windows 95 hosts.)
- *Macintosh target (during development)*
 - A Macintosh or Power Macintosh running System 7.0 or later (System 7.5 highly recommended).
 - 8 MB of memory (16 MB recommended).
 - 20 MB hard-disk space required for Macintosh development.
 - A CD-ROM drive.
 - Ethernet hardware supporting an Ethernet AppleTalk® or TCP/IP network connection between the PC and Macintosh. (TCP/IP network or serial cable required for Windows 95 hosts.)

Availability

- Available now.

Contact

Microsoft Corporation

One Microsoft Way
Redmond, WA 98052-6399
Tel: (800) 719-5577
Web: <http://www.microsoft.com/visualc>

Optimizing C/C++ Compilers

Compiler, Debugger, Utilities

Microtec

Microtec's C/C++ compiler, assembler, linker and front end technology combined with Apogee Software, Inc.'s RISC optimization technology provides an advanced PowerPC compiler solution. Apogee's industry-proven proprietary optimization technology has been licensed by major RISC systems makers such as Silicon Graphics, Motorola, and others.

This advanced optimization technology transforms compiled programs to minimize the number of computations when these programs are running on a target processor. Further performance improvements are achieved by scheduling instructions generated for each compiled program to maximize the utilization of the fine-grained parallelism of a PowerPC microprocessor. The Microtec compiler also efficiently allocates hardware registers to reduce the number of times compiled programs must access memory, thus alleviating the memory bandwidth bottleneck. In addition, the compiler takes advantage of the multi-stage pipeline, multiple issue of instructions, large number of registers and multiple functional units of the PowerPC microprocessor to obtain the highest possible performance.

Features

- Versatile and flexible language conformance
- Migration support
 - K&R C, ANSI C (strict and relaxed modes).
 - C++ 2.0/2.1/3.0/Annotated Reference Manual.
- Debugging optimized code.
- High run-time performance and fast compile time.
- EABI compliant.

General Compiler Features

The Microtec PowerPC compilers give you extensive control over the compilation process. Some controllable aspects of compilation are:

- Optimization: Six levels of control. Each type may be individually controlled, usually within several different levels.
- Diagnostic and error reporting.
- Zero-trip vs. one-trip treatment of loops.
- Stack vs. static treatment of local variables.
- .data vs. .bss treatment of uninitialized data.
- Printing of compiler progress.
- Printing of intermediate representations.
- Control of memory utilization.
- C/C++ language extensions for embedded language programming (i.e. extended asm() and packed).
- Integration with XRAY MasterWorks with advanced C/C++ debugging capability.

Optimizations

- Global and local constant propagation (repeated until all possible higher order indirect propagations are done).
- Constant folding.
- Global and local common subexpression elimination including partially redundant expressions.
- Global and local copy propagation.
- Useless and unreachable (dead) code elimination, including elimination of useless loads and redundant loads and stores.
- Global backward code motion (hoisting).
- Global forward code motion, including stores.

Software Generation and Debug Tools (Cross)

- Extensive strength-reduction and reassociation in nested loops of all levels, including loops with complex control flow (i.e. multiple exits, irreducible loops).
- Induction variable elimination.
- Interprocedural memory-reference alias analysis.
- Interprocedural call-effect analysis.
- Interprocedural register allocation.
- User procedure inlining.
- Control-flow optimizations (repeated iteratively).
- Loop unrolling.
- Variables may be resident in registers.
- Global register allocation using priority-based coloring.

- Scheduling specific to the target machine instruction pipeline.
- Delayed-branch filling.

Debug Information

- Advanced C++ debugging—Class/Object breakpoints, overloaded breakpoints.

Hosts Supported

- Sun SPARCstations.
- HP9000-700 workstations.

Availability

- Available now for PowerPC 603 and 604 target platforms.

Contact

Microtec

2350 Mission College Blvd
Santa Clara, CA 95054
Tel: (408) 980-1300
Toll Free: (800) 950-5554
Fax: (408) 982-8266
Web: <http://www.mri.com>

Chicago

Mentor/Microtec
Tel: (847) 605-0230
Fax: (847) 605-8535

Orlando

Phone: (407) 240-1130
Fax: (407) 240-4840

Domestic Offices

Nashua, New Hampshire
Tel: (800) 933-3036
Fax: (603) 891-3193

Winter Park

Tel: (407) 677-9661
Fax: (407) 677-1972

Maryland

Tel: (301) 921-1990
Fax: (301) 921-1994

Irvine

Mentor/Microtec
Tel: (714) 453-2500
Fax: (714) 453-2520

New York

Tel: (516) 244-1497
Fax: (516) 563-1225

San Diego

Mentor/Microtec
Tel: (619) 597-1530
Fax: (619) 554-0023

Connecticut

Tel: (860) 648-0681
Fax: (860) 648-1143

San Jose

Mentor/Microtec
Tel: (408) 436-1500
Fax: (408) 451-5680

Dallas

Mentor/Microtec
Tel: (214) 450-2300
Fax: (214) 991-0706

International Offices

Microtec Ltd.-England
Tel: +44.1256 707784
Fax: +44.1256 707786

*Microtec GmbH-
Germany*

Tel: (49) 089 609 00 81
Fax: (49) 089 609 96 59

Microtec S.A.-France

Tel: (33) 1-30-12-02-10
Fax: (33) 1-30-12-02-20

Microtec AB-Sweden

Tel: +46-8-744 53 00
Fax: +46-8-645 53 36

Microtec-Italy

Tel: 39-2-33-21-71
Fax: 39-2-39-00-25-00

Microtec-Israel

Tel: 972-9-552636
Fax: 972-9-552627

*Nihon Microtec, K.K.-
Japan*

Tel: (81) 3-5210-3050
Fax: (81) 3-5210-3180

*Nihon Microtec, Kansai
Japan*

Tel: (81) 6-359-1620
Fax: (81) 6-359-1625

Hankuk Microtec-Korea

Tel: (82) 2-517-0838
Fax: (82) 2-517-0839

China Microtec- Beijing

Tel: (86) 10-6202-2744
Fax: (86) 10-62020135

Microtec-Taiwan

Tel: 886-2-7576020-5
Fax: 886-2-7576027

*Microtec- Australia/New
Zealand*

Tel: 61-2-413-4600
Fax: 61-2-413-4622

XRAY Debugger

Debugger, Real-Time Tool

Microtec

The XRAY Debugger operates on C++, ANSI C, or assembly application code letting you completely control and monitor the flow of program execution. The XRAY Debugger displays multiple windows simultaneously for quick analysis of different views of the target system. When used with Microtec's compilers, the XRAY Debugger allows non-intrusive debugging of optimized, production-quality code.

Unique to XRAY Debugger is its ability to provide single stepping through optimized code. A powerful command language also provides simple and complex breakpoint setting, code patching, and continuous variable monitoring.

The XRAY Debugger also provides a powerful high-level macro language. Macros consisting of ANSI C and C++ statements, expression, and debugger commands can be composed either within the XRAY Debugger environment, the XRAY MasterWorks integrated C and C++ development environment, or externally using your favorite text editor.

The debugger supports multiple execution environments including instruction set simulator and real-time operating systems so that you only need to learn one interface from beginning to end.

Software Generation and Debug Tools (Cross)

Features

- Debugs ANSI C, C++, and assembly languages.
- Source-level debugging of optimized code.
- Supports multiple execution environments, including simulator for early prototyping.
- Integrated with Microtec compiler package and XRAY MasterWorks productivity package.

Hosts Supported

- Sun workstations
- HP9000-700 workstations.

Availability

- Available now for PowerPC 603 and 604 microprocessors.

Contact

Microtec

2350 Mission College Blvd
Santa Clara, CA 95054
Tel: (408) 980-1300
Toll Free: (800) 950-5554
Fax: (408) 982-8266
Web: <http://www.mri.com>

Domestic Offices

Nashua, New Hampshire
Tel: (800) 933-3036
Fax: (603) 891-3193

Maryland

Tel: (301) 921-1990
Fax: (301) 921-1994

New York

Tel: (516) 244-1497
Fax: (516) 563-1225

Connecticut

Tel: (860) 648-0681
Fax: (860) 648-1143

Dallas

Mentor/Microtec
Tel: (214) 450-2300
Fax: (214) 991-0706

Chicago

Mentor/Microtec
Tel: (847) 605-0230
Fax: (847) 605-8535

Orlando

Phone: (407) 240-1130
Fax: (407) 240-4840

Winter Park

Tel: (407) 677-9661
Fax: (407) 677-1972

Irvine

Mentor/Microtec
Tel: (714) 453-2500
Fax: (714) 453-2520

San Diego

Mentor/Microtec
Tel: (619) 597-1530
Fax: (619) 554-0023

San Jose

Mentor/Microtec
Tel: (408) 436-1500
Fax: (408) 451-5680

International Offices

Microtec Ltd.-England
Tel: +44.1256 707784
Fax: +44.1256 707786

Microtec GmbH-Germany

Tel: (49) 089 609 00 81
Fax: (49) 089 609 96 59

Microtec S.A.-France

Tel: (33) 1-30-12-02-10
Fax: (33) 1-30-12-02-20

Microtec AB-Sweden

Tel: +46-8-744 53 00
Fax: +46-8-645 53 36

Microtec-Italy

Tel: 39-2-33-21-71
Fax: 39-2-39-00-25-00

Microtec-Israel

Tel: 972-9-552636
Fax: 972-9-552627

Nihon Microtec, K.K.-Japan

Tel: (81) 3-5210-3050
Fax: (81) 3-5210-3180

Nihon Microtec, Kansai Japan

Tel: (81) 6-359-1620
Fax: (81) 6-359-1625

Hankuk Microtec-Korea

Tel: (82) 2-517-0838
Fax: (82) 2-517-0839

China Microtec- Beijing

Tel: (86) 10-6202-2744
Fax: (86) 10-62020135

Microtec-Taiwan

Tel: 886-2-7576020-5
Fax: 886-2-7576027

Microtec- Australia/New Zealand

Tel: 61-2-413-4600
Fax: 61-2-413-4622

Ultra C/Ultra C++

Compiler, Debugger, Real-Time Tool

Microware Systems Corporation

Microware's Ultra C and Ultra C++ are advanced technology compilers for the OS-9[®] real-time operating system. Ultra C and Ultra C++ incorporate a revolutionary compiler design with state-of-the-art optimization techniques to extract maximum performance from modern 16-, 32-, and 64-bit CISC and RISC microprocessors, including the PowerPC microprocessors. Ultra C and Ultra C+ are the result of concentrated effort devoted to creating compilers whose trademark is world-class performance. Ultra C and Ultra C++ offer the level of performance required for today's hard real-time applications in avionics, imaging, process control, robotics and telecommunications.

By utilizing the latest advances in compiler optimization strategies, Ultra C and Ultra C++ produce fast, tight code that delivers the throughput and reliability needed for mission-critical systems.

Advanced Architecture

Unlike traditional compilers that translate source code into microprocessor-specific assembly language, Ultra C's and Ultra C++'s front-end modules compile source code into an intermediate code (I-code) format that is independent of the source language and target microprocessor.

The I-code representation of the program can then be linked against C, C++, OS and user libraries to generate an I-code image of the entire application. This file is processed by an I-code optimizer that performs various optimizations, as specified by the user.

In the last stages of compilation, Ultra C's and Ultra C++'s back-end modules translate the optimized I-code file into assembly

language for the target microprocessor. This code is further optimized, assembled and linked into an executable module.

The benefits of this modular architecture are numerous. Linking and optimizing at the I-code level allows Ultra C and Ultra C++ to perform true interprocedural optimization over the entire application, resulting in much faster and typically smaller executables.

The compilers' design also gives Ultra C and Ultra C++ the flexibility to support alternative front-end language modules, new optimizations that can be added once to the I-code optimizer to benefit all supported languages and processors, and additional back-end assembly generators to target new families of microprocessors. This assures compatibility and familiarity for OS-9 applications across CISC- and RISC-based systems.

Leading Edge Optimizations

Ultra C's and Ultra C++'s performance exceed traditional compilers by using the latest optimization strategies developed in academic and industry forums. The majority of optimization techniques are applied over the entire application, rather than on just a file-by-file basis.

Full ANSI Compliance

The Ultra C compiler system and supporting libraries fully conform with the ANSI X3J11 1989 and ISO/IEC 9899:1990 specifications for the C programming language.

Ultra C's ANSI conformance was validated using the Plum Hall ANSI C Validation Suite Version 6.0. Validation against this suite assures complete portability of ANSI C source

Software Generation and Debug Tools (Cross)

code between OS-9 and other computing platforms. Ultra C++ is tracking ANSI X3J16 draft.

Features

- Next-generation architecture.
- Incorporates latest optimization strategies.
- Fully compliant with the ANSI X3J11 and ISO/IEC 9899:1900 C language standards.
- Tracking ANSI X3J16 draft for C++.
- Backward compatible with OS-9 C v3.2.
- Validated with the Plum Hall ANSI C Validation Suite.

- Produces highly-optimized, compact, ROMable binaries.
- Full C/C++ source-level debugging.
- Resident versions for OS-9, cross versions for UNIX and PC.

Software Requirements

- OS-9

For information on UNIX and PC cross-development platforms, contact Microware.

Availability

- Available now.

Contact

United States

Microware Systems Corporation
Corporate Headquarters
1900 N.W. 114th Street
Des Moines, IA 50325-7077
Tel: (515) 224-1929
Fax: (515) 224-1352
Email: info@microware.com
Web: <http://www.microware.com>

Western Regional Office
2055 Gateway Place,
Suite 400
San Jose, CA 95110
Tel: (408) 451-3999
Fax: (408) 451-3998

Northeastern Regional Office
One Crank Road
Hampton Falls, NH 03844
Tel: (603) 929-4107
Fax: (603) 929-4233

Southeastern Regional Office
2611 N.E. 6th Street
Pompano Beach, FL 33062-4926
Tel: (305) 946-9280
Fax: (305) 946-9350

South Central Regional Office
Great Hills Corporate Center I
Suite 220
9020 Capital of Texas Highway North
Austin, TX 78759
Tel: (512) 794-0247
Fax: (512) 794-0251

United Kingdom

Microware Systems (U.K.) Limited
Beech Court
27/33 Summers Rd
Burnham SL1 7EP
United Kingdom
Tel: (44) 1628 667578
Fax: (44) 1628 667579

France

Microware Systems France
Chateau de la Saurine
Pont de Bayeux
13590 Meyreuil, France
Tel: (33) 42.58.63.00
Fax: (33) 42.58.62.28

Japan

Microware Systems K.K.
17-3, Sotokanda 2-Chome
Chiyoda - Ku
Tokyo 101, Japan
Tel: (81) 3-3257-9000
Fax: (81) 3-3257-9200

Germany

Dr. Rudolf Keil, GmbH
Gerhart-Hauptmann-Str.30
D-69221 Dossenheim
Germany
Tel: (49) 6221-862091
Fax: (49) 6221-861954

Switzerland

Elsoft AG
Tafernstr. 20
5405 Baden - Dattwil
Switzerland
Tel: (41) 56-83-3377
Fax: (41) 56-83-3020

Australia

Microprocessor Consultants Pty. Ltd.
23 Norma Road
Palm Beach 2108
NSW Australia
Tel: (61) 2-974-4917
Fax: (61) 2-974-4900

Motorola C/C++ SDK PowerPC Edition for MacOS

Compiler, Debugger, Libraries, Utilities

Motorola, Inc.

The Motorola C/C++ SDK, PowerPC Edition for Mac OS produces optimized applications from within today's most popular development environments. The Motorola compilers are available as a full SDK that includes C/C++ compilers for Apple Macintosh Programmer's Workshop (MPW[®]), Symantec Project Manager and Metrowerks CodeWarrior, a complete MPW environment, and the Kuck & Associates preprocessor (KAP for C). They are also available as C/C++ "plug-in" compilers for the Metrowerks CodeWarrior and Symantec Project Manager development environments.

The Motorola C/C++ SDK delivers world-class code optimization for any specific PowerPC microprocessor, while ensuring compatibility across the entire PowerPC family of microprocessors.

Features

- ANSI-compliant C/C++ front-end.
 - Apple language extensions.
 - Full integration with Apple MPW, Metrowerks CodeWarrior, and Symantec Project Manager.
 - Kuck & Associates Preprocessor (MPW only).
 - Assembly and XCOFF code generation.
 - Separate assembler provides translation of assembly code to XCOFF object code.
 - Integration with Apple's source-level PowerPC debugger.
 - Hosted natively on Power Macintosh™ or compatible systems.
- PowerPC optimization:
 - Superscalar instruction scheduling.
 - Register allocation and renaming.
 - Branch prediction and branch acceleration.
 - Cache and memory hierarchy.
 - Specific optimizations for each 32-bit PowerPC microprocessor.
 - Global optimization:
 - Local and global common subexpression elimination.
 - Priority-based graph coloring register allocation.
 - Software pipelining.
 - Loop unrolling.
 - Constant and copy propagation.
 - Aggressive load/store removal.
 - Interprocedural analysis and optimization.
 - Function inlining capability.
 - Execution profile feedback mechanism.
 - Customization:
 - Complete set of command-line options.
 - Different optimization levels.
 - Control variables and variable groups.
 - Internal flags for controlling intermediate debugging trace generation.
 - Diagnostic messages (can be disabled).

Software Generation and Debug Tools (Cross)

Contents of Full SDK

- Motorola C/C++ compilers for MPW.
- CodeWarrior and Symantec Project Manager C/C++ plug-in compilers.
- LIBMOTO—Motorola's highly optimized math and string routines for PowerPC-based systems.
- Kuck & Associates Preprocessor for MPW (KAP for C).
- Motorola portable assembler (pas).
- Apple MPW environment & tools including:
 - Linker.
 - Source-level debugger.
 - Libraries.
- Hardcopy documentation.

Contents of Plug-In Kit

- CodeWarrior and Symantec Project Manager C/C++.
- LIBMOTO—Motorola's highly optimized math and string routines for PowerPC-based systems.
- Online documentation.

Devices Supported

- All 32-bit PowerPC microprocessors.

Hosts Supported

- Apple Power Macintosh or compatible systems.

Technical Support

Full-time technical staff provides support via voice, fax and Internet:

- ppcinfo@risc.sps.mot.com
- <http://www.mot.com/PowerPC/>
- 1-800-347-8384 voice

Availability

- Available now.

Contact

Motorola, Inc.

For additional information, call 1-800-347-8384 or
Tel: 512-891-2999
Fax: 512-891-3798
Email: ppcinfo@risc.sps.mot.com
Web: <http://www.mot.com/PowerPC/>

ENVY®/*Embedded* Smalltalk

Compiler, Debugger, Libraries, Utilities
Object Technology Inc.

ENVY/*Embedded* Smalltalk is an object-oriented collaborative software engineering environment designed for complex embedded systems development. It provides a complete solution for developers of complex embedded systems.

ENVY/*Embedded* Smalltalk is an object-oriented development environment based on Smalltalk. Teams of programmers can use ENVY/*Embedded* Smalltalk to achieve high productivity without sacrificing quality.

ENVY/*Embedded* Smalltalk includes extensive class and component libraries which help programmers quickly bootstrap new application development efforts, and which provide support for graphics, user interfaces, standard data types and communications.

Applications can be ROMed or integrated with commercially-available real-time operating systems (RTOS) or targeted for bare metal when a full-featured RTOS is not required.

Real, industrial-strength commercial systems are being shipped today, based on OTI's ENVY/*Embedded* Smalltalk object-oriented environment:

- Telecommunications
- Oscilloscopes
- Command and control systems
- Protocol testers
- LAN analyzers
- Automated test equipment (ATE)
- Hand-held maintenance terminals
- Computer-integrated factories
- Process control systems
- Voice mail

Features

ENVY/*Embedded* Smalltalk includes these tools:

- ENVY/*Smalltalk*—A lean and robust implementation of Smalltalk.
- ENVY/*Developer*—A team-programming support tool.
- ENVY/*XD*—A cross-development tool.
- ENVY/*Stats*—Execution profiling and memory analysis tools.

ENVY/*Smalltalk*

ENVY/*Smalltalk* is OTI's standards based, multi-platform Smalltalk 32-bit virtual machine. It supports portable OSF X/Motif GUIs as well as "headless" configurations. ENVY/*Smalltalk* supports up to four gigabytes of object space and includes a configurable, high-speed scavenging garbage collector.

ENVY/*Smalltalk*'s virtual machine architecture insulates the application from changes in the underlying operating system and hardware, and enhances portability. Once the virtual machine has been ported, Smalltalk source code, or even complete images, can be run immediately on the new system.

ENVY/*Smalltalk* runs on bare hardware or with an underlying RTOS. When an RTOS is used, user primitives provide full access to the underlying OS services.

ENVY/*Smalltalk* offers a modern, multi-threaded process model with priorities and round-robin scheduling. Users can subclass or modify process-scheduler source-code to implement alternative scheduling algorithms.

Software Generation and Debug Tools (Cross)

ENVY/Developer

ENVY/Developer provides team programming support, component management and version control and is the defacto standard for Smalltalk programmers. Integration with ENVY/Developer provides the multi-user team programming facilities required for large software engineering projects. ENVY/Developer's managed component architecture reduces the need for new code development by encouraging software manufacturing from reusable components.

ENVY/XD

ENVY/XD is a cross-development tool providing run-time packaging facilities to generate Smalltalk images, remote debugging of images executing on the target platform, and management of multi-platform Smalltalk images via LANs or communications links.

ENVY/Stats

ENVY/Stats provides execution profiling and memory analysis tools that accumulate execution-time statistics on applications. In addition to reporting time spent in various methods, the profiler reports the number of scavenges and full garbage collections that occurred during the profile. It also provides tools to statistically and dynamically profile object memory.

Benefits

The entire ENVY/Embedded Smalltalk development environment can run in-target for debugging and testing on production

hardware. On smaller targets, a remote interface/debugging facility provides the graphics and I/O services required for target systems with limited I/O devices.

Applications can be modeled, developed and tested on a host before the target hardware is even available. Requirements for expensive instrumented target systems can be minimized where target resources permit.

ENVY/Embedded Smalltalk supports incremental development. Programmers can grow programs one small piece at a time, trying out alternative implementations as they go.

Garbage collection effectively eliminates memory management errors, and uses only about 3% of the CPU time in a typical interactive application. If desired, time-critical functions can be implemented in assembler or C, and the garbage collector is guaranteed not to run during their execution.

Hosts Supported

- Windows 3.11, Windows NT, Windows 95
- OS/2
- AIX 4.1.x
- Solaris 2.5
- HP 9.x

Target Processors

- PowerPC 400-family embedded controllers.

Availability

- Available now.

Contact

Object Technology Inc.
301 East Bethany Home Road
Suite A-100
Phoenix, AZ 85012

Tel: (602) 222-9519
Fax: (602) 222-8503
Email: kim_clohesy@oti.com
Web: <http://www.oti.com>

Rational Ada, C, C++

Compiler, Debugger, Emulator/Simulator, Libraries, Utilities

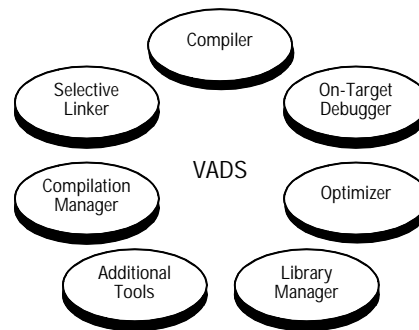
Rational Software Corporation

VADScross is an integrated environment for developing, debugging, testing, and tuning your embedded real-time applications. Our mature optimizing Ada compiler provides full support for Ada machine code insertions, address clauses, and record representations. Our common object module formats, optimizers, code generators, cross-linker, and analysis tools make mixed-language programming simple. VADS, whether used on self-hosted systems or embedded systems, has the same look, feel, and programming model. This simplifies host-based testing and minimizes retraining. Rational also offers a host-based instruction set simulator, VADSSim, entirely compatible with our compiler, cross linker, and debugger. This environment is the ultimate in host-based testing and development.

The VADS Motif-based symbolic cross-debugger allows debugging of your optimized application without recompilation of your source code. VADS keeps symbolic and semantic information external to the linked image. This enables the host-based debugger access to all the information needed to debug any program, optimized or not, without slowing down links or taking up valuable space on your target system. Because VADScross includes a configurable ROMable debug monitor, your debugger connection is simple, even with custom hardware. The debugger transparently supports other target connections, such as ethernet, and in future releases, emulators, ROMulators, and hardware background debugging modes.

The build manager ensures automatic efficient rebuilds of your Ada applications, without makefiles. The VADS cross-linker automatically eliminates unreferenced

subprograms and data. It also allows you to position your program sections in the memory locations you choose. You have the capability of including C, C++, and assembly code in your application. Rational provides Ada compatible ANSI C compilers and standardized C++ compilers for embedded systems.



Features

- Industry Leading Application Development System
- Ada Build Management
- Performance Analysis
- High-performance User-Configurable Runtime System
- Motif-based Symbolic Debugging
- Embedded Networking and Filesystem Capable
- Convenient Mixed-language programming
- Host-based Instruction Set Simulation

Software Generation and Debug Tools (Cross)

The VADScross runtime system, included at no extra charge, is scalable and high-performing for real-time applications. Users have access to mailboxes, semaphores, and passive tasking optimizations. Users have full control over time-slicing, task priority, preemption control, and the use of interrupt service routines. The compiler and debugger are also compatible with third-party runtime systems, such as VxWorks from Wind River Systems, if your runtime requirements are more extensive.

Coverage analysis, performance profiling, program tracing, embedded networking, embedded Filesystem, and configuration management facilities are all available and integrated with the VADScross environment.

VADS is already proven on large applications of over a million lines of code. Developers are building mission critical systems of all kinds using the VADScross toolset and runtime system. For embedded applications large and small, VADScross is a practical solution for delivering your system in a timely and low-risk fashion.

Hosts Systems Requirements

VADScross is available from most UNIX workstations, including Sun, HP, DEC, and IBM.

Target Processors

VADScross is currently available for PowerPC 603, 604, and 403 microprocessors.

Technical Support

Rational provides technical support for all the VADScross products. Support includes telephonic hotline support, updates for bug fixes, updates for OS upgrades, and updates for enhanced features.

Availability

- Available now.

Contact

United States

Rational Software Corp.
2800 San Tomas Expy
Santa Clara, CA 95051-0951
Tel: (800) 728-1212
Fax: (408) 496-3636
Email:
product_info@rational.com
Web: <http://www.rational.com>

Canada

Tel: 613-599-8581

France

Tel: +33-1-30-12-09-50

Germany

Tel: +49-89-797-021

United Kingdom

Tel: +44-1273-624814

Sweden

Tel: +46-8-703-4530
Fax: +46-8-760-0026

Australia

Tel: +61-2-419-8455

Taiwan

Tel: +886-2-720-1938

Italy

Tel: +39-2-264-0107

Spain

Tel: +34-1-571-39-62

Israel

Tel: +972-3-531-3333

Japan

Tel: +81-03-3779-2541

SingleStep™

Debugger, Emulator/Simulator, Real-Time Tool

Software Development Systems, Inc.

SingleStep is an easy-to-use integrated debugging environment for embedded, real-time debugging. This ease of use is available under both Windows and UNIX.

SingleStep offers full source-level debugging in C and C++. It is tightly coupled to the embedded compilers from all the leaders in real-time compiler technology.

SingleStep also offers an innovative kernel-aware API that gives you point-and-click kernel awareness for both internally developed and off-the-shelf real-time kernels and operating systems. Kernel awareness is available today for many different kernels including pSOSystem, VxWorks, C EXECUTIVE, Nucleus, RTEK, RTXC, OSE, MQX, AMX, and SuperTask!.

SingleStep is available in many different varieties, including:

- *Advanced Simulator/Debugger* lets you develop your software and hardware in parallel.
- *On Chip Debugger* provides a simple target connection through JTAG and JTAG-like ports and offers you extremely fast downloading speeds.
- *Target Monitor Debugger* is available for many off-the-shelf boards and can be easily adapted to any custom hardware configuration.

- Versions that talk to Ethernet and various emulator and emulator-like products are also available.

Features

- Easy to use.
- Extremely responsive support.
- Runs seamlessly under Windows and UNIX (Motif and OpenLook).
- Extensive support for C++.
- Works with the editors and make utilities that you use today.
- Fast, advanced simulation technology.
- Full support for all PowerPC processors.
- On Chip Debugging through PowerPC JTAG and JTAG-like ports.
- Kernel Aware Debugging for pSOSystem, VxWorks, C EXECUTIVE, Nucleus, RTEK, RTXC, OSE, MQX, AMX, and SuperTask!.
- Integrated with compilers from all the leaders in real-time compiler technology.

Software Generation and Debug Tools (Cross)

Processors Supported

- All PowerPC microprocessors.
- Other processor architectures are also supported.

Host Systems Supported

- Windows, Windows NT, and Windows 95.
- SunOS.
- Solaris.
- HP-UX.

Availability

- Available now. For a free Starter Kit, call or visit the Software Development Systems web site at <http://www.sdsi.com>.

SDS also offers several compiler suites. See "SDS C and C++ Compilers" on page 226.

Contact

North America

Software Development Systems, Inc.
815 Commerce
Suite 250
Oak Brook, IL 60521
USA
Tel: (630) 368-0400
Fax: (630) 990-4641
Email: sales@sdsi.com
Web: <http://www.sdsi.com>

Europe

Software Development Systems, Ltd.
Berkhamsted House
121 High Street
Berkhamsted
Hertfordshire HP4 2DJ
UK
Tel: +44 (0) 1442 876065
Fax: +44 (0) 1442 873262
sales@sdsuk.demon.co.uk

Japan

A. I. Corporation
IIJIMA Building 6F
2-25-2 Nishi-Gotanda
Shinagawa-ku, Tokyo 140
Japan
Tel: +81 (0) 334 937981
Fax: +81 (0) 334 937993

Asia-Pacific

Beijing Xuanji S&T Co.
Dongyuan Electron Bldg
No. B 3 Xitcheng Rd.
Haiden District
100088 Beijing
Peoples Republic of China
Tel: +86 10 623 83376
Fax: +86 10 623 72872

STEP Exceed-400

Analyzer, Debugger, Emulator/Simulator

STEP Engineering

The STEP Exceed-400 family of in-circuit emulators and integrated GUI source-level debuggers provides a cost-effective, flexible development platform for designing IBM PowerPC processor-based systems. Each Exceed-400 model provides non-intrusive, real-time, in-circuit emulation of PowerPC processors at full processor speed. The Exceed-400 is capable of reconstructing the program code executing from on-chip cache memory. The trace includes displays of the address, data, and instruction buses, including multiple instructions which are executed in one cycle, the control signals, and 32 external bits. An on-line assembler allows patching during the debug session.

The Exceed-400 can be configured with many advanced features, such as multi-level triggering, range breakpoints, and time tagging. Advanced logic analysis capability is provided via an integrated logic analyzer to allow multi-level triggering with a pass and position count and an enhanced matchword capability to allow range condition definitions.

Long execution histories based on complex conditions can be captured using selective store control. A performance analysis package allows program profiling as well as cache performance monitoring. Performance bottlenecks can be identified and measured through use of event and inclusive or noninclusive histograms and min/mean/max execution statistics.

As an option to the designer, high speed mapped memory permits ROM chips in the target system to be replaced with RAM on an external pod. The designer can then download to this mapped memory and execute programs even when the target's memory interface is nonfunctional.

To enhance software debugging, STEP Engineering's GUI source-level debuggers, SDEBUG II for Windows 3.1 and STEPGuide under X11/R6 and the Motif Window Manager, allow quick and easy access to many of the major functions of the Exceed-400 emulators using state-of-the-art point-and-shoot methodology.

Software Generation and Debug Tools (Cross)

Hosts Supported

- IBM PC (Windows, PS/2).
- RS/6000.
- Sun.

Processors Supported

- IBM PowerPC 400 series.

Availability

- Available now.

STEP Engineering

U.S. Sales Office
661 East Arques Avenue
Sunnyvale, CA 94086

Tel: (800) 538-1750
Tel: (408) SEE-STEP
Fax: (408) 773-1073
Email: info@stepeng.com
Web: <http://www.stepeng.com>

Contact

For international contacts, call U.S. Sales office.

The AdaWorld Cross-Development Environment

Compiler, Debugger, Libraries, Real-Time Tool, Utilities

Thomson Software Products

AdaWorld for Power PC microprocessor under LynxOS operating system is a powerful Ada development environment specifically designed for creation of demanding real-time embedded applications. The AdaWorld cross-development system runs on IBM RISC System/6000 workstations (both POWER and PowerPC 601 processor-based) under AIX. The optimized cross-compiler generates fast, efficient code for the PowerPC architecture running under LynxOS, a real-time POSIX-compliant UNIX operating system.

Standard AdaWorld Features

- *AdaWorld for MOTIF GUI*—AdaWorld/Motif is a highly intuitive OSF/MOTIF-based GUI. Its COSE-compliant design allows you to make maximum use of AdaWorld tools with minimal training.
- *Multi-Library System (MLS)*—This unique AdaWorld feature supports both relational and hierarchical libraries, simplifying the development of large applications in distributed workgroup environments. MLS can also move or copy a library or set of libraries in object code format without recompiling the source, and with full library security. Library roll back provides safe and easy recovery from erroneous library updates.
- *Maximum Runtime Efficiency*—The Ada Executive delivers highly efficient runtime performance by providing predefined and non-blocking input/output, automatic deallocations for each access type on scope exit, and optional exception handling.
- *Data Sharing between Applications*—AdaWorld provides access to externally defined data in Ada programs. Ada-defined data may be exported for easy access by programs written in other languages.
- *Chapter 13 Features*—The compiler supports Chapter 13 features of the *Ada Reference Manual*, including representation clauses to the bit level, address clauses, unchecked conversion and deallocation, package SYSTEM, interrupt entries for tasks, shared data, and interfaces to Assembler and C.
- *Productivity-Enhancing Tools*—The standard AdaWorld offering includes four powerful tools to enhance program development productivity.
 - *AdaProbe* is both a source code viewer for static analysis and a symbolic debugger for dynamic analysis.
 - *AdaXref* generates a full cross-reference of the declaration and use of Ada entities throughout an application.
 - *AdaReformat* gives source code a common look and is easily customizable to meet most application-building standards.
 - *AdaMake* automates application rebuilding after source-level modifications.
- *Portable OS Calls*—Implementation of the POSIX Ada binding (IEEE 1003.5) provides Ada applications with direct access to POSIX primitives, allowing greater flexibility for utilizing operating system capabilities. The POSIX real-time Ada binding provides Ada applications with portable real-time services.

Software Generation and Debug Tools (Cross)

- *Clear Diagnostic Messages*—The AdaWorld compiler includes a powerful diagnostic system which indicates error sources, and references relevant sections of the *Ada Language Reference Manual*. The compiler enhances the productivity of both beginning and advanced programmers by suggesting corrective actions for many errors, and providing details regarding program objects involved.
- *World-Class Support from Thomson Software Products*—Should you need more than just technical support, Thomson Software Products provides a comprehensive range of consulting services. At Thomson Software Products, we are committed to making your project a success.

AdaWorld for PowerPC/LynxOS Features

- *Optimized Cross-Compiler*—The AdaWorld compiler has both high-level and low-level optimizations to take full advantage of the PowerPC architecture
- *LynxOS Threads Support*—AdaWorld maps each Ada task on a LynxOS thread so that task blocks waiting for resources do not affect other tasks. External events are efficiently handled through blocking reads on device drivers.

Optional AdaWorld Components

- AdaEdit
- AdaConnect
- Ada/WorkBench Package
- Interfacing X-Windows and OSF/MOTIF

Contact

Thomson Software Products

10251 Vista Sorrento
Parkway
Suite 300
San Diego, CA 92121
Tel: (619) 457-2700
Fax: (619) 452-2117
Web: <http://www.thomsoft.com/products/ada/Ada.html>

Domestic Sales Offices

California

Thomson Software Products
10251 Vista Sorrento
Parkway
Suite 300
San Diego, CA 92121
Tel: (619) 457-2700
Fax: (619) 452-2117

Texas

Thomson Software Products
2777 Stemmons Freeway
Suite 1133
Dallas, TX 75207
Tel: (214) 630-4211

Massachusetts

Thomson Software Products
200 Wheeler Road
6th Floor
Burlington, MA 01803
Tel: (617) 270-0030
Fax: (617) 270-6882

Virginia

Thomson Software Products
779 Leesburg Pike
Suite 900N
Falls Church, VA 22043
Tel: (703) 847-6787
Fax: (703) 847-2958
Fax: (214) 630-3766

Worldwide Locations

France

Thomson Software Products
66-68 Avenue Pierre
Bossollette
92240 Malakoff
Tel: (1) 41.48.10.0
Fax: (1) 41.48.10.20

United Kingdom

Thomson Software Products Ltd.
Patridge House
Newton Road
Henley-on-Thames
Oxon, RG9 1EN
Tel: (0491) 579090
Fax: (0491) 571866

Sweden

Thomson Software Products AB
Marinens Vag 30
S-136 40 Haninge
Tel: (08) 707 3060
Fax: (08) 707 3080

Germany

Thomson Software Products GMBH
Kleinoberfeld 7
D-76135 Karlsruhe
Tel: (72) 1-98653-0
Fax: (72) 1-98653-98

Japan

Thomson Software Products KKE
TechnoWave 100, 16F
1-1-25 Shin-Urashima-cho
Kanagawa-ku
Yokohama 221
Tel: (45) 451-2412
Fax: (45) 451-2419

Software Generation and Debug Tools (Native and Cross)

Apogee-C and Apogee-C++

Compiler, Debugger, Libraries

Apogee Software, Inc.

Apogee Software, Inc. specializes in optimizing compilers for RISC-based systems. Currently, Apogee offers compilers for RS/6000 and PowerPC processors running AIX and Windows NT, and SPARC processors running Solaris 1 and 2. Apogee's proprietary optimizing technology has been licensed by major hardware and software makers such as Silicon Graphics, Intergraph, Philips, and Microtec Research.

Modes

Apogee-C and Apogee-C++ are available as native as well as embedded compilers. The Apogee-C compiler has four modes:

- ANSI mode, which is fully compliant with ANSI C (AIX only).
- K & R mode, which is compatible with K & R C (AIX only).
- Mixed mode, which adds a number of features to ANSI mode that simplify porting older programs (AIX only).
- Microsoft C compatibility mode (Windows NT only).

The Apogee-C++ compiler has five modes:

- Cfront 2.1 compatibility mode (AIX only).
- Cfront 3.0 compatibility mode (AIX only).
- ANSI-C++ mode (AIX only).
- Mixed (ANSI-C++ with selected Cfront constructs) (AIX only).
- Microsoft C++ compatibility mode (Windows NT only).

Features

The Apogee Compilers give you extensive control over the compilation process through use of a compilation control language. This

language can be used either on the compilation invocation line or on pragma statements within the source file. Some of the controllable aspects of compilation are:

- Optimization. A very fine level of control of the optimizations performed is available. Each type may be individually controlled, usually within several different levels.
- Target Computer Properties. The instruction pipeline, and the cache properties may be independently specified.
- Diagnostic and error reporting.
- Zero-trip vs. one-trip treatment of loops.
- Stack vs. static treatment of local variables.
- Support for incompatible VMS features.
- PIC vs. non-PIC compilation.
- .data vs. .bss treatment of uninitialized data.
- Printing of compiler progress.
- Printing of intermediate representations.
- Control of memory utilization.

The Apogee Compilers offer an impressive range of optimizations:

- Global and local constant propagation (repeated until all possible higher order (indirect) propagations are done).
- Constant folding.
- Global and local common subexpression elimination, including partially redundant expressions.
- Global and local copy propagation.
- Useless and unreachable (dead) code elimination, including elimination of useless loads and redundant loads and stores.
- Global backward code motion (hoisting).
- Global forward code motion, including stores.

Software Generation and Debug Tools (Native and Cross)

- Extensive strength-reduction and reassociation in nested loops of all levels, including loops with complex control flow, (e.g. multiple exits, irreducible loops).
- Induction variable elimination.
- Interprocedural memory-reference alias analysis.
- Interprocedural call-effect analysis.
- Interprocedural register allocation.
- User procedure inlining.
- Control-flow optimizations (repeated iteratively).
- Loop unrolling.
- Variables may be resident in registers.
- Global register allocation using priority-based coloring.
- Scheduling specific to the target machine instruction pipeline.
- Delayed-branch filling.

Target Processors Supported

- PowerPC 600 family running AIX or Windows NT.
- PowerPC 403 family/EABI.
- Some Motorola PowerPC processors are also supported.

Hosts Supported

- IBM RS/6000 running AIX™.
- PowerPC 600 family running AIX or Windows NT.
- SPARC/SunOS and SPARC/Solaris 2.

Configurations

- Native compilers for RS/6000 and PowerPC processors running AIX.
- Native compilers for PowerPC processors running Windows NT (compilers come with Microsoft-compatible linker, run-time libraries and debugger).
- Stand-alone cross-compilers for PowerPC 600 and 400 embedded processors, ready for integrations with vendor-provided tools.
- Cross-compilers integrated with Microtec Research's XRAY® programming environment for PowerPC 600 and 400 processors.

Availability

- Available now.

Contact

Apogee Software, Inc.
1901 S. Bascom Avenue,
Ste. 325
Campbell, CA 95008-
2207

Tel: 408-369-9001
Fax: 408-369-9018
Email:
sales@apogee.com

Japan

Apogee Japan Corp.
1264-6, Minami-Otsuka
Kawagoe-Shi
Saitama-Ken
Japan 350-11
Tel: 0492-48-0037
Fax: 0492-44-9670
email:
mcrane@bekkoame.or.jp

Germany

G&W Systems GmbH
Neue Weide 35
52499 Baesweiler
Germany
Tel: 2401-9768-0
Fax: 2401-9768-27
email:
thomas@gwsys-
tems.com

Other Areas

Apogee has over 20
resellers worldwide.
Please contact Apogee
for the reseller nearest to
you.

Apogee-FORTRAN 77

Compiler, Debugger, Libraries

Apogee Software, Inc.

Apogee Software, Inc. specializes in high performance highly optimizing compilers for RISC based systems. Currently, Apogee offers compilers for RS/6000 and PowerPC processors running AIX and Windows NT, and SPARC processors running Solaris 1 and 2. Our Apogee's proprietary optimizing technology has been licensed by hardware and software makers such as Silicon Graphics, Intergraph, Philips, and Microtec Research.

Features

The Apogee-FORTRAN 77 compiler supports almost all language extensions found in Sun, VAX/VMS, IBM, Cray, and MIL-STD 1753 FORTRAN 77. Some of these extensions are:

- Record and structure declarations, and computations with aggregates
- Type extensions (e.g. REAL*4, INTEGER*4, BYTE, LOGICAL*1, LOGICAL*2, INTEGER*2, COMPLEX*16, REAL*16, COMPLEX*32, etc.)
- Initialization in type statements
- The END DO and DO WHILE statements
- The INCLUDE statement.
- The VOLATILE statement.
- Intrinsic functions in PARAMETER statements.
- OPEN and INQUIRE statement extensions.

General Compiler Features

The Apogee Compilers give you extensive control over the compilation process through use of a compilation control language. This language can be used either on the compilation

invocation line or on pragma statements within the source file. Some of the controllable aspects of compilation are:

- Optimization. A very fine level of control of the optimizations performed is available. Each type may be individually controlled, usually within several different levels.
- Target Computer Properties. The instruction pipeline, and the cache properties may be independently specified.
- Diagnostic and error reporting.
- Zero-trip vs. one-trip treatment of loops.
- .data vs. .bss treatment of uninitialized data.
- Printing of intermediate representations.
- Control of memory utilization.

The Apogee Compilers offer an impressive range of optimizations.

- Global and local constant propagation (repeated until all possible higher order (indirect) propagations are done).
- Constant folding.
- Global and local common subexpression elimination, including partially redundant expressions.
- Global and local copy propagation.
- Useless and unreachable (dead) code elimination, including elimination of useless loads and redundant loads and stores.
- Global backward code motion (hoisting).
- Global forward code motion, including stores.

Software Generation and Debug Tools (Native and Cross)

- Extensive strength-reduction and reassociation in nested loops of all levels, including loops with complex control flow, (e.g. multiple exits, irreducible loops).
- Induction variable elimination.
- Interprocedural memory-reference alias analysis.
- Interprocedural call-effect analysis.
- Interprocedural register allocation.
- User procedure inlining.
- Control-flow optimizations (repeated iteratively).
- Loop unrolling.
- Variables may be resident in registers.
- Global register allocation using priority-based coloring.
- Scheduling specific to the target machine instruction pipeline.
- Delayed-branch filling.

Target Processors Supported

- PowerPC 600 family of processors running AIX or Windows NT.
- Some Motorola PowerPC processors are also supported.

Hosts Supported

- IBM RS/6000 running AIX™.
- PowerPC 600 family running AIX or Windows NT.
- SPARC/SunOS and SPARC/Solaris 2.

Configurations

- Native compiler for RS/6000 and PowerPC processors running AIX.
- Native compiler for PowerPC running Windows NT (the compiler comes with Microsoft-compatible linker, run-time library, and debugger).
- Stand-alone cross-compiler for PowerPC 600 and 400 embedded processors, ready for integration with vendor-provided tools.

Availability

- Available now.

Contact

Apogee Software, Inc.
1901 S. Bascom Avenue,
Ste. 325
Campbell, CA 95008-
2207
Tel: 408-369-9001
Fax: 408-369-9018
email:
sales@apogee.com

Japan
Apogee Japan Corp.
1264-6, Minami-Otsuka
Kawagoe-Shi
Saitama-Ken
Japan 350-11
Tel: 0492-48-0037
Fax: 0492-44-9670
email:
mcrane@bekkoame.or.jp

Germany
G&W Systems GmbH
Neue Weide 35
52499 Baesweiler
Germany
Tel: 2401-9768-0
Fax: 2401-9768-27
email:
thomas@gwsys-
tems.com

Other Areas
Apogee has over 20
resellers worldwide.
Please contact Apogee
for the reseller nearest to
you.

Essentials•Tools•Objects

Compilers, Debuggers, Libraries, Utilities

Apple Computer, Inc.

E.T.O. is a general-purpose C/C++ development environment for creating, debugging and testing applications that can be run on a 680x0- or PowerPC-based Macintosh system.

E.T.O. includes:

- *MPW Shell*—An integrated multiwindow text editor and command shell with many built-in commands and a powerful scripting language. It also includes Projector, an integrated source code control system ideal for managing large, complex software projects.
- *SC/SCpp C and C++ Compilers (680x0)*—These new ANSI-compliant MPW compilers are fast, run in native mode on a Power Macintosh, and support the new CPM-68K runtime model.
- *MrC/MrC++ C and C++ Compilers (PowerPC)*—These new ANSI-compliant MPW compilers offer fast turnaround time and generate efficient and highly-optimized PowerPC code for fastest binary execution on Power Macintosh systems.
- *Assembler (680x0 and PowerPC)*—Supports the full 680x0 and PowerPC instruction sets. The 680x0 assembler also supports the 68851 PMMU and the 68881/882 floating-point coprocessors.
- *MPW Tool Suite*—Dozens of tools and scripts to assist in the development process. These include linkers, a Make tool, resource manipulation tools, file comparison utilities, and many more.
- *SourceBug (680x0)*—A source-level debugger that provides basic debugging capabilities, such as setting breakpoints, controlling program execution, and displaying the contents of variables. SourceBug also has special support for debugging object-oriented code.
- *Power Macintosh Debugger (PowerPC)*—A powerful PowerPC debugger featuring an easy-to-use interface for setting breakpoints, examining and changing the contents of memory and registers, and viewing the code at either source or machine level.
- *MacApp*—An advanced object-oriented application framework and class library which can be used to streamline the development of Power Macintosh and 680x0 applications.
- *Documentation*—A printed manual that introduces the MPW environment: *Introduction to MPW*. Electronic versions of this manual and most of the major components of E.T.O. are included on a CD-ROM for easy reference. Printed manuals can be ordered separately.

E.T.O. is a deluxe product designed specially for professional Macintosh developers. It is sold by subscription, so new releases with tool updates are automatically sent every four months.

Software Generation and Debug Tools (Native and Cross)

System Requirements

- A 68020, 68030, 68040 or Power Macintosh. A Power Macintosh is required for the execution and debugging of PowerPC code.
- 8 MB of RAM (16 MB or more are strongly recommended).
- CD-ROM drive.
- System 7.0 or later.

Availability

- Available now.

Ordering Information

- E.T.O.—Order Number M0895LL/C.

Contact

Apple Computer, Inc.
Apple Developer Catalog
P.O. Box 319
Buffalo, NY 14207-0319
U.S.: (800) 282-2732
Canada: (800) 637-0029
International: (716) 871-6555
Fax: (716) 871-6511
Web: <http://www.devtools.apple.com>

Cygnus Developer's Kit for PowerPC Architectures

Compilers, Debugger, Libraries, Utilities

Cygnus Support

The Cygnus Developer's Kit (CDK) is optimized to simplify development of embedded applications targeted to IBM PowerPC architectures. Cygnus backs CDK with time-critical problem resolution and adds to GNU technology by incorporating updates and enhancements into each quarterly release. This process ensures that CDK remains on the cutting edge of software development.

An integral part of CDK is the wide range of world-class support and custom development services offered by Cygnus: Guaranteed response times to problem reports as short as one day, custom compiler enhancements and optimizations as well as development of complete custom tool chains.

Features

- System v.4 ABI conformant.
- PowerPC Simulator
 - Greater than 200K instructions per second.
 - Full MMU simulation.
 - Function unit performance tracing.
 - Virtual device interface.
- Includes the GNU C/C++ compilers, remote windowing source level debugger with gui interface, macro-assembler, linker, binary file utilities.
 - ELF/DWARF1 format support for C.
 - PowerOpen calling sequence supported.
 - Command-line structure packing, bit field alignment, big or little endian code.
 - String instruction optimizations.
 - Function prologue/epilogue optimizations.
 - Processor-specific scheduling.

- One optimized toolkit portable to over 70 host/target combinations.
- Quarterly updates of maintained versions of GNU, fully integrated, single-sourced tool set.
- Tested quarterly against regression and Plum Hall test suites.
- Guaranteed response time to all reported problems.
- Customizing capabilities include GNU make and full source code; use modify and redistribute without fees.
- Graphical user interface for the GNU debugger is available for X Windows and Windows 3.1 environments.

Host Platforms

- HP 9000/700 platform running HP-UX 9.05.
- i386 platform running DOS.
- PowerPC platform running AIX 4.1.1.
- IBM RS/6000 platform running AIX 3.2.5.
- SPARC platform running Solaris 2.4 or SunOS 4.1.4

PowerPC Target Platforms

- PowerPC 601, 603, 603E and 604 microprocessors.
- PowerPC 403GA, 403GB, and 403GC embedded controllers.

Software Generation and Debug Tools (Native and Cross)

Components

- *GCC*
 - Strict compilation modes; K&R, ANSI, Strict ANSI compilation modes.
 - Plum Hall, regression tested.
 - ROMable applications for better control of code.
 - Three user controlled optimization levels.
 - No built-in compile-time size limits.
 - Converts C to assembly.
- *GDB*
 - Symbolic, source-level debugger.
 - Graphical user interface.
 - Supports multiple execution environments, including simulator for early prototyping.
 - Fully integrated with GCC and G++.
- *G++*
 - Field tested since 1989.
 - Compiles C++ to assembler, not a cfront implementation.
 - Tracking ANSI X3J16 C++.
 - Standard template library—Libstdc++.
 - Embedded EH and RTTI support for optimized code.
 - Automatic template instantiation.

Availability

- Available now.

Contact

Cygnus Support

1937 Landings Drive
Mountain View, CA 94043
Tel: (800) cygnus-1
Tel: (415) 903-1400
Fax: (415) 903-0122
Email: info@cygnus.com
Web: <http://www.cygnus.com>

C for AIX® Version 3

Compiler

IBM Corporation

IBM C for AIX Version 3 offers enhanced function and flexibility for C software developers who build and maintain applications on AIX Version 4.1. C for AIX Version 3 is a new C compiler product designed to replace the XL C Compiler, which is shipped with the AIX Version 3 operating system. IBM C for AIX Version 3 includes an optimizing C Compiler and the xldb debugger.

Features

- *New C Compiler and Language Features*—C for AIX supports 64-bit integer (long long) data type and 128-bit floating-point (long double) data type. In addition, C for AIX supports run-time address checking. An exception will be raised at runtime in situations where storage is being referenced by a null pointer, or a subscript within an object is out of bounds. Run-time checks enable programmers to trace memory problems at runtime and use the information to make necessary changes to programs.
- *Improved Optimization*—C for AIX supports profile-directed feedback. This allows the optimizer to have a better understanding of the program behavior before actually attempting to optimize it. The result is better execution performance of the program. In addition, these compilers generate code to fully exploit the RISC System/6000 family (including POWER, POWER2, and PowerPC 601 processors) plus common code that runs on all RISC System/6000 processors. You can now develop more efficient C applications on RISC System/6000 platforms using C for AIX.

- *New Debugger*—A new GUI-based C and C++ debugger, xldb, will be shipped with C for AIX. This makes debugging C programs on AIX easier and more efficient.
- *Open Enterprise*—C for AIX conforms to the following standards:
 - ANSI/ISO-IEC 9899:1990 1992
 - ISO/IEC 9899:1990(E)
 - FIPS 160 C
- *Release 3.1.3 enhancements:*
 - Exploits PowerPC 604 RISC System/6000 processors.
 - xldb debugger supports multiple thread application, CICS for AIX V2 application and displays multiple byte character set.

Compatibility

- *Source Compatibility*—C programs written using C Set ++ Version 2, and XL C Compiler (component of AIX Version 3.2), are source compatible with C for AIX Version 3, with some exceptions to detect invalid programs or areas where results are undefined. These exceptions are documented in the product README file.
- *User Interface Compatibility*—The compile options of C for AIX are consistent with that of C Set ++ for AIX Version 2 and the XL C Compiler that ships with AIX Version 3.
- *Binary Compatibility*—Most programs compiled on AIX Version 3.2 or greater for POWER, POWER2, and PowerPC based models of RISC System/6000, using C Set ++ for AIX Version 2 and XL C Compiler, may run without recompilation for those same models.

Software Generation and Debug Tools (Native and Cross)

Compiler Runtime

- The compiler run-time components of C for AIX are shipped with AIX Version 4.1 and do not need to be redistributed.

Machine Requirements

- IBM C for AIX is designed to execute on RISC System/6000 family processors running AIX Version 4.1 including POWER, POWER2, and PowerPC processors configured with at least one supported display and keyboard.
- xldb requires a graphical display and mouse to operate.

Program Requirements

- AIX Version 4.1. The source debugger (xldb) requires X11R5 runtime.

Ordering Information

- C for AIX Version 3 (5765-423).

Availability

- Available now.

Contact

IBM Corporation

To order, contact IBM Direct:
Tel: (800) IBM-4YOU
Email: askibm@info.ibm.com
Web: <http://ibm-direct.e-com.ibm.com>

For licensing information, contact:
IBM RISC System/6000 Division
AIX OEM & Licensing/MS 9581
11400 Burnet Road
Austin, TX 78758
Tel: (512) 838-4075
Fax: (512) 838-3461

C Set ++™ for AIX® Version 3

Compiler

IBM Corporation

Version 3 of C Set ++™ for AIX is the follow-on offering to Version 2 of C Set ++ for AIX and C++ POWERbench. C Set ++ for AIX now includes tools provided by SDE Workbench and C++ POWERbench, integrated using the common desktop environment (CDE).

Features

- IBM C for AIX C compiler.
- C++ compiler that supports native system object model (SOM) objects, including direct-to-SOM.
- Powerful set of C and C++ programming tools, integrated using the CDE:
 - LPEX editor.
 - Program builder.
 - xldb, a new graphical C and C++ source debugger.
 - HeapView debugger.
 - Browser.
 - Test coverage analyzer.
 - C Set ++ InfoExplorer™ documentation.
- Comprehensive set of class libraries:
 - Iostream, task, and complex.
 - Application support class library.
 - Collection class library.
 - User interface class library.
- C++ tutorial.

Version 3 of IBM C Set ++ for AIX supports the new features of AIX Version 4.1, including de-install, loader, binder, linker, and system libraries. C and C++ compilers shipped with IBM C Set ++ for AIX Version 3 fully exploit the RS/6000™ family of processors including POWER, POWER2, and PowerPC 601 processors. The compilers also generate common code that runs on all RS/6000™ processors.

New Programming Tools

- *LPEX*—LPEX is a programmable editor for creating and editing many kinds of data including programs and documentation. LPEX supports:
 - Live parsing of C and C++ source code using color and fonts.
 - Multiple windows to view different files or more than one view of a given file.
 - Block copy or move between two files or between a file and a UNIX shell or another application.
 - Comprehensive search capability.
 - Programmable auto-save capability.
 - Unlimited undo capability.
 - Addition of frequently-used commands to menus—create new menus and set keys to issue specific commands (LPEX is highly extensible by use of MACROS).
- *Program Builder*—The program builder is a GUI to the compiling and linking tools. The Motif-based interface has pull-down menus and dialog boxes that simplify compile options, linking libraries and invoking compilers. C and C++ compilers are supported. The program builder saves build and make-file options so that, upon returning to a given directory, the appropriate configuration is restored. The program builder also supports error browsing. When an error is selected from the program builder list, the editor automatically positions the cursor to the source code where the error occurred.
- *Debugger*—xldb, a new GUI-based C and C++ debugger, will be shipped with Version 3 of C Set ++ for AIX.

Native Support for SOM

Version 3 of C Set ++ for AIX offers support for direct-to-SOM (DTS) C++. This simplifies the effort for developing SOM applications and allows C++ programmers to write virtually the same code they presently do for C++ objects. The C++ compiler takes care of generating the objects as SOM objects.

SOM includes release-to-release binary compatibility, local and remote objects, language independence of objects, and easy coding to SOM-based frameworks.

New C and C++ Compiler and Language Features

- 64-bit integer (long long) data type.
- 128-bit floating point (long double) data type.
- Run-time address checking allows an exception to be raised at run-time in situations where storage is referenced by a null pointer, or a subscript within an object is out of bounds.

Improved Optimization

The C and C++ compilers support profile-directed feedback allowing the optimizer to have a better understanding of the program behavior before attempting to optimize it. The result is better execution performance. These compilers also generate code to fully exploit the RISC System/6000 family of processors (including POWER, POWER2, and PowerPC

processors) and generate common code that runs on all RS/6000 processors.

New and Enhanced Class Libraries

New features added to the collection class library include three new pointer classes for more efficient handling of storage management, a newcursor class for better polymorphic programming, and new sample programs to help users. The user interface class library is an object-oriented C++ class library that enables programmers to build efficient Motif-based GUI applications on AIX. This class library enables programmers to develop Motif applications more conveniently in C++.

The C compiler of C Set ++ for AIX conforms to the following standards:

- ANSI/ISO-IEC 9899:1990 1992
- ISO/IEC 9899:1990(E)
- FIPS PUB 160 C (certified)
- XPG4 (branded)

Machine and Programming Requirements

- RISC System/6000 or other supported hardware running AIX Version 4.1 configured with at least one supported display, keyboard, and mouse.

Ordering Information

- C Set ++ for AIX Version 3 (5765-421).

Availability

- Available now.

IBM Corporation

To order, contact IBM Direct:
Tel: (800) IBM-4YOU
Email: askibm@info.ibm.com
Web: <http://ibm-direct.e-com.ibm.com>

Contact

For licensing information, contact:
IBM RISC System/6000 Division
AIX OEM & Licensing/MS 9581
11400 Burnet Road
Austin, TX 78758
Tel: (512) 838-4075
Fax: (512) 838-3461

PowerAda® and PowerAda®/LynxOS

Compiler, Debugger, Utilities

OC Systems, Inc.

PowerAda from OC Systems (OCS) provides a complete, integrated software development and support environment for all PowerPC platforms running AIX and LynxOS, including the RS/6000 platform. PowerAda includes full, validated implementations of both Ada language standards, Ada 83 and Ada 95, as defined by the ANSI/ISO standards for the language. PowerAda has been used to develop tens of millions of lines of code for large-scale, complex, critical software systems throughout the world.

PowerAda generates code for the PowerPC 601, 603, and 604 microprocessors, and for the IBM RS/6000 and RS/6000 SP2 platforms. The compiler is also designed to run on SMP configurations for the PowerPC processor. The compiler generates the best code quality for Ada on PowerPC architectures.

Object-oriented support is provided with a CORBA-compliant object request broker (ORB), IBM's SOM/DSOM (System Object Model/Distributed System Object Model), and an IDL-to-Ada 95 compiler. CORBA (Common Object Request Broker Architecture) is an industry standard provided by the Object Management Group (OMG). IDL (Interface Description Language) provides a standard mapping between software packages written in different programming languages, enabling the automatic generation of bindings between programs.

Ada 95 is the first and only international standard for object-oriented programming languages. With the other OO standards (CORBA, IDL, SOM/DSOM), PowerAda delivers superior, well-defined/designed support for object-oriented software development and support.

In addition to both Ada 83 and Ada 95 compilers, PowerAda includes a powerful suite of software tools:

- Multi-language, full source-code, point-and-click debugger, with an intuitive, easy-to-use interface. Provides the capability for remote debugging for host and target computer platforms.
- Source-code and class browsers, with GUI user interface.
- Aprobe, a dynamic code monitoring and instrumentation tool that allows minimally intrusive programmatic monitoring of executing code, for debugging, validation, and performance monitoring.
- Afun provides automatic detection of uninitialized variables.
- Test coverage analysis.

PowerAda also features on-line hypertext documentation, enabling immediate look-ups of pertinent information. A copy of the documentation is delivered in postscript files, allowing the user to print relevant portions of the documentation.

PowerAda/LynxOS provides a superb real-time embedded software capability for hard real-time applications. LynxOS is a POSIX-compliant real-time UNIX OS, that supports multi-threaded, multi-process embedded systems. LynxOS is modular and ROMable, with advanced interrupt handling and memory management.

OC Systems has a strong commitment to providing outstanding technical support. Virtually all of the technical support is handled via electronic mail over the OCS Internet node. Most questions and problem or bug reports are resolved in less than one day, with a typical

Software Generation and Debug Tools (Native and Cross)

response or fix requiring two hours or less of elapsed time. Technical questions and inquiries are handled directly by senior software engineers. PowerAda users have direct access to senior technical personnel at OCS.

PowerAda users receive a quarterly newsletter, *The Power Source*, which keeps users up-to-date on planned enhancements to PowerAda, improved techniques for working with the software tools included with PowerAda, and general software-related features and updates.

OCS also maintains an active Web page, as well as an ftp site for PowerAda users to download new software packages and code.

Here are some of the main reasons to choose PowerAda:

- 60-day evaluation of PowerAda on request.
- No runtime fees for PowerAda.
- PowerAda is offered free to accredited academic institutions.

- CORBA-compliant ORB and IDL included with PowerAda.
- PowerAda supports both Ada 83 and Ada 95.
- The world's first international standard for object-oriented software, Ada 95, is included with PowerAda.
- PowerAda generates code for all PowerPC- and POWER-architecture computers (PowerPC 601, 603, 604 microprocessors, RS/6000, RS/6000 SP2, and SMP computers).
- Field-proven, with tens of millions of lines of code developed.
- Technical support and powerful software tools are part of the PowerAda solution.

Availability

- Available now.

Contact

OC Systems, Inc.

9990 Lee Highway
Suite 270
Fairfax, VA 22030
Tel: 703-359-8160
Fax: 703-359-8161

Sales & Marketing
Tel: 703-359-9709
Email: info@ocsystems.com
Web: <http://www.ocsystems.com>
Point of contact: Ralph Crafts (rec@ocsystems.com)

France (Benelux)

AixLife
Batiment Cezanne
Avenue Madeleine Bonnaud
13770 Venelles
France
Tel: +33 4254 1064
Fax: +33 4254 1091
Email: 100564/2573@compuserve.com
Point of contact: Jean-Pierre Hoornaert

Germany

GSE Gesellschaft für Software Engineering mbH
Riesstrasse 17
80992 München
Germany
Tel: 49 89 14 009 265
Fax: 49 89 14 009 140
Email: elk@gse.com
Point of contact: Else Kluger

Operating Systems and Development Environments (Desktop)

Power Firmware™ System ROM Code

Code, Utilities

FirmWorks

Power Firmware is a complete Open Firmware ROM implementation for the PowerPC. Open Firmware, formally known as IEEE Standard 1275-1994, is the first non-proprietary open standard for boot firmware that is usable on different processors and buses. Open Firmware includes a processor-independent *device interface* that allows an add-in peripheral card to identify itself and to supply a single boot driver that can be used, unchanged, on any CPU using Open Firmware. Open Firmware also includes a *user interface* with powerful scripting and debugging capabilities, and a *client program interface* that allows operating systems and their loaders to make use of Open Firmware services to assist in the configuration and initialization process. Open Firmware is required by the PowerPC Reference Platform Specification and by the Common Hardware Reference Platform Specification (CHRP™).

Power Firmware complies with:

- IEEE Standard 1275-1994 Open Firmware Core Standard.
- PowerPC Binding to IEEE Standard 1275-1994.
- PCI Binding to IEEE Standard 1275-1994.
- PowerPC Reference Platform Binding to IEEE Standard 1275-1994.
- PowerPC Microprocessor Common Hardware Reference Platform (CHRP™) System Binding to IEEE Standard 1275-1994.
- PowerPC Reference Platform Specification.
- Common Hardware Reference Platform Specification.

Power Firmware supports:

- PowerPC 601, PowerPC 603, PowerPC 604, and PowerPC 620 microprocessors and their variants.
- IBM, Motorola, and other popular bridge chips.
- PCI, ISA and other buses.
- Windows NT, AIX, Macintosh OS, Solaris, LynxOS, VxWorks.

The core technology of Power Firmware is a small, fast, efficient Forth micro-kernel enabling powerful, interactive debugging and automated system configuration. This mature code is based on a field-proven implementation and can be easily ported to your specific system architecture. Both binary and source licensing are available on attractive terms.

Features

- Provides machine-independent configuration and booting support for plug-in devices.
- Provides a framework for plug-in drivers so that user-installed peripherals work out-of-the-box.
- Provides a standard set of firmware functions for use by client programs: operating systems, loaders, diagnostics, etc.
- Provides complete run-time configuration information to client programs.
- Contains a full ANS Forth interpreter for interactive programming, debugging and configuration.
- Off-the-shelf drivers are available for many commonly-used devices.
- Custom drivers can be created for you.

Operating Systems and Development Environments (Desktop)

Technical Support

- Telephone support.
- Consulting services.
- Training:
 - At FirmWorks.
 - At your site.
- Porting to your system:
 - Modifications for your architecture.
 - Creation of custom drivers.
- Bring-up assistance with new systems.

Licensing

Source and object code licenses available. A royalty will be due for each system sold that incorporates Power Firmware or any derivative thereof.

Availability

- Available now.

Contact

FirmWorks

Suite 115
480 San Antonio Road
Mountain View, CA 94040-1218
Tel: (415) 917-0100
Fax: (415) 917-6990

Email: ppc-tools@firmworks.com
<ftp://firmworks.com/pub>
Web: <http://www.firmworks.com>

Configuration Management Version Control (CMVC)

Utilities

IBM Corporation

IBM Configuration Management Version Control (CMVC) is a product family available for IBM RISC System/6000, HP, and Sun environments. The IBM CMVC products provide PowerPC application developers with configuration management and change control or versioning that is integrated with design and defect tracking for heterogeneous environments. Any CMVC server can support any of the three clients (IBM, Sun or HP).

CMVC/6000 was developed for use in a distributed networking environment. It is based on a client-server model. The CMVC server code accesses the server file system and a relational database for the storage and retrieval of versioned files and project information. The CMVC client code accesses the information and files stored on the CMVC server workstation.

The CMVC products run on IBM RISC System/6000, Sun, HP, OS/2 or DOS/Windows client workstations. On all platforms, the CMVC Server provides versioning, tracking and management support.

The CMVC/6000 Server uses a relational database management system (RDBMS). Currently supported databases include: DB2/6000, ORACLE, INFORMIX, and SYBASE on the RISC System/6000. The CMVC for Sun Server uses the ORACLE and INFORMIX databases on Sun systems. The CMVC for HP Server uses the ORACLE and INFORMIX databases on HP systems.

Features

- Command line interface.
- Graphical user interface.
- Software configuration management.
- Version control.
- Integrated problem tracking.
- Change control.
- Release management.
- Access control.
- Automatic notification.
- Configurable processes and fields.
- User exits.

Benefits

- *Improved Software Quality*
 - provides a common process.
 - ensures easy process comprehension.
 - provides and audit trail.
 - provides quality metrics.
- *Increase Productivity*
 - provides an integrated system.
 - provides a consistent user interface across IBM, Sun and HP platforms.
 - facilitates software maintenance.
 - provides a change history.
- *Improved Project Communication*
 - provides change-specific documentation.
 - facilitates enhanced communication.
 - provides a customized report facility.
- *Increase Flexibility*
 - defining user roles.
 - allows configurable processes.
 - provides configurable fields.
 - provides over 100 user exits.
 - provides archive and restore compatibility.

Operating Systems and Development Environments (Desktop)

Operating Environments

- AIX Version 3.2 AIX Windows Environment/6000 Version 1.2.
- SUN OS Version 4.1.
- HP-UX Version 9.
- Solaris Version 2.3.

Reference Material

- IBM CMVC Concepts, (SC09-1633).
- IBM CMVC User's Guide, (SC09-1634).
- IBM CMVC User's Reference, (SC09-1597).
- IBM CMVC Commands Reference.

Ordering Information

- CMVC/6000 Version 2 (5765-207).

Availability

- Available now.

IBM Corporation

To order, contact IBM Direct:
Tel: (800) IBM-4YOU
Email: askibm@info.ibm.com
Web: <http://ibm-direct.e-com.ibm.com>

Contact

For licensing information, contact:
IBM RISC System/6000 Division
AIX OEM & Licensing/MS 9581
11400 Burnet Road
Austin, TX 78758
Tel: (512) 838-4075
Fax: (512) 838-3461

AIX® Version 3 for RISC System/6000®

Operating System

IBM Corporation

AIX Version 3.2.5 for RISC System/6000 is a full function polished release of the AIX operating system. It is a solid environment providing the latest improvements in AIX Version 3 software.

AIX Version 3.2 for RISC System/6000 is structured as a single worldwide operating system which includes National Language Support (NLS). The base operating system, compiler and networking performance improvements are designed to allow continued productivity and growth for users. Its related licensed programs support workstations and server solutions for engineering/scientific and commercial multi-user environments.

Compilation in common mode on AIX Version 3.2.5 creates an executable for POWER, POWER2, and PowerPC Platforms. This ensures that applications will optimize compatibility across these platforms and minimize the need for separate application source and/or binaries.

By pursuing a multiple-architecture strategy, IBM has been able to provide customers with a wide choice of functions and hardware to meet various requirements. The AIX operating system environment on multiple IBM processor architectures supports interoperability and portability of people, data, and programs across a broad range of price/performance solutions for customers.

AIX Version 3.2 for RISC System/6000 continues to demonstrate IBM's commitment to provide standards-driven products that satisfy customer requirements for open systems by incorporating many formal and informal industry standards and specifications. The AIX Family is evolutionary and will be extended over time to incorporate new technologies to provide solutions to open system market requirements.

Features

- Virtual Memory Manager (VMM) now supports up to 2GB of real memory.
- Logical Volume Manager (LVM) now supports hardfile devices with greater than 2GB via partitioning of space into multiple 2GB of logical volumes.
- TCP/IP performance enhancements based on RFC1323.
- High Availability Network File System (HANFS).
- Application Development Tools.
- Application Development Toolkit.
- Simple Network Management Protocol Agent.
- Block Multiplexer Channel Connective.
- Fiber Distributed Data Interface (FDDI) Connectivity.
- RISC System/6000 Serial Optical Channel Converter (SOCC) Support.
- On-Line Hypertext Softcopy Information.
- Diskless/Dataless Workstation Support.
- National Language Character Encoding and Handling.
- Text Formatting System.
- System Management Interface Tool (SMIT)
- Selective Enhancements.
- Visual Systems Manager feature provides a framework and functionality for an iconic interface to system management. Four applications are provided which allow the user to manage users and groups, devices, storage, and printers. the user is able to use drag and drop to perform actions on systems objects.
- AIX commitment to Open Systems.
- Data Encryption Standard.

Operating Systems and Development Environments (Desktop)

- Network File System™.
- Network Computing System™.
- Networking Facilities.
- IBM Software Support Services.
- AIX/6000 Support Family.
- System available on Tape or CD-ROM.
- CD-ROM Hypertext Information Base Library.
- Common Mode Development Static Libraries.

Reference Material

- AIX General Concepts and Procedures, publication number GC23-2202.
- AIX General Programming Concepts for RISC System/6000, publication number GC23-2205.
- Getting Started, publication number GC23-2521.

Ordering Information

- AIX Version 3 for RISC System/6000 (5756-030)

Availability

- Available now.

Contact

IBM Corporation

To order, contact IBM Direct:
Tel: (800) IBM-4YOU
Email: askibm@info.ibm.com
Web: <http://ibm-direct.e-com.ibm.com>

For licensing information, contact:
IBM RISC System/6000 Division
AIX OEM & Licensing/MS 9581
11400 Burnet Road
Austin, TX 78758
Tel: (512) 838-4075
Fax: (512) 838-3461

AIXwindows® Environment/6000

User Interface

IBM Corporation

AIXwindows Environment/6000 Version 1.2.5 is a state-of-the-art windowing system providing support for X Windows(1) Release 5 (X11R5) windowing/services for AIX Version 3.2.5 for RISC System/6000 (AIX/6000). AIX windows Environment/6000 version 1.2.5 is binary compatible with X Windows Release 4 (X11R4).

AIXwindows Environment/6000 provides a graphical interface to AIX Version 3.2.5 for RISC System/6000. It is based on and compatible with the industry-accepted X Window System and the OSF/Motif™ 1.2.2 graphical user interface, and can interact with other AIX and other equipment manufacturer systems implementing the X Window System and OSF/Motif interfaces. AIXwindows Environment/6000 provides a sophisticated graphical desktop (AIXwindows Desktop) that can be tailored for integrating and launching applications. AIXwindows Environment/6000 also provides the facilities to execute and develop windows applications, OSF/Motif applications, or applications requiring Display PostScript support.

In addition, the AIXwindows/3D feature provides the facilities for the execution and development of three-dimensional applications for scientific and engineering applications. These include 3D applications supported by graPHIGS™, OpenGL, GL, or PEX. 2D and 3D applications may be executed concurrently.

Features

- *AIXwindows Environment/6000 Version 1.2.5 (X11R5) has several enhancements to Version 1.2.4, including:*
 - AIXwindows Environment/6000 1.2.5 (X11R5)
 - Support for new graphics adapters.
 - Xterm Terminal emulation.
 - X Windows Color Management.
 - ISO fonts.
 - Display PostScript Level 2.
 - Crosshair & multicolor cursor.
- *AIXwindows/3D Feature Enhancements:*
 - SoftGraphics - Full software implementation of PEXlib 5.1, graPHIGS, and OpenGL 1.0 APIs.
 - graPHIGS Unicode Character Set and graPHIGS Image Workstation type.
 - PEXlib server XLFD font naming support and PEXlib online documentation.

Operating Systems and Development Environments (Desktop)

Reference Material

- AIXwindows Environment/6000 User's Guide, publication number (GC23-2432).
- AIXwindows Environment Desktop Reference Manual, publication number (SC23-2280).
- graPHIGS Programming Interface: Writing Applications, publication number (SC23-8192).
- AIXwindows Environment/6000, publication number (SK2T-0213).

Requirements

AIXwindows Environment/6000 Version 1.2.5 is designed to execute on the IBM RISC System/6000 POWERstations and POWER servers with AIX Version 3.2.5 for RISC System/6000.

Ordering Information

- AIXwindows Environment/6000 Version 1.2 (5601-257).

Availability

- Available now.

Contact

IBM Corporation

To order, contact IBM Direct:
Tel: (800) IBM-4YOU
Email: askibm@info.ibm.com
Web: <http://ibm-direct.e-com.ibm.com>

For licensing information, contact:
IBM RISC System/6000 Division
AIX OEM & Licensing/MS 9581
11400 Burnet Road
Austin, TX 78758
Tel: (512) 838-4075
Fax: (512) 838-3461

AIX® Version 4.2

Operating System, Utilities

IBM Corporation

AIX Version 4.2 represents a significant enhancement of capabilities to the AIX Version 4 operating system. AIX Version 4.2 delivers many new features in a system designed for usability and growth, and it maintains a high degree of commitment to binary compatibility with AIX Version 4.1.

AIX Version 4.2 supports your investments in previous IBM systems using the AIX operating system, and provides the following new features:

- *Large-File Support*—Supports the creation and use of data files larger than 2GB.
- *Dynamic Loading*—An API for dynamic loading of program objects.
- *Large Executables*—New support for executables with initialized data of sizes larger than 256MB.
- *Device Support*—Up to 1 terabyte.
- *New Entry Client Package*—A reduced-function client package at a lower price.
- *Bonus Pack for AIX Version 4.2*—New and popular software, making AIX Version 4.2 a rich, robust network computing environment.
- *Graphical Workspace Manager*—Enhances Common Desktop Environment (CDE) usability and management.
- *Networking Support*—Support for Network Time Protocol (NTP) and Authentication support for Point-to-Point Protocol (PPP).

AIX Version 4.2 has many additional performance enhancements in I/O, streams, networking, and C language run-time. It also adds support for the RISC System/6000™ 7024 E30 Server, additional I/O devices and other hardware extensions.

Features

- Provides the new Entry Client package.
- Provides support for:
 - Data files greater than 2GB.
 - Program executables greater than 256MB.
 - Merge of the LVM and CLVM function.
 - Graphical Workspace Manager.
 - Dynamic loading APIs.
 - AIX Version 4.2 year 2000 enabled.
- Received XOpen's UNIX(1) 95 Brand. The X/Open UNIX 95 brand signifies compliance with the X/Open Single UNIX Specification (also known as Spec 1170) and indicates that the operating system supports a common set of application programming interfaces (APIs) that enable greater portability of applications between UNIX systems.
- Provides a no-charge Bonus Pack that contains:
 - Ultimedia® Services for AIX, Version 2.1.4.
 - Netscape Navigator, Version 2.01.
 - IBM's implementation for AIX of Sun's Java(2) programming environment, Version 1.0.
 - Adobe Acrobat Reader, Version 2.1.
 - Netscape FastTrack Server.
 - Netscape Commerce Server, Version 1.1 (substituted for the Netscape FastTrack Server until availability of Netscape FastTrack Server).
 - IBM Internet Connection Secure Server for AIX.
- Provides for pre-install of RS/6000 Welcome Center.

Operating Systems and Development Environments (Desktop)

- Enhances
 - Hardware support.
 - Async and Networking.
 - National Languages.
 - X Window System XTEST Extension.

AIX Version 4.2 for Entry Client Package

AIX Version 4.2 expands the AIX family of operating system packages by introducing the new AIX Version 4.2 for Entry Client Package. This new package provides the same reliability, scalability, and industry-strength architecture that has come to be expected with AIX but with reduced function at a lower price. With the addition of the new AIX Version 4.2 for Entry Client, the previously announced AIX Version 4.1 for Clients package has been renamed for AIX Version 4.2 to AIX Version 4.2 for Workgroups. This name change was made to better identify this AIX package with its function as an advanced client with server capability.

The Entry Client Package includes:

- Uniprocessor support.
- A single user plus administrator (root user).
- The CDE.
- The Distributed Computing Environment (DCE) client.
- The full National Language Support provided in the larger AIX packages.

- Many popular PCI, ISA, and PCMCIA adapters found in the larger AIX Version 4.2 packages.
- IDE disk and CD-ROM support.
- SCSI support for disk devices, CD-ROM, and tape devices provided in the larger AIX packages.
- Support for all printers supported by the larger AIX packages.
- TCP/IP PPP.
- TCP/IP client.
- Serial Line Internet Protocol (SLIP).

Reference Material

- AIX and Related Products Documentation Overview, SC23-2456.
- IBM RISC System/6000 Site and Hardware Planning Information System Overview and Planning, SA38-0508.
- AIX Version 4 General Programming Concepts: Writing and Debugging Programs, SC23-2533.

Ordering Information

- AIX Version 4.2 (5765-655).

Availability

- Available now.

Contact

IBM Corporation

To order, contact IBM Direct:
Tel: (800) IBM-4YOU
Email: askibm@info.ibm.com
Web: <http://ibm-direct.e-com.ibm.com>

For licensing information, contact:
IBM RISC System/6000 Division
AIX OEM & Licensing/MS 9581
11400 Burnet Road
Austin, TX 78758
Tel: (512) 838-4075
Fax: (512) 838-3461

AIX® Version 4 Licensing

Operating System

IBM Corporation

AIX Version 4 licensed offerings are designed to support the needs of IBM customers and Other Equipment Manufacturers (OEMs). AIX Version 4 Licensed offerings include the following:

- *License to distribute AIX binaries on OEM PowerPC systems*—PowerPC systems manufacturers interested in a UNIX offering should consider AIX Version 4, which provides binary compatibility for over 10,000 software applications across a range of systems from laptops to teraflop class MPP systems.
- *Internal use Source code licenses*—Provide IBM customers the ability to customize their RS/6000 computing environments.
- *View-only source code licenses*—Provide IBM customers and ISVs greater insight into AIX function to enhance development and support of AIX applications
- *AIX Version 4 technology licenses*—Provide licensing of source code for AIX components, such as the Journaled File System, for incorporation into other OEM OS offerings.
- *AIX Version 4 source code license with rights to prepare and distribute derivative works*—Provides PowerPC system manufacturers the ability to port AIX to platforms that are not supported by binary AIX.
- *AIX Version 4.2 Portability Assist Layer (PAL license with rights to prepare and distribute AIX-trademarked derivative works*—Provides PowerPC system manufacturers with the source code, software products

and tools needed to port AIX to other PowerPC systems without requiring a full source-code license.

- *AIX Trademark License and Multi-Vendor Program (MVP)*—OEM source and binary licensees are encouraged to license the AIX trademark and participate in the AIX Multi-Vendor Program (MVP), which promotes binary compatibility of trademarked AIX across MVP participant platforms, produces compatibility and compliance test suites and performs ISV recruiting and support.
- *IBM Licensed Program Products (LPPS)*—IBM AIX software applications, such as compilers, software development environments, databases and network management applications are available for licensing in conjunction with AIX source or binary licenses.

Intended Use

AIX Version 4 offerings are intended for use on PowerPC hardware architectures.

Technical Support

The following technical support is available separately:

- Documentation.
- Consulting services.
- Training and education.
- Electronic question and answer.
- Development and Project Management support.

Operating Systems and Development Environments (Desktop)

Terms and Conditions

- AIX offerings are available under terms and charges specified in respective Licensing Agreement.
- Availability and use of the code is subject to third-party terms and conditions as may apply, including:
 - UNIX® System V, Release 3.2 or Release 4.0 Source Code License.
 - OSF/1 1.2 Source Code License.
 - OSF/Motif 1.2.4 Source Code License.
 - University of California Tahoe or Reno Version of Berkeley Software Distribution 4.3 Source Code License.
- PowerPC Microprocessor Family: The Programmer's Reference, publications number SA14-2090.
- PowerPC: Concepts, Architecture and Design, publications number SR28-5599.
- PowerPC System Architecture, publications number SR28-5783.
- Introducing AIX Version 4, publications number SC23-2534.
- AIX Quick Reference, publications number SC23-2529.
- AIX General Programming Concepts, publications number SC23-2533.

Reference Material

- PowerPC Architecture, publications number SA14-2082.
- PowerPC Microprocessor Family: The Programming Environment, publications number SA14-2089.

Availability

- Available now.

Contact

IBM RISC System/6000 Division

AIX OEM & Licensing/MS 9581
11400 Burnet Road
Austin, TX 78758
Tel: (512) 838-4075
Fax: (512) 838-3461

Windows NT™

Operating System

IBM Corporation

IBM and Motorola, working jointly and with support from Microsoft, have ported the Windows NT operating system to the PowerPC platform. Windows NT is a portable, preemptive, multi-tasking operating system. Windows NT on PowerPC platforms supports client server computing, downsizing and rightsizing, re-engineering, multimedia, object-oriented development tools, wireless connectivity, networking, 3D graphics, and new human interface technologies for emerging application environments.

Features

- *Performance*—32-bit, preemptive, multiuser, multitasking, multithreaded.
- *Ease of Use*—Windows 3.1 look-alike graphical user interface (GUI).
- *Reliability*—Data protection via disk mirroring:
 - Disk striping with parity.
 - UPS features.
 - Built-in tape backup.
 - C2-level security.
- *Open, Scalable Design*—Runs 16-bit and 32-bit applications for DOS, POSIX, and character-based OS/2 version 1x.
- *Networking*—well integrated with popular networking and communications software.

Operating Systems and Development Environments (Desktop)

Technical Support

The IBM Kirkland Programming Center located in Kirkland, Washington, has development, testing, application-porting facilities, and support resources available for hardware and software developers to port applications.

Availability

- Available now.

Contact

IBM Corporation

PowerPC Technical Support Center
3600 Carillon Point
Kirkland, WA 98033-7354
Tel: (206) 803-5821
Fax: (206) 889-4538
Email: winnppc@ibm.vnet.com

JAM

Utilities

JYACC, Inc.

JAM is a cross-platform tool for building client/server, three-tier and web-based transactional applications. JAM lets you build applications quickly and easily without sacrificing the control you need in the most complex and performance-critical areas. JAM applications can run unmodified on a wide range of platforms, including PowerPC processor-based systems, and in many operating environments, including Windows, Windows 95, Windows NT, Motif, OS/2 Warp, Macintosh, Open VMS and virtually every implementation of UNIX. JAM also integrates seamlessly with a broad spectrum of RDBMS products, and provides transparent access to legacy systems via DRDA and Microsoft's ODBC.

JAM WEB (Web Enterprise Builder)

JAM WEB is a development environment for building fully transactional database applications on the World Wide Web. JAM WEB provides a graphical drag and drop environment for building and deploying database forms that run on a Web server. JAM WEB automatically converts the forms into dynamic HTML for display on any current Web Browser. The generated HTML can include both data and action controls, enabling you to build fully interactive, multi-screen transaction-oriented applications.

JAM/TPi

JAM/TPi is a development environment for building partitioned, multi-tier transactional applications. With JAM/TPi, a single graphical tool can be used to develop both client and server application components, with the server modules running under the control of the popular TP monitor, TUXEDO. JAM/TPi server applications can run with JAM-built clients or with other popular client-building tools.

JAM/ReportWriter

JAM/ReportWriter version 7 adds a report-writing component to JAM, a second generation tool for building client/server and three-tier enterprise applications. JAM/ReportWriter provides sophisticated reporting capabilities to developers of JAM applications. JAM/ReportWriter also produces stand-alone reports.

Jam/ReportWriter fully leverages JAM's Visual Object Repository, Transaction Manager and Wizard technologies. This makes it possible for everyone on the development team to quickly and easily generate complex reports that incorporate business graphics and data from multiple sources.

Availability

- Available now.

Contact

JYACC, Inc.
116 John Street
New York, NY 10038
Tel: (800) 458-3313
Tel: (212) 267-7722
Fax: (212) 608-6753
Email: jammin@jyacc.com
Web: <http://www.jyacc.com>

Motorola Hardware Abstraction Layer (HAL) Kit for Windows NT™

Code, Specification, Test Suite, Utilities
Motorola, Inc.

The Motorola PowerPC Architecture Hardware Abstraction Layer (HAL) kit for Windows NT consists of a set of functions that abstract the dependencies between Windows NT and the underlying PowerPC hardware platform. The kit enables a single version of the Windows NT kernel to run on all uniprocessor 32-bit PowerPC microprocessor platforms. It also abstracts multiprocessor issues, so a single multiprocessor version of the kernel can run on all 32-bit PowerPC multiprocessor platforms.

The HAL kit helps you develop ports of the Windows NT operating system to new PowerPC platforms and enables a device driver to support the same device across all PowerPC platforms. The device driver describes its resource requirements to the HAL, and the HAL translates those requirements to the specific hardware platform on which it is running. The functions used to abstract these differences are bound to the kernel by the OSLoader during the boot phase. After the firmware initializes any hardware required for booting, the HAL ensures that the base system hardware (bus controllers, interrupt controllers, timers, etc.) is initialized for the specific platform.

Features

The abstracted platform characteristics include:

- Initialization.
- I/O bus mapping and access.
- Hardware interrupts.
- DMA.
- Real-time clock and timers.
- Basic console I/O.
- Multiprocessor support.
- Cache support.

Contents

- HAL Source Code for PowerPC Platform.
- HAL Specification for PowerPC Interfaces.
- HAL Test Suite.
- HAL Porting Guide—explains hardware dependencies within the HAL, installation, test suite, execution and debugging techniques.

Devices Supported

- PowerPC 601 microprocessor.
- PowerPC 603 microprocessor.
- PowerPC 604 microprocessor.

Operating Systems and Development Environments (Desktop)

Hosts Supported

- Native PowerPC systems running Windows NT v3.5.
- Intel 386 or higher systems running Windows NT v3.5.

Availability

- Available now.

Technical Support

Full-time technical staff provide support via voice, fax and Internet:

- ppcinfo@risc.sps.mot.com
- <http://www.mot.com/PowerPC/>
- 1-800-347-8384 voice

Contact

Motorola, Inc.

For additional information, call 1-800-347-8384 or
Tel: 512-891-2999
Fax: 512-891-3798
Email: ppcinfo@risc.sps.mot.com
Web: <http://www.mot.com/PowerPC/>

PowerPC Boot Firmware

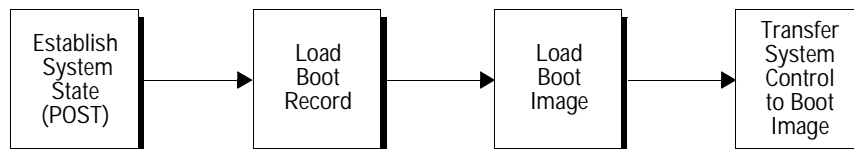
Code

Softex

Softex's PowerPC Boot Firmware is a fully reconfigurable, graphically-oriented Common Hardware Reference Platform compliant tool for initializing any combination of PowerPC hardware and operating system. It handles power-on self test (POST), console configuration, password access control (optional), and operating system boot. The following devices are tested:

- PowerPC microprocessor.
- Main system memory.
- System planar devices (i.e., on-board peripherals).
- Floppy diskette drives.
- IDE hard disk drives.
- Video display controllers.
- Keyboard.
- PS/2-compatible mouse.
- Real-time clock.
- SCSI hard disk drives and CD-ROM drives.
- PCMCIA interface.

The POST has a completely modular design so that future expansion and customer-specific extensions can be easily accommodated. The current selection of modules already exceeds the list of PowerPC boot-critical components. A setup utility with a graphical user interface follows the POST and helps resolve any conflicts between address mapping, interrupt requests (IRQs), etc., that may require changing settings in the non-volatile RAM or adapter cards.



Operating Systems and Development Environments (Desktop)

Features

- Power-On Self-Test (POST) for system and peripherals.
- Setup utility with graphical user interface.
- PowerPC Reference Platform compliant.
- Advanced RISC Computing (ARC) compliant code for Windows NT boot.
- Open Firmware Standard (IEEE P1275) compliant.
- 80x86 real-mode emulator for executing adapter ROM code. Compatibility with existing PCI video cards.

Operating Systems Supported

- Windows NT
- Workplace OS
- AIX
- OS/Open
- Mac OS
- Solaris
- NextStep

Availability

- Available now.

Contact

Softex

Mahendra Bhansali
6609 Cuesta Trail
Austin, TX 78730
Tel: (512) 452-8836
Fax: (512) 795-8702
Web: <http://www.eden.com/~softex>

Real-Time Operating Systems

Nucleus PLUS

Debugger, Operating System, Real-Time Tool, Utilities

Accelerated Technology, Inc.

Accelerated Technology provides PowerPC developers unsurpassed real-time support with its Nucleus PLUS real-time kernel. Nucleus PLUS enhances development of real-time applications that require the performance of the PowerPC superscalar microprocessor.

Nucleus PLUS eliminates the need for execution-resource allocation in the application software. When a more important task requires execution, Nucleus PLUS suspends the currently executing task and starts the pending task. After the important task is finished, the suspended task is resumed.

Nucleus PLUS also provides facilities that include task communication, task synchronization, timers, and memory management. Nucleus PLUS includes dynamic creation of all Nucleus PLUS objects, queues, mailboxes, timers, pipes, and priority or first-in-first-out (FIFO) driven supervision on all Nucleus PLUS objects. Nucleus PLUS also includes the Advanced Interrupt Management Mechanism (AIMM) which virtually eliminates interrupt latencies.

Nucleus PLUS incorporates a micro-kernel philosophy which facilitates additions to the real-time operating environment by providing standard I/O-device interfaces. The micro-kernel philosophy allows for creation of new service-call interfaces by combining existing interfaces.

Nucleus PLUS facilities have been designed to be highly deterministic. Accelerated Technology provides worst-case times for interrupt latencies and service-call overhead on a processor-by-processor basis. Task switches are fixed in time and are not dependent on the system configuration. Accelerated Technology supports both the DIAB/DATA and Software Development Systems (SDS) PowerPC development tools.

Standard Features

- Priority-based, preemptive or non-preemptive, time-slicing kernel.
- Complete ANSI C source code.
- One-time license fee per end-user product (no royalties).
- Appropriate for loading in ROM.
- Prioritized scheduling of user-defined tasks.
- Dynamic allocation of all Nucleus PLUS objects.
- Task communication through user-defined public queues.
- Queue item-size defined by user.
- Optional task suspension on full queues.
- Fixed- and variable-sized queues.
- Event flag management for task synchronization.
- Optional consumption of event flags resource management using semaphores.
- Predictable fixed-length memory management.
- Flexible variable-length memory management.
- Optional task suspension when memory is unavailable.
- Optional timeout available for any task suspension.
- User selectable FIFO or priority order for timeout lists on queues, events, resources, pipes, fixed memory, variable memory, etc.
- System history log.
- Advanced Interrupt Management Mechanism (AIMM).

Real-Time Operating Systems

Technical Support

- Well engineered and documented source code.
- Programmer's Reference Manual and Internals Manual.
- Telephone support.
- BBS support.
- Training available.

Availability

- Available now.

Contact

Accelerated Technology, Inc.

P.O. Box 850245
Mobile, AL 36685
Tel: (334) 661-5770
Tel: 1-800-468-6853
Fax: (334) 661-5788
Email: sales@atinucleus.com
Web: <http://www.atinucleus.com>

RTXC

Debugger, Operating System, Real-Time Tool

Embedded System Products, Inc.

RTXC is a flexible, field-proven, multitasking real-time kernel for use in a wide variety of embedded applications. It is written primarily in C and features a single Applications Programming Interface for all supported processors. The result is a configurable, multitasking architecture.

RTXC manages tasks and time, synchronizes with events, and permits movement of data within the application. But RTXC goes beyond basic requirements through its extensive set of understandable kernel services, each operating on one of seven classes of kernel objects. In addition to the fundamental requirements, RTXC also contains kernel services for RAM management and exclusive access to any entity.

While all this capability can be found in RTXC, you remain in control. RTXC is distributed in source code form so that you may easily include only those Kernel Objects and Kernel Services you need in your application and eliminate the others.

RTXC is noted for its understandable function names which make it easy to learn and easy to use. That translates to less time spent on system software issues and more time to spend on developing the application. RTXC is licensed per product and is free of royalties.

Features

- Multitasking with preemptive, round robin and time-sliced task scheduling.
- Intertask communication and synchronization via semaphores, messages, and queues.

- Efficient timer management.
- RAM management through static and dynamic Memory Partitions.
- Resource management for exclusive access needs.
- Source code permits flexible configuration and easy customization.
- Highly acclaimed 600+ page User's Manual.

Interrupt Management

RTXC provides a generalized design for servicing interrupts in an efficient yet flexible manner achieving minimum interrupt latency and maximum responsiveness.

System Generation Utility

RTXCgen is an interactive program used to define the kernel objects needed for the application. Objects are defined in a simple interactive dialog with the program. When all definitions are complete, RTXCgen produces C source code of the kernel objects. The result is error free system generation.

System Level Debug Task

During the debugging phase, RTXCbug may be employed as a task to examine the interaction between the application tasks and RTXC. RTXCbug remains blocked and consumes no CPU time until invoked by the process or by operator intervention. When in use, RTXCbug displays coherent snapshots of the various classes of kernel objects showing current states and relationships with other objects.

Real-Time Operating Systems

Warranty and Support

RTXC carries a standard 12-month initial warranty and support period. If you have a question, you are backed up by a highly acclaimed user's manual of over 600 pages and knowledgeable telephone support by the engineers who wrote RTXC.

Training

RTXC Training Classes are held each month in Houston and feature a combination of lecture and hands-on exercises. Training classes at

customer's sites are available by special arrangement. Call for schedule details and prices.

Requirements

Supported host development environments include:

- MS Windows 3.1 or later.
- SunOS 4.1.3 or later.

Availability

- Available now for PowerPC 403GA, 601 and 603 microprocessors.

Contact

North America

Embedded System
Products, Inc
11501 Chimney Rock
Houston, TX 77035-2900
Tel: (800) 525-4302
Tel: (713) 728-9688
Fax: (713) 728-1049
Email: sales@esphou.com

Europe

Cosmic S.A.R.L.
33, Rue Le Corbusier
94035 Creteil Cedex
France
Tel: +33-1-43.99.53.90
Fax: +33-1-43.99.14.83
Email: mf@cosmic.cosmic.fr

South Africa

Eagle Technology
31-35 Hout Street
Cape Town 8000
South Africa
Tel: +27-21-23-4943
Fax: +27-21-24-4637
Email: davidt@aztec.co.za

Japan

NPS, Inc.
Shuwa Yoyogi Building
4-26-15 Sendagaya Shibuya-ku
Tokyo, 151 Japan
Tel: +81-33-4050511
Fax: +81-33-4055410
Email: an@nps.twics.com

Australia/New Zealand

Alfa-Tek Australia
Unit 6, 42-50 Stud Road
Bayswater, Vic 3153
Australia
Tel: +61-3-720-5344
Fax: +61-3-720-5268
Email:
wwfiala@ozemail.com.au

Israel

Agam Cross Systems, Ltd.
"ATIDIM" Neve Sharet
Tel Aviv
Israel
Tel: +972-3-648-4121
Fax: +972-3-647-8365
Email: agam@elronet.co.il

Israel

ITEC, Ltd.
"ATIDIM" Neve Sharet
Tel Aviv
Israel
Tel: +972-6-491-202
Fax: +972-6-497-661
Email: itec@netvision.net.il

Taiwan

EXARTECH International
Corp.
10F-82 Chung-Cheng S.
Road
Sanchung, Taipei,
Taiwan
Tel: +886-2-977-6828
Fax: +886-2-977-6829
Fax: +886-2-978-9927
Email: idpt182@tpsl.seed.net.tw

OSE Delta® Real-Time Operating System

Operating System, Real-Time Tool

Enea OSE Systems

OSE Delta is a message-based real-time operating system for distributed and fault-tolerant systems, allowing exchange or addition of software and hardware during runtime. The signal handling within OSE is extremely efficient, resulting in very high data throughput rates, making it ideal for high performance communications applications. OSE also offers a modern, high-level approach to the development of real-time systems. Most applications can be programmed with a subset of less than ten OSE calls. This results in a great clarity of design and much faster code development.

The OSE Delta API enables a UNIX program to communicate transparently with a distributed OSE system. Non-time-critical parts of the application may execute as OSE processes on the UNIX system while interacting with other UNIX programs or resources. By using OSE Delta Soft Kernel, the application may be simulated and tested in the host environment before moving it to target hardware.

The OSE Delta DDS provides debugging at the system level and allows fully symbolic debugging. The DDS can be used in

combination with any industry standard source code debugger such as XRAY, D-Tective, SingleStep, GDB, and XDB. Networking facilities and an advanced POSIX-compliant file system are also available for OSE Delta.

OSE is widely used among some of the world's largest companies in applications ranging from engine control and mobile phones, to major telecom switches. Enea OSE Systems offers a qualified and experienced support organization and extensive training, and all product development and services are carried out according to the industry quality standard ISO 9001.

Features

- Supports distributed systems.
- Dynamic reconfiguration features.
- UNIX interface.
- Support for fault-tolerant systems.
- Automatic supervision.
- Powerful debug environment.
- High performance.
- Easy to use.

Real-Time Operating Systems

PowerPC Processors Supported

- PowerPC 603 microprocessor.
- PowerPC 403 embedded controller.

Host Systems Supported

- Sun Workstation.
- Hewlett-Packard Workstation.
- PC.

Availability

- Available now.

Contact

ENE DATA AB

Nytorpsvagen 5B
P.O. Box 232
S-183 23 TABY
SWEDEN
Tel: 46 (0)8 638 50 00
Fax: 46 (0)8 638 50 50
Email: info.ose@enea.se
Web: <http://www.enea.se/ose>

ENE DATA Software GmbH, Germany

Tel: 49 (0)89 59047 251
Fax: 49 (0)89 59047 200

Distributors and Local Offices

Germany

ENE DATA Software GMBH
Arnulfstrasse 27
D0800335 Munchen
Tel: +49 89 59 04 72 51
Fax: +49 89 59 04 72 00

BeNeLux

Air-Parts B.V.
P.O. Box 255
NL-2400 AGALPHEN AAN DEN RIJN
Tel: +31 172 422 455
Fax: +31 172 421 022

France

MB Electronique S.A.
606, Rue Fourny - Z.I.
B.P. 31
F-78533 BUC CEDEX
Tel: +33 1 39 56 81 31
Fax: +33 1 39 56 53 44

Israel

Telsys Ltd.
Dvora Hanevia Str.
Neve Sharet, Atidim Bldg. 3
TEL-AVIV 61 431
Tel: +972 3 6492001
Fax: +972 3 6497407

Italy

Special Ind. SpA
Piazza Spotorno, 3
I-20159 MILANO
Tel: +39 2 66 80 51 77
Fax: +39 2 66 80 04 93

Switzerland

Litronic AG
Fiechthagstrasse 19
CH-4103 BOTTMINGEN
Tel: +41 61 421 32 01
Fax: +41 61 421 18 02

United Kingdom

Reflex Technology Ltd
3, Buckingham Place
Bellfield Road
HIGH WYCOMBE
Bucks. HP13 5HW
Tel: +44 1494 46 59 07
Fax: +44 1494 46 54 18

PowerUX™ Operating System

Operating System, Real-Time Tool, Libraries, Utilities

Harris Computer Systems Corporation

PowerUX is a real-time operating system that provides industry-standard (System V Release 4.2 MP) UNIX® for platforms based on the PowerPC 604 microprocessor. PowerUX features high I/O throughput, fast response to external events and efficient interprocess communication. PowerUX supports the real-time interfaces defined in the IEEE POSIX standard 1003.1b-1993 and is designed for maximum real-time performance and functionality. The kernel is multithreaded and fully preemptive. PowerUX is based on the Real-Time/PowerUX operating system from Harris Computer Systems Corporation (HCSC). PowerUX brings all of Real-Time/PowerUX's features and real-time kernel technology to low-cost off-the-shelf VME single-board computers.

Features

- Real-time, UNIX-based.
- Industry-standard System V Release 4.
- Supports PowerPC 604 microprocessor-based platforms.
- Software development environment from vendor includes:
 - Integrated common compiler suite (C, Fortran and Ada).
 - NightStar™ real-time software development tools.
- Expandable interconnectivity and networking.
- Preemptive, multithreaded (re-entrant) kernel.
- Minimal process dispatch latencies.
- Compatibility with HCSC's PowerPC microprocessor-based Night Hawk® Real-Time PowerUX™.
- Optional kernel extension provides B2-level security (PowerSX™).

- Single-vendor support for OS, compilers and software development tools.
- Open systems standards:
 - OSIX™ 1003.1-1990
 - POSIX 1003.1b-1993
 - POSIX 1003.5
 - POSIX 1003.9
 - VID Issue 3
 - XPG3
 - ANSI C
 - ANSI Fortran 77 with MIL-STD-1753

Multithreading and Preemption

A multithreaded kernel allows multiple processes to execute in the kernel simultaneously. The kernel protects key data structures and critical sections of code with semaphores and spin locks to preserve the integrity of the system. With this implementation, processes contend with each other only when requesting the identical resource. Otherwise, all kernel features and capabilities are available to users.

A significant benefit of a multithreaded kernel is that a process executing in the kernel can be forced to relinquish the CPU involuntarily. The kernel can transfer control of the CPU from a lower-priority process to a higher-priority process. This allows a high priority process waiting for an external event to respond immediately when the event occurs - even if the CPU is currently in use.

The degree of multithreading or the length of critical sections is key to minimizing worst-case response times by reducing interrupt latency. The fine-grain multithreading implementation of the PowerUX kernel ensures that critical sections are extremely short.

Real-Time Operating Systems

Features such as rapid context switches, an efficient preemption mechanism and low-interrupt latencies combine to provide for low dispatch latencies.

In addition to the standard communication components of the UNIX operating system (e.g., uucp, ftp), a full range of networking capabilities is optionally available. These include FDDI, Ethernet™, TCP/IP, NFS™ and the X Window System™ (including OSF/Motif™). PowerUX supports multiple interfaces and networks simultaneously.

Real-Time Features

- *Static Priority Scheduling*—A configurable range of static real-time priorities is provided.
- *Shared Data and Synchronization*—Access to shared data is provided through the shared-memory system services or the POSIX memory mapping services. A shared-memory definition utility is also provided for ease of use and control. A set of library routines and system calls allows user applications to solve problems associated with sharing data among cooperating processes.
- *Physical Address Mapping Shared*—Memory regions may be bound to specific physical addresses including the VME I/O address ranges.
- *User Interrupt Routines*—User-written software that responds directly to hardware interrupts may be used.
- *Memory Locking*—The pages of frequently-executed tasks may be made memory resident so they are ready to execute without demand paging. This feature improves predictability for real-time applications and increases system throughput by reducing overhead in transaction-intensive applications and applications with many concurrent tasks.
- *Asynchronous I/O*—Asynchronous I/O allows a user process to perform other tasks while an I/O completion notification can be selected on a per-process basis. Asynchronous I/O can be performed to any device or disk file supported by PowerUX.
- *High Resolution Clocks and Timers*—Time-of-day clocks and interrupting timers are available with microsecond resolution.
- *Direct Disk I/O*—The raw asynchronous I/O feature allows programs to bypass the kernel's buffer cache and write the user's data buffer directly to the disk.
- *Threads*—The threads library provides the interfaces used to manage and synchronize multiple threads of control in a single process.

Availability

- Available now.

Contact

Harris Computer Systems Corporation

Real-Time Systems Division
2101 W. Cypress Creek Road
Ft. Lauderdale, FL 33309
Tel: (800) 666-4544 ext. 5469
Tel: (954) 973-5469
Email: nhnews@mail.hcsc.com
Web: <http://www.hcsc.com>

OS Open™

Debugger, Libraries, Operating System, Real-Time Tool, Utilities

IBM Corporation

The OS Open real-time operating system provides a scalable run-time and development environment for embedded systems running on PowerPC™ processors. The OS Open operating system embodies the IBM commitment to open systems and industry standards. This commitment protects application software investments and enhances portability.

As a provider of microprocessors and operating systems for embedded systems, IBM is uniquely qualified to supply integrated solutions yielding superior performance, and providing for a turn-key operation.

The OS Open operating system is designed to exploit the PowerPC Architecture, and has the following features:

- Easy installation and configuration.
- Support for ANSI C and POSIC standards.
- Open network interfaces.
- Support for real-time systems.

The OS Open operating system comprises a full-featured real-time executive and a rich collection of optional libraries.

Compact, Fast Real-Time Executive

The real-time executive provides the basic services defined in the draft POSIX real-time standards. Used alone, the real-time executive meets the needs of memory-constrained deeply embedded systems. Developers can add libraries to the operating system to meet a wide variety of embedded systems functional requirements.

ANSI C Library

The ANSI C library provides source-code portability, reducing the effort required to port application software.

TCP/IP Networking

The network library provides Berkeley 4.3 TCP/IP networking interfaces, including sockets, RPC and NFS. Utilities such as ping, ifconfig, FTP, and Telnet are also included. The network library supports Token Ring, Ethernet, and Serial Line IP (SLIP) attachments.

Device I/O

The device I/O library supports the POSIX file and device access model. Users can easily add or remove device drivers, even while an OS Open operating system is running.

DOS File System

Application programs can create, read, write, and delete DOS files and directories. User-supplied device drivers can handle any DOS-formatted media.

OpenShell

OpenShell, a powerful interactive native tool for debugging and system testing, can display memory, control blocks, and disassembled instructions. The C interpreter allows developers to call any function from a command line and interactively define C functions.

Remote Debugger

The OS Open operating system interfaces with either RISCWatch or rxde to provide RTOS-aware system debug. Versions of OS Open are available to support both XCOFF and ELF module formats and ABI conventions. For XCOFF, OS Open provides rxde, a complete remote C source-level debugger for the X Window System. Familiar xde menus are tailored to display OS Open information. The

Real-Time Operating Systems

ELF debugger solution is RISCWatch, providing C source-level debug via a multi-window user interface. The host system and target OS Open embedded system communicate using TCP/IP.

Built for the PowerPC Architecture

Unlike operating systems developed for CISC processors, the OS Open operating system is designed for and exploits the PowerPC Architecture™ and IBM's RISC optimization technology.

Easy Installation and Configuration

Board support packages for popular board-level products provide plug-and-play installation.

Supports POSIX Standards

POSIX programming interfaces speed system development and offer new levels of code portability and reuse for embedded systems.

Support for Hard Real-Time Systems

The OS Open operating system provides the mechanisms required for hard real-time systems, including deterministic execution, priority inversion, and periodic scheduling. The OS Open operating system can be configured to meet the requirements and constraints of a wide variety of embedded systems.

Host Systems

- IBM RISC System/6000™ running AIX 3.2 or 4.1.
- 386, 486 or Pentium running DOS/Windows 3.1 with a Windows Sockets-compatible TCP/IP protocol stack.
- SPARCStation or equivalent running Solaris 2.3 or SunOS 4.1.3 with OpenWindows.

Availability

- Available now.

Contact

United States and Canada

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531
Tel: (800) PowerPC
Fax: (800) POWERfax

IBM homepage:
<http://www.ibm.com>

IBM Microelectronics homepage:
<http://www.chips.ibm.com>

Fax Service: (415) 855-4121

Europe

IBM
La Pompanne BP 1021
34006 Montpellier
France
Tel: (33) 6713-5757 (French)
Tel: (33) 6713-5756 (Italian)
Fax: (33) 6713-5750*
*from Paris add 16

IBM
Informations Systeme GmbH
Laatzener Str. 1
30539 Hannover
Germany
Tel: (49) 511-516-3444 (English)
Tel: (49) 511-516-3555 (German)
Fax: (49) 511-516-3888

Japan

IBM
800, Ichimiyake,
Yasu-cho, Yasu-gun
Shiga-ken, Japan 520-23
Tel: (81) 775-87-4745
Fax: (81) 775-87-4735

MTOS-UX/PPC™

Operating System, Real-Time Tool

Industrial Programming, Inc.

MTOS-UX for PowerPC microprocessors is a member of the MTOS-UX family of real-time operating systems. All versions of MTOS-UX have the same programmer interface. Application software, when written in C, is portable from platform to platform.

MTOS-UX is specifically designed for high speed, compactness, portability, and generality. It is widely used in communications, process control, medical instrumentation, factory automation and broad variety of other embedded systems.

Features

- *Dynamic objects*—All objects (tasks, mailboxes, event flags, memory pools, etc.) can be created and deleted under MTOS-UX.
- *Full coordination system*
 - Event flags to coordinate multiple asynchronous events.
 - Semaphores for controlling access to critical regions.
- Signals provide software interrupts.
- Mailboxes for message transfer and coordination.
- Time-outs for all services whose completion may be delayed.
- *C language compatibility*—MTOS-UX assumes that applications are written in C. There is no run-time interface, with its associated overhead.
- *Multi-processor support*—MTOS-UX supports up to 16 CPUs on a common bus in a tightly-coupled configuration. MTOS-UX is a symmetrical, transparent multi-processor system. It is a virtual single-processor system.
- *UNIX™ portable library*—Included as part of the standard package.
- *Development hosts*—All commonly used equipment, such as UNIX-based workstations and DOS/Windows-based PCs may be used.
- *Enabled interrupts*—MTOS-UX nearly always runs with interrupts enabled.

Real-Time Operating Systems

System Requirements

- About 35 KB code space for the kernel.

Availability

- Available now.

Contact

Industrial Programming, Inc.

Bernard Mushinsky
100 Jericho Quadrangle
Jericho, NY 11753
Tel: (800) 365-MTOS
Tel: (516) 938-6600
Fax: (516) 938-6609
Email: bernard@ipi.com
Web: <http://www.ipi.com>

pSOSystem™

Debugger, Operating System, Real-Time Tool, Utilities

Integrated Systems, Inc.

pSOSystem for PowerPC microprocessors is a modular, high quality real-time operating system and development environment designed specifically for the embedded microprocessor market. It has achieved widespread industry recognition as one of the world's most efficient and reliable embedded operating systems. And Integrated Systems is enhancing that reputation by providing some of the most advanced and productive graphical design, development and debugging tools available in the industry today.

pSOSystem software integrates the fully deterministic pSOS+™ real-time kernel and pROBE+™ debugger with multiprocessing, STREAMS and TCP/IP networking, SNMP network management, client-server NFS, real-time and DOS compatible file systems. pSOSystem software is supported by an integrated cross-development environment that can reside on UNIX workstations or DOS PCs. It includes complete language support for C and C++ and a powerful cross debug environment that supports source and system level debugging and profiling.

Features

- Scalable, deterministic multitasking operating system optimized for PowerPC applications.
- Integrated C/C++ development tools.
- Flexible, industry standard networking facilities.
- MS-DOS CD-ROM (ISO 9660) and real-time UNIX compatible file systems.
- Source code support for commonly available peripheral chips and evaluation boards.
- Graphical design, development and debugging tools.

pSOS+ and pSOS+m™

pSOS+ provides a core set of multitasking services, including priority-based task scheduling, time management, two memory allocation schemes along with four different communication and synchronization mechanisms between tasks or tasks and interrupt service routines (ISR). pSOS+m, the multiprocessing version of pSOS+, allows application tasks to be distributed over several processor nodes, exchanging data and synchronizing as if running on a single processor.

pNA+™ and OpEN™

pNA+ allows real-time tasks to communicate with any system supporting TCP/IP protocols. OpEN provides a STREAMS based networking environment.

pHILE+™

The file system manager provides a high-performance file system structure and an MS-DOS file system organization, and ISO 9660 CD-ROM support. pHILE+ provides a superset of UNIX file system capabilities, including UNIX-like path name conventions, function call interfaces and hierarchical file structures. It can also read and write any standard IBM PC floppy format.

ESp™

ESp is the industry's most sophisticated visual tool for monitoring and debugging complex multitasking embedded applications. It maps execution tasks, interrupts and objects over

time, using icons to indicate events such as context switches, interrupts and semaphores. Its event triggering capabilities and customizable filtering enable developers to zero in on problems, even after a system crash. ESp networking functions permit target sharing and remote debugging of applications anywhere in the world.

Training, Service and Support

Customer services include training, a pSOSystem email users' group, and on-site field application engineering.

Requirements

Host development environment requires either AIX (3.2.5 or later) or SunOS™ (4.13 or later) or Solaris 2.4 or Windows 3.1 or later.

Availability

- PowerPC 602, 603, and 604 support, available now.
- PowerPC 403 support, available now.

Contact

Integrated Systems, Inc.

201 Moffett Park Drive
Sunnyvale, CA 94089
Tel: (408) 542-1500
Fax: (408) 542-1950
Email: scg_sales@isi.com
Web: <http://www.isi.com>

Great Britain

Integrated Systems, Ltd.
Unit 5, Meadway Court
Rutherford Close
Stevenage, Herts SG1 2EF
Tel: (44) 1438 751651
Fax: (44) 1438 312311

Japan

Integrated Systems, Inc.
9F Asahgin Gotanda Bldg
1-23-9 Nishi Gotanda
Shinagawa-Ku
Tokyo 141, Japan

Sweden

Integrated Systems, SA
Ynglingarängen 3
Jabosberg Centrum, Stockholm
Pstäl: Box No. 140
Sweden
Tel: (46) 85 80 89950
Fax: (46) 85 80 89959

Germany

Integrated Systems Inc, GmbH - Munich
Starnberger STR 22
82131 Gauting, Munich
Germany
Tel: (49) 89 850 6081
Fax: (49) 89 850 8918

Integrated Systems Inc, GmbH - Mainz
55128 Mainz
Bürogebäude Am Schleifweg 16, Germany
Tel: (49) 6421 91 0285
Fax: (49) 6421

C EXECUTIVE® and PSX™

Debugger, Operating System, Real-Time Tool, Utilities

JMI Software Systems, Inc.

C EXECUTIVE, a real-time, multitasking kernel for embedded applications, has supported a wide variety of microprocessors since 1981. C EXECUTIVE provides a complete and efficient run-time environment optimized for the C language.

The PowerPC is the eighth RISC processor supported by C EXECUTIVE. The kernel, 95% written in portable C, has been optimized for the use of the C language on RISC processors. The combination of a widely-used portable kernel and the PowerPC provides reliable real-time software on the latest RISC architecture.

Customer products employing C EXECUTIVE include X Window terminals, laser printers, cardiac monitors, SCADA systems, FAA and military radar systems, process control products, color ink jet printers, cellular telephone systems, military avionics, and a variety of time-critical applications.

PowerPC customers are using C EXECUTIVE for laser printers, GPS receivers, space programs, mainframe interconnection, and laboratory instruments.

PSX adds 56 POSIX.1 system calls to C EXECUTIVE, providing a 60% subset of POSIX.1. PSX is a single-user, single-group, multi-process execution environment. PSX provides a smooth migration path from C EXECUTIVE to full POSIX.

Features

- Real-time, multitasking kernel optimized for the C language.
- Fast system call mechanism for C programs.
- Fully prioritized, preemptive scheduler based on interrupts.
- Multiple methods of inter-task communication (semaphores, data queues, events, and signals).
- Complete standard C language I/O subsystem built in.
- 57 system calls for task scheduling, time control, dynamic memory allocation, task coordination, I/O, performance profiling, and stack checking.
- PSX adds 56 system calls from POSIX.1.
- ROMable, reentrant Portable C library of 100 functions.
- Optional DOS compatible file system—CE-DOSFILE™.
- Optional TCP/IP communications package—CE-TCP™.
- Optional SNMP package—CE-SNMP™.
- System level debugger, CE-VIEW™, allows dynamic system testing.
- Ready to use with standard PowerPC C compilers.
- Full set of device drivers for Sandalfort Development Board.

Real-Time Operating Systems

Technical Support

- Direct factory support for all products.
- International distributors with technical staff support.
- Warranty, annual update and maintenance service.
- Training customized to user's needs.
- Extensive consulting and contract services available.

Availability

- Available now.

Contact

JMI Software Systems, Inc.

904 Sheble Lane
P. O. Box 481
Spring House, PA 19477
Tel: (215) 628-0840
Fax: (215) 628-0353
Email: inquiries@jmi.com
Web: <http://www.mcb.net/jmi/>

Europe

RTS
M & G House, Head Road
Douglas, Isle of Man, IM1 5BF
British Isles
Tel: +44 1624 623841
Fax: +44 1624 623004
Email: alan@mannel.mcb.net

Japan

Advanced Data Controls Corp.
Nihon Semei Otsuka Building
No. 13-4 Kita Otsuka 1-Chome, Toshima-Ku
Tokyo 170, Japan
Tel: +81 3 3576 5351
Fax: +81 3 3576 1772
Email: kawahara@adac.co.jp

India

Software Development Systems
85, Narayanappa Block
R.T. Nagar II Block
Bangalore, 560 032, India
Tel/Fax: +91 80 3430219
Email: drs@sdsblr.uunet.in

Korea

Zeus Computer Co. Ltd.
506 Jung Ang Building
44-26 Yoido-Dong
Youngdeungpo-Ku, Seoul, Korea
Tel: +82 2 784 7841
Fax: +82 2 784 7844

Taiwan

Soljet Computer Co. Ltd.
5F-1, No. 237, Section 3
Roosevelt Road
Taipei, Taiwan, R.O.C.
Tel: +886 2 366 0080
Fax: +886 2 366 0315
Email: martnfan@tps1.seed.net.tw

AMX™ PPC32 Real-Time Multitasking Kernel

Operating System, Real-Time Tool, Utilities

KADAK Products Ltd.

AMX is a full-featured, real-time multitasking kernel for a wide range of target processors. AMX PPC32 supports both the PowerPC™ 400 and 600 families of microprocessors. AMX PPC32 has been tested on the IBM PPC403GA Evaluation Board and on the PowerPC 603 processor. The AMX family of kernels, first released in 1980, is used by more than 1,000 product development companies worldwide.

AMX is a simple, readily understandable software development tool which meets the stringent requirements of all real-time applications. Restart procedures kick the system off the ground. Tasks execute in response to requests from other tasks, from

interrupt service procedures or from timer procedures. Tasks can create other tasks. Interrupt service procedures handle the specifics of the hardware configuration, service the device in question and send messages to tasks to handle the more complex processing associated with the event. Timer procedures provide precise interval measurement and can be used to provide periodic requests for task execution.

AMX is delivered ready for development on a PC with DOS or Windows. Source code of all AMX modules is provided with AMX to permit AMX to be ported to any development platform. A sample program is provided to illustrate the proper use of many of the AMX services.



PHOTO #1
(location marker only—
do not use keyline)

AMX PPC32 is delivered in library object format ready for use with Diab Data D-CC. There is no need to reconstruct AMX in order to use it. The Tool Guide included with AMX for each supported tool set directs you in the proper use of the compiler, assembler, librarian and linker. Although rebuilding AMX is not required, instructions for doing so are included.

AMX is offered with a liberal site license agreement which does not limit the number of development work stations. Executable application modules incorporating AMX can be distributed without royalties.

AMX documentation is well organized, comprehensive and includes tutorial explanations and examples. The Reference Manual highlights the answers to the more common technical support questions.

It is KADAK's policy to provide prompt and courteous technical support to licensed AMX users. Each AMX product purchased includes automatic software updates for a period of one year from the date of purchase.

Features

- Full-featured, compact ROMable kernel with optimized execution speed.

- Preemptive, priority based task scheduler with optional time slicing.
- Nested interrupts with automatic vectoring.
- Mailbox, semaphore, resource, event, list, buffer and memory managers.
- Configuration Builder utility eases system construction.
- *KwikLook*[™] exploits the SDS SingleStep[™] task aware debugger to provide quick access to the state of your AMX application.
- AMX/FS[™] DOS compatible file system.
- TCP/IP support is available.
- Clear and comprehensive documentation.
- Site licenses include no-hidden-charges.
- No royalties.
- Source code included.
- Envable track record for reliability and support.

Availability

- Available now.

Ordering Information

- AMX PPC32: PN382-1
- AMX/FS PPC32: PN388-1
- *KwikLook* PPC32: PN390-2

Contact

KADAK Products Ltd.

206-1847 West Broadway Avenue
Vancouver, BC V6J 1Y5
CANADA
Tel: (604) 734-2796
Fax: (604) 734-8114
Email: amxsales@kadak.com

Australia

Baltec Systems Pty. Ltd.
26 Mayneview Street
Milton, Queensland
Australia 4064
Tel: (61) 7 33695900
Fax: (61) 7 33695257

France

OMNITEL
31, rue Jean Rostand
Orsay Cedex, France
91893
Tel: (33) 1 69855044
Fax: (33) 1 69855426

United Kingdom

Great Western Group Ltd.
Redwood House, Bristol Road
Keynsham, Bristol
England UK BS18 2BB
Tel: (44) 117 9860400
Fax: (44) 117 9860401

LynxOS®

Operating System, Real-Time Tool

Lynx Real-Time Systems

LynxOS is a UNIX-compatible, POSIX-conforming operating system designed for embedded real-time applications that require fast, deterministic response even in the presence of many asynchronous interrupts or data streams. Applications include video servers, communications packet-switch routing and control, networked office equipment, process supervisory control, workcell control, electronic test instrumentation control, and medical instrumentation.

The LynxOS kernel was designed to meet hard real-time requirements, such as short interrupt and preemption latencies, deterministic worst-case task response, and fast context switching, scheduling and interprocess communications. The kernel is modular, compact, and ROMable, allowing developers to target embedded applications.

AT&T System V and 4.3 BSD system-call interfaces and libraries provide compatibility with UNIX. Code written for UNIX can be easily ported to LynxOS and vice versa. LynxOS has been certified by the National Institute of Standards and Technology (NIST) to have passed the POSIX Conformance Test Suite which demonstrates conformance to FIPS PUB 151-1 and POSIX 1003.1 (certification performed using LynxOS version 2.2 for 386/486/Pentium). In addition, Lynx has implemented the real-time and threads extensions to POSIX. Lynx has implemented the POSIX.1b real-time extensions and draft 4 of the POSIX.1c threads extensions.

By fully exploiting the PowerPC microprocessor's memory management unit (MMU), LynxOS is a true multi-process operating system. Each process, which may consist of multiple threads of execution, is given its own

separate, protected memory space. Programming and debugging complex applications is far easier, application portability to different computer architectures is straightforward, and system reliability is greatly improved over single address space operating systems.

LynxOS for PowerPC microprocessor is available as a Porting Kit and as Source Code. The Porting Kit, targeted at developers of custom embedded designs, consists of:

- 10-user cross development.
- Environment hosted on IBM's AIX operating system version 3.2.5 or later.
- LynxOS operating system.
- Licenses for two target systems,
- Porting verification test suites.
- Documentation.
- Customer training classes for two.

Although the porting kit consists primarily of object-code files, it also includes source code for hardware-dependent operating system files required by developers to port LynxOS to any custom design based on the supported microprocessors.

LynxOS has been ported to the leading open system computer microprocessors, including the 386, 486, Pentium, Pentium Pro, MC68040, MC68060, SPARC 2, MicroSPARC, and R3000 processors. Reference Platform support packages are available to support popular computer platforms based on these microprocessors.

Real-Time Operating Systems

Features

- *Fully Preemptible, Compact Kernel*
 - Ensures that any higher priority task will preempt a lower priority one.
 - Kernel can be ROMed.
- *Processes and Threads*
 - Multiple memory-protected processes.
 - POSIX.1c support for execution of multiple threads within a process.
 - Processes and threads, including kernel threads, can be assigned priorities (up to 256 levels).
- *Input/output and File System*
 - Unified UNIX-like I/O—open, close, read, write, ioctl.
 - Dynamically loadable and re-entrant device drivers.
 - UNIX-like hierarchical file system.
 - Demand-paged virtual memory.
- *Other Real-Time Support*
 - Synchronous and asynchronous I/O.
 - Semaphores, mutexes, condition variables, pipes, events, queued reliable signals, message passing for intertask communications.
 - Clocks and timers.
 - Shared memory, memory locking, contiguous files, and priority inheritance.
- *Networking*
 - TCP/IP—telnet, rlogin, rsh, ftp, rcp.
 - NFS server and client.
 - STREAMS System V.3.

Reference Platforms

- IBM PowerPC Reference Platform, Reference Implementation motherboard.
- Motorola MVME1603 and 1604 motherboards.
- Motorola Ultra and Atlas motherboards.
- Force CPU603RT and CPU604RT.
- CES RTPC and CES RIO2.

Ordering Information

- LynxOS Native Development System for PowerPC microprocessors.
- LynxOS Cross-Development System for PowerPC microprocessors.
- LynxOS for PowerPC microprocessors Porting Kit.
- LynxOS for PowerPC microprocessors Source Code.

Processors Supported

- PowerPC 601 microprocessor.
- PowerPC 603 microprocessor.
- PowerPC 604 microprocessor.

Availability

- LynxOS for PowerPC microprocessors is currently available in native and cross-development versions.

Lynx Headquarters

2239 Samaritan Drive
San Jose, CA 95124
Tel: (408) 879-3900
Fax: (408) 879-3920
Web: <http://www.lynx.com>

Contact

Lynx Europe

2 Allée de la Fresnerie
78330 Fontenay Le Fleury
France
Tel: 331-3085-0600
Fax: 331-3085-0606

smxPPC™

Operating System, Libraries, Real-Time Tool

Micro Digital Inc.

smx® has been in use for over seven years in hundreds of applications. It is now available for PowerPC microprocessors as *smxPPC*.

smxPPC is a real-time multitasking kernel for use in embedded systems. It is specifically designed for demanding, real-time applications. *smxPPC* offers a full suite of kernel services, yet emphasizes simplicity and ease of use. It is reliable, robust, and highly capable.

Features

- *Task Management*—Full task control including create, delete, start, stop, resume, suspend, lock, and more.
- *Memory Management*—Heap and dynamically allocated regions. Block pools, message pools, and fast block pools.
- *Timing and Timers*—Real-time and elapsed-time clocks. Wakeups, timeouts, and precision delays. Cyclic and one-shot timers.
- *Input and Output*—Pipes and buckets for character I/O and macros for interrupt management.
- *Intertask Communication*—Message exchanges, semaphores, and pipes. Message pools. Dynamic messages.
- *Event Management*—Count events and monitor combinations of flags.
- *Scheduler*—Fully preemptive. Timeslicing and round-robin also supported.
- ROMable.
- *Link Service Routines (lsr's)*—Operate like foreground tasks for high performance.
- *Extensive Error Checking*—Over 70 types. Speeds debugging.
- *Numerous Support Products*—These include *smxFile*, *smxNet*, *smx++*, *smxProbe*, and others.
- *Miscellaneous*—Initialization, error recovery, and special functions.

smxPPC Development Kit Contents

- Pre-made EABI-compliant ELF/DWARF *smxPPC* libraries.
- Source-code platform for easy start.
- *User's Guide*, *Reference Manual*, and *smxPPC Manual*.
- Site development license.
- Royalty-free license for one developed product.

Supported Tools

- Diab Data C/C++ compiler.
- MetaWare High C/C++ compiler.
- SDS SingleStep Simulator/Debugger with point and click *smx* awareness.
- SDS SingleStep Target Monitor.

System Requirements

- DOS 5.0 or later.
- Windows 3.1, Windows 95, or Windows NT.

Processors Supported

- PowerPC 400 family.
- PowerPC 600 family.

Availability

- Available now.

Ordering Information

- *smxPPC* development kit.
- *smxPPC* source code.

Contact

Micro Digital Inc.
12842 Valley View St. #208
Garden Grove, CA 92645
Tel: (800) 366-2491
Fax: (714) 891-2363
Email: mdi@earthlink.net
BBS: (714) 893-5118
Web: <http://www.earthlink.net/~mdi>

Europe
PSOFT
49 Rue La Martine
Versailles, Cedex
France 78035
Tel: 33 1 30 62 1125
Fax: 33 1 30 69 9981

Japan
A-Z
3-16-11 Koshienguchi
Nishinomiya, Hyogo 663
Japan
Tel: 81 7 98 64 0005
Fax: 81 7 98 67 1600

VRTX/OS

Operating System, Real-Time Tool, Libraries

Microtec

The VRTX/OS real-time operating system is a modular RTOS that can be configured to meet the needs of a wide range of embedded applications. VRTXsa features responsive, state-of-the-art design reflecting the latest advances in operating system technology. Preemptibility and priority inheritance contribute to the predictability and safety of embedded software designs based on VRTXsa. Additionally, VRTXsa has been carefully designed to prevent priority inversion. Priority inversion occurs when a high-priority task is blocked, pending some action by a low priority task, leading to unpredictable system behavior.

VRTXsa can be used with SNX, which provides a rich set of high-performance TCP/IP networking facilities for applications based on VRTXsa. SNX brings the openness and modularity of STREAMS-based networking to the embedded real-time arena and combines standardization with high throughput.

VRTXsa is used with Spectra[®], a leading client-server cross-development environment. Spectra comprehends the full suite of C and C++ development tools including the XRAY Debugger.

Features

- Scalable preemptible RTOS architecture.
- The full-featured VRTXsa kernel is 100% compatible with VRTX and VRTX32 continuing a 12-year tradition of upward compatibility.
- VRTXsa is Preemptable and priority-inversion-free for responsiveness and reliability.
- VRTXsa features fast deterministic operations and is entirely suitable for use in deeply embedded systems.
- VRTX/OS includes powerful STREAMS-based networking including SNMPV2, TCP/IP, RPC/XDR, and NFS support.
- IFX supports real-time device-independent I/O and features hierarchical file management, disk caching, optional DOS media compatibility and byte stream management.
- ANSI RTL and DOS file system also available.

Hosts Supported

- Sun workstations.
- HP9000-700 workstations.

Real-Time Operating Systems

Software Requirements

- Requires the Spectra cross-development environment for configuration and development support.

Availability

- Available now.

Contact

Microtec

2350 Mission College Blvd
Santa Clara, CA 95054
Tel: (408) 980-1300
Toll Free: (800) 950-5554
Fax: (408) 982-8266
Web: <http://www.mri.com>

Domestic Offices

Nashua, New Hampshire
Tel: (800) 933-3036
Fax: (603) 891-3193

Maryland

Tel: (301) 921-1990
Fax: (301) 921-1994

New York

Tel: (516) 244-1497
Fax: (516) 563-1225

Connecticut

Tel: (860) 648-0681
Fax: (860) 648-1143

Dallas

Mentor/Microtec
Tel: (214) 450-2300
Fax: (214) 991-0706

Chicago

Mentor/Microtec
Tel: (847) 605-0230
Fax: (847) 605-8535

Orlando

Phone: (407) 240-1130
Fax: (407) 240-4840

Winter Park

Tel: (407) 677-9661
Fax: (407) 677-1972

Irvine

Mentor/Microtec
Tel: (714) 453-2500
Fax: (714) 453-2520

San Diego

Mentor/Microtec
Tel: (619) 597-1530
Fax: (619) 554-0023

San Jose

Mentor/Microtec
Tel: (408) 436-1500
Fax: (408) 451-5680

International Offices

Microtec Ltd.-England
Tel: +44.1256 707784
Fax: +44.1256 707786

Microtec GmbH- Germany

Tel: (49) 089 609 00 81
Fax: (49) 089 609 96 59

Microtec S.A.-France

Tel: (33) 1-30-12-02-10
Fax: (33) 1-30-12-02-20

Microtec AB-Sweden

Tel: +46-8-744 53 00
Fax: +46-8-645 53 36

Microtec-Italy

Tel: 39-2-33-21-71
Fax: 39-2-39-00-25-00

Microtec-Israel

Tel: 972-9-552636
Fax: 972-9-552627

Nihon Microtec, K.K.- Japan

Tel: (81) 3-5210-3050
Fax: (81) 3-5210-3180

Nihon Microtec, Kansai Japan

Tel: (81) 6-359-1620
Fax: (81) 6-359-1625

Hankuk Microtec-Korea

Tel: (82) 2-517-0838
Fax: (82) 2-517-0839

China Microtec- Beijing

Tel: (86) 10-6202-2744
Fax: (86) 10-62020135

Microtec-Taiwan

Tel: 886-2-7576020-5
Fax: 886-2-7576027

Microtec- Australia/New Zealand

Tel: 61-2-413-4600
Fax: 61-2-413-4622

OS-9®

Compiler, Debugger, Real-Time Tool, Operating System, Utilities

Microware Systems Corporation

The OS-9 operating system is a collection of system modules that includes a high-speed kernel, robust I/O manager, dedicated file managers, and interrupt-driven device drivers. All modules are independent and dynamic in the OS-9 system, allowing immense flexibility and easy configuration. This architecture promotes structured programming techniques to make system integration quick and manageable. The broad spectrum of OS-9 I/O modules assures support for virtually all classes of I/O devices used in consumer, industrial and scientific environments.

The compact size and scalable architecture of OS-9 make it the ideal choice for embedded PowerPC designs by providing plug-and-play solutions for the complete range of systems, from high performance industrial systems to small embedded electronic products. Its microkernel core and host of independent I/O file managers support a broad spectrum of industrial applications including process control, telecommunications, medical instrumentation and intelligent consumer electronics.

Microware also supports the PowerPC microprocessors with its OS-9 Development Package for resident development and FasTrak, an integrated development toolset for Windows and UNIX cross-development. The OS-9 Development Package is a complete drop-in package that includes:

- OS-9 kernel.
- I/O manager and file manager for OS-9 disks and PC-DOS disks and tapes.
- Console, serial and parallel devices, and pipes.
- Ultra C or Ultra C++ compiler.
- Source-level debugger.
- Symbolic debugger.
- Screen editor.
- Complete documentation.
- 90-day hotline support.

The Ultra C or Ultra C++ advanced technology compiler is an integral part of Microware's FasTrak cross-development product. FasTrak can be hosted on UNIX workstations and Windows-based PCs targeting OS-9 embedded designs. FasTrak is a real-time development tool which concentrates on the implementation phases of real-time software design. A fully integrated package, FasTrak consists of a workbench, automatic makefile generator, multitask source and assembly debugging, code animation, target application and system profiling, and performance monitoring.

Real-Time Operating Systems

Features

- Real-time operating system for embedded PowerPC systems.
 - Priority-based, preemptive task scheduler.
 - Complete interrupt, exception, resource and task management facilities.
 - Interprocess communication facilities: signals, events, pipes, alarms, sockets and data modules.
 - I/O extension and driver support
 - Serial, parallel, industrial analog and digital I/O support.
 - SCSI, PC-DOS disk and tape support.
- ISDN, T1/E1, TCP/IP, Ethernet, NFS, SLIP networking.
 - MPEG audio and video.
 - *FasTrak development options*
 - UNIX.
 - DOS/Windows.
 - Ultra C and Ultra C++ compilers target embedded PowerPC microprocessors.

Availability

- Available now.

Contact

United States

Microware Systems Corporation
Corporate Headquarters
1900 N.W. 114th Street
Des Moines, IA 50325-7077
Tel: (515) 224-1929
Fax: (515) 224-1352
Email: info@micro-ware.com
Web: <http://www.micro-ware.com>

Western Regional Office
2055 Gateway Place,
Suite 400
San Jose, CA 95110
Tel: (408) 451-3999
Fax: (408) 451-3998

Northeastern Regional Office
One Crank Road
Hampton Falls, NH 03844
Tel: (603) 929-4107
Fax: (603) 929-4233

Southeastern Regional Office
2611 N.E 6th Street
Pompano Beach, FL 33062-4926
Tel: (305) 946-9280
Fax: (305) 946-9350

South Central Regional Office
Great Hills Corporate Center I
Suite 220
9020 Capital of Texas Highway North
Austin, TX 78759
Tel: (512) 794-0247
Fax: (512) 794-0251

United Kingdom

Microware Systems (U.K.) Limited
Beech Court
27/33 Summers Rd
Burnham SL1 7EP
United Kingdom
Tel: (44) 1628 667578
Fax: (44) 1628 667579

France

Microware Systems France
Chateau de la Saurine
Pont de Bayeux
13590 Meyreuil, France
Tel: (33) 42.58.63.00
Fax: (33) 42.58.62.28

Japan

Microware Systems K.K.
17-3, Sotokanda 2-Chome
Chiyoda - Ku
Tokyo 101, Japan
Tel: (81) 3-3257-9000
Fax: (81) 3-3257-9200

Germany

Dr. Rudolf Keil, GmbH
Gerhart-Hauptmann-Str.30
D-69221 Dossenheim
Germany
Tel: (49) 6221-862091
Fax: (49) 6221-861954

Switzerland

Elsoft AG
Tafernstr. 20
5405 Baden - Dattwil
Switzerland
Tel: (41) 56-83-3377
Fax: (41) 56-83-3020

Australia

Microprocessor Consultants Pty. Ltd.
23 Norma Road
Palm Beach 2108
NSW Australia
Tel: (61) 2-974-4917
Fax: (61) 2-974-4900

PowerTV™

Multimedia Tool, Operating System, Real-Time Tool, Utilities

PowerTV, Inc.

The PowerTV multitasking operating system takes a new approach. Its design reflects a single purpose: to support real-time, media-rich applications delivered across interactive TV networks. The PowerTV OS is an open platform. It offers the state-of-the-art in multimedia processing in a compact and highly efficient format. Its modular architecture provides cross-platform portability, application flexibility, high-performance playback, and dynamic scalability while keeping memory costs to a minimum.

Cross-Platform Portability

The PowerTV OS achieves true platform independence by defining a rich set of access and control interfaces to underlying media hardware:

- Content developers can create applications that run transparently on a wide range of platforms.
- Network providers can protect their investment in content as hardware platforms evolve to higher levels of functionality.
- Set-top box manufacturers can easily adapt the OS to different hardware configurations to address multiple market segments cost effectively. All digital home communications terminals manufactured by Scientific-Atlanta will incorporate the PowerTV operating system.

Flexible Application Support

PowerTV's standards-based multimedia and network facilities fulfill the runtime needs of existing and emerging applications. In the near term, while broadcast services dominate the market, the PowerTV OS enables two new classes of applications:

- Near video-on-demand, allowing subscribers to choose movies broadcast at preset times.
- Information services, letting subscribers select newspaper articles, weather information, sports events, and other text-based media from menu-driven data archives.

Home shopping, video-on-demand, networked games, and financial trading are among the many applications that can achieve their full potential using native PowerTV communications, media processing, session management, and user interface features.

High-Performance Playback

PowerTV delivers entertainment-quality audio and video at consumer price levels for three separate classes of content developers:

- For video game developers wanting both application speed and cross-platform portability, PowerTV provides low-level software control of media processing hardware.
- Authors using high-end tools can take advantage of PowerTV's native playback engines for authoring environments including Oracle Media Objects™ and Media Net™, Sybase Gain Momentum™ and Inter-Play™, and Scala Backbone™.
- Custom applications can write directly to the operating system for best performance.

Dynamic Scalability

PowerTV's modular, scalable architecture can be tailored for different application and market needs. Modules can be downloaded on the network as a batch system upgrade, by individual applications at run time, or on demand.

PowerKernel™

- Fully preemptive, multithreaded kernel.
- Optimized for RISC processors.
- Unified event system.
- Real-time event processing.
- Low memory footprint.
- Dynamic loader.

Graphics Subsystem

- Optimized graphic performance.
- RGB and CLUT support.
- Automatic color format conversion.
- Automatic scaling.
- Translucent alpha-blending.
- Chroma keying.
- Live video capture.

PowerDraw™ 2D Imaging System

- Comprehensive drawing primitives.
- Complete rendering facilities.
- Anti-aliased lines.
- Clipping and other visual effects.
- Built-in font engine.
- Adobe NFNT font support.
- Anti-alias text support.

Audio Subsystem

- Device-independent audio.
- AIFF sound file support.

Screen Manager

- Private or shared screen support.

- Application-controlled resolution.
- NTSC and PAL format.
- Transparent context switching.
- Graphic overlays.

TV Manager

- Logical channel tuning.
- Unified interface to analog and digital services.

MPEG Transport

- Connection-based model supporting decomposition of multiple streams from network servers, attached devices, and local RAM.
- Control at the transport stream, program, and PID level provided.
- System event generation supporting features such as presentation time stamps, network information table access, etc.
- MPEG volume control.

TCP/IP Socket Utility

- Berkeley Sockets API.
- TCP, UDP, and ICMP support.

PowerPC Microprocessors Supported

- PowerPC 603 microprocessor.
- PowerPC 403 microprocessor.

Availability

- Availability now.

Contact

PowerTV
20833 Stevens Creek Blvd
Suite 100
Cupertino, CA 95014

Tel: (408) 777-7573
Fax: (408) 777-0176
Email: info@powerTV.com
Web: <http://www.powerTV.com>

Precise Real-Time Executives

Operating System, Real-Time Tool, Utilities

Precise Software Technologies Inc.

The Precise Real-Time Executives are designed for real-time and embedded applications that range from single-processor PowerPC microcontrollers to distributed multiprocessor configurations. The executives are implemented in the C programming language and are delivered with royalty-free source-code licenses, extensive I/O support, and guaranteed portability across configurations.

Selecting one of the Precise Real-Time Executives for an initial design is both a smart short-term investment and a risk-free long-term strategic decision. In the short term, your purchase is easily amortized on any research and development project. In the long term, your application will port to new PowerPC hardware and can be easily reconfigured to run on a distributed or multiprocessor configuration.

The Precise Real-Time Executives are constructed using modular independent real-time executive components. The executives are delivered in pre-integrated default single-processor or multiprocessor configurations called *Precise/MQX* and *Precise/MQX⁺* respectively. A developer may reconfigure or extend the executives using any of the supplied components or by developing and adding proprietary components.

Features

- Royal-free license.
- PC-based execution supports rapid prototyping and testing.
- Component-based architecture.
- Scalable support for distributed or multiprocessor configurations.
- Complete set of real-time executive features.
- Reliable operation with error handling and run-time checking.
- Multi-threaded micro-kernel.
- Support for:
 - Multitasking
 - Message passing
 - Semaphores
 - Events
 - Mutexes
 - Queues
 - Memory management
 - Time delay
 - Interrupt
 - Formatted I/O
 - Profiling
 - Time-of-day
 - Routing
- Optional support for TCP/IP, PPP, RPCs, SNMP, SDLC, HDLC, LAPB, File System.
- Portable.
- 95% ANSI C source code.

Precise/MQX

Precise/MQX is a full-featured, general-purpose, single-processor real-time executive. The minimum configuration includes:

- Task management.
- Interrupt handling.
- Memory management.
- Time management.

Typical applications that have employed the Precise/MQX real-time executive include: avionics, vehicle electronics, medical instruments, process control, telephony, test and measurement, data communications, networking, automotive electronics, consumer products, dispatch systems, mobile radio, and conveyor systems.

Precise/MQX⁺

Precise/MQX⁺ is used specifically for applications that require more than one processor. It is an upward-compatible variant of Precise/MQX. The only functional difference is that Precise/MQX⁺ includes the *Routing Component* and either standard or a use-specified inter-processor communication drivers.

Typical applications that have employed Precise/MQX⁺ are data communications, signal processing, networking, medical electronics, avionics, simulation, air traffic control, and measurement.

Precise/MQX⁺ supports real-time multiprocessing and real-time distributed processing on any configuration of processors. The processors do not need to be fully connected. The most common multiprocessor configurations employ from two to eight processors.

Any application that uses Precise/MQX⁺ will require at least one type of Inter-Processor Communications (IPC) component to interconnect processors. The choice of IPC is very flexible, because Precise/MQX⁺ does not depend on the implementation of the IPC. Software developers may define their own IPCs or employ one or more IPCs supplied by Precise Software Technologies Inc. IPCs can be implemented with Embedded I/O Components or chip drivers.

Hosts Supported

- Windows 3.1, Windows 95, Windows NT.
- Sun workstations.

Targets Supported

- PowerPC 403 GA embedded controller.
- PowerPC 603 microprocessor.

Availability

- Available now.

Contact

Precise Software Technologies Inc.

1740 Massachusetts Avenue
Boxborough, MA 01719
Tel: (508) 264-4413
Tel: (800) 628-8631 sales
Fax: (508) 264-4819

Headquarters

Suite 308, 301 Moodie Drive
Nepean, ON, K2H 9C4
Tel: (613) 596-2251
Tel: (800) 265-9833 sales
Fax: (613) 596-6713
Email: info@psti.com
Web: <http://www.achilles.net/~psi>

RealTime Craft®

Operating System, Real-Time Tool

TECSI S.A.

RealTime Craft is a range of real-time executives and associated development tools. RealTime Craft executives run on most embedded microprocessors and controllers as well as on computers running MS-DOS or Windows.

Exceptional performances in terms of speed, compactness and certifiability make RealTime Craft a first choice for high-volume or quality-demanding applications.

RealTime Craft puts no constraint on the choice of the development system or of the host machine, but provides a full set of complementary tools to debug the multitasking

aspects of applications. Customers thus get a powerful, complete development environment with the most advanced capabilities.

TECSI is a long-term-oriented company, dedicated to quality of service. Delivery of a software package includes unlimited hot-line support during a one-year period. Additional training, consulting, or custom development are available.

RealTime Craft products are already used throughout the world by major industrial companies, in aerospace, automotive, defence, energy, factory automation, measurement, telecommunications, transportation, etc.



PHOTO #2
(location marker only—
do not use keyline)

Real-Time Operating Systems

Features

- Exceptional speed and compactness.
- Full set of executive modules around the kernel: TCP/IP, Memory, I/O, File Management and Object support, etc.
- Interfaces to popular development environments.
- Powerful complementary tools to debug multitasking aspects.
- Easy set-up.
- Real-time hot-line support.

PowerPC Processors Supported

- PowerPC 400 family of embedded controllers.

Availability

- Available Q2 97.

Contact

TECSI
Tour Aurore
18, place des Reflets
92975 Paris La Défense Cedex
France
Tel: +33-1-47 78 67 67
Fax: +33-1-47 78 67 68
Email: rtc@tecsi.com

International Headquarters will forward you to your local agent.

SuperTask!

Analyzer, Debugger, Operating System, Real-Time Tool

U S Software

The SuperTask! Operating System and Development Suite promotes a structured development cycle with three balanced components—all standard, no options to buy:

- *ViewTask!*—Design and development tool.
- *ProtoTask!*—Prototype and debugger tool.
- *MultiTask!*—U S Software's RTOS core and multitasking operating system.

ViewTask!

ViewTask! features the ability to analyze task set interactions. The generation of a 'C' code framework automatically assigns to each task optimized priorities. The ViewTask! tool allows you to immediately start prototyping and debugging with operational 'C' code.

ProtoTask!

ProtoTask! with ViewTask! prototypes and debugs your real-time multitasking applications. Use it on your development platform for stand-alone task level debugging or in concert with a source level debugger such as Microsoft Codeview or Borland Turbo Debugger. ProtoTask! facilitates over 29 task level debug operations for the PowerPC processor.

MultiTask!

MultiTask! is U S Software's open-architecture core suite. A high performance embedded multitasking operating system, including over seventy powerful system calls, but can be implemented within as little as an eight kilobyte footprint. Included is complete source code with ANSI C stream I/O including `sprintf` and `scanf`. With MultiTask! serial I/O operations are performed on your target processor using the standard ANSI C interface.

The MultiTasking! Core, ANSI C Standard (Methodology), is identical across all processors - a pure engineering design concept. No matter which target processor you choose, your code will behave identically with SuperTask!, an extremely valuable feature that insures maximum reuse of existing code and a shorter time-to-market.

Reliability and Performance

U S Software's test lab is dedicated to rigorous automated testing of SuperTask! products on all major compiler toolchains for the PowerPC environment and many software/hardware configurations.

U S Software benchmarks are not just a list of simple cycle counts, but real-world measured timing using situations and compiler toolchains. The effort we make assures an expectation level that is realistic for any operation that you can anticipate on the PowerPC platform.

Technical Support

Full telephone product support for the first year is included. A comprehensive manual documenting our multitasking suite -- ViewTask!, ProtoTask! and MultiTask!, as well as the complete operating system source also is included.

Real-Time Operating Systems

Training

Classes range from the conceptual to the specifics of generating code. We can provide the instruction at your location or ours. Flexible training schedules assist your specific project and resource needs. Our instructors are the very software engineers that have designed, tested and implemented our embedded products throughout the world.

Implementation Services

U S Software offers product implementation and customization services.

Availability

- Available now.

Contact

U S Software

14215 NW Science Park Drive
Portland, OR 97229
Tel: (800) 356-7097
Tel: (503) 641-8446
Fax: (503) 644-2413
Email: info@ussw.com
Web: <http://www.ussw.com>

Cross-Development Environments (Embedded)

CHORUS/ClassiX™

Debugger, Libraries, Operating System, Real-Time Tool, Utilities

Chorus Systems

CHORUS/ClassiX combines the CHORUS/Nucleus™ open microkernel standard with a UNIX-based remote development and debugging environment. CHORUS/ClassiX brings transparent access to UNIX in a scalable and flexible distributed execution environment. It can be used to build open, distributed, real-time applications for the telecommunications, internetworking and other embedded-systems markets.

Features

- CHORUS® open microkernel standard.
- High performance real-time executive.
- Fast, local and remote Transparent Connectivity services (Inter-Process Communication).
- Supports both privileged and protected processes.
- Dynamic evolution, and reconfiguration of processes, including dynamically loadable device drivers.
- Enabling technologies for building fault-tolerant services.
- Fully portable on all hardware platforms.
- Easily tailored to specific hardware and software configurations.
- TCP/IP, NFS, and many UNIX utilities.

Benefits

- Mature operating system technology and industry-proven robustness.
- Deterministic, real-time response to external events.
- Easy transparent programming of distributed or clustered systems.
- Can switch from development to deployment without compromising performance.

- Enables customization of hardware and software resources for optimized performance, reliability, and cost.
- Increased availability and guaranteed continuity of service for mission-critical applications.
- Hardware platform independence.
- Flexibility and scalability of system configuration.
- Transparent integration of real-time remote targets into UNIX environments.

System Specifications

- *Real-Time Executive*
 - Light-weight threads.
 - Preemptive priority-based scheduler.
 - 256 priority levels.
 - Multiple scheduling classes.
 - Synchronization by mutexes, semaphores, and mini-messages.
 - Execution control.
 - Timers.
 - Dynamic kernel resource management.
- *Hardware Supervisor*
 - Dynamic (de)installation of interrupt and trap handlers.
 - User-level handlers installable in system space.
 - Multiple priority-ordered handlers.
 - Dynamic resource allocation and management.
- *Distributed Virtual Memory*
 - Dynamic allocation/deallocation of memory.
 - Separate, protected address spaces.
 - Memory sharing between processes.

Cross-Development Environments (Embedded)

- *Transparent Connectivity*
 - Fast, location-transparent asynchronous and synchronous Remote Procedure Call (RPC).
 - Inter-Process Communication (IPC) services.
 - Local and remote communication.
 - Light-weight RPC optimization.
 - Small untyped messages for fastest processing by network interfaces.
 - Efficient low-overhead internal protocols.
 - Automatic localization of distributed objects for transparent remote access.
 - High-level network interface independent of specific network protocols.
 - Facilities for managing and broadcasting to groups of destinations.
 - At-most-once RPC semantics.
 - Thread abort propagated through RPC's.

c_actor Programming Interface

An extension to the CHORUS/Nucleus native programming interface:

- ANSI thread-safe C library (100 functions).
- Thread-safe C++ library (iostream).
- POSIX I/O interfaces (60 Calls).
- Transparent remote host access (BSD Sockets, TCP/IP, NFS).
- Transparent distributed execution control (spawn, kill, list).
- Debugging support (trace, wait, symbols).

Cross-Development Environment

- *Target Operating System Build*—CHORUS Allows production, modification, and dynamic configuration of target systems from a UNIX host.
- *Distributed Development Environment*—ANSI-C and C++ cross-development system. User and supervisor interfaces.
- *Multiple Targets Remote Control*—Network target boot (TFTP). Target configuration control (rsh), mount file systems, c_actor list and status.
- *Remote Symbolic Debugging*—CHORUS KDB: CHORUS/Nucleus structures, interrupt handlers debugging. CHORUS GDB: source level debugging, multi-threaded application. Both remotely activated from UNIX host.
- *Profiling*—Profiler for supervisor actors and for the CHORUS/Nucleus.

PowerPC Target Platforms

- PowerPC 603 and 604 microprocessors.

Availability

- Available now.

Contact

North America

Chorus Systems
1999 South Bascom Ave, Suite 400
Campbell, CA-95008
Tel: (800) 97-CHORUS toll free
Tel: (408) 879-4100
Fax: (408) 879-4102
Email: info@chorus.com
Web: <http://www.chorus.com/>

Europe

Chorus Systems
6, avenue Gustave Eiffel
78182, Saint-Quentin-en-Yvelines
FRANCE
Tel: +33 (1) 30 64 82 00
Fax: +33 (1) 30 57 00 66
Email: info@chorus.fr

Asia/Pacific

Chorus Systems
Mitsutake Building Ikejiri, 8F
Ikejiri 3-22-4
Setagaya Ku, Tokyo 154
JAPAN
Tel: +81 (3) 5430-1131
Fax: +81 (3) 5430-1133
Email: info-ap@chorus.com

MULTI[®] Development Environment

User Interface, Utilities

Green Hills Software, Inc.

The MULTI development environment for PowerPC[™] microprocessors provides a framework of interacting tools to support program development by small or large workgroups. MULTI includes all of the tools you need to support a major programming project.

MULTI supports program development in Ada, C, C++, Fortran, Pascal and assembly language. Source code from these languages can be mixed together in almost any combination to create a single executable. MULTI supports both embedded and native development, so programmers who do both only need to deal with a single set of tools.

The program builder provides an advanced means of controlling compilation that is easier to use than *make*, provides more project control and works identically on all systems. Configure your program by simply listing your files. All dependencies are resolved automatically. The builder communicates with the compilers to allow automatic compilation across source modules and across languages.

The hierarchical configuration management system provides a methodology for managing program organization. Nested subprojects can be used to coordinate between groups working on the same large project or to manage code which may be shared between different projects. Program options can be set at any level and propagate downward through the hierarchy unless overridden at a lower level.

The integrated version control system automatically checks files in and out as you edit them. Named checkpoints can be created at any time so that you can later retrieve the source code corresponding to intermediate program versions. Portions of your program can be split off into separate branches for development when major changes are required, then automatically merged back into the mainline program when the changes are finished.

The powerful editor is designed specially to run under a window manager and is fully configurable to meet your personal style.

Cross-Development Environments (Embedded)

Host System Requirements

- Most UNIX workstations including Sun, HP, DEC, RS/6000, SGI, Data General, MIPS, 386/SCO, 386/Univel.
- PC running Windows.

Availability

- Available now.

Contact

North America

Green Hills Software, Inc.
510 Castillo Street
Santa Barbara, CA 93101
Tel: (805) 965-6044
Fax: (805) 965-6343

Germany

XCC Software Sales
Tel: 49.721.616474
Fax: 49.721.621384

Belgium

RTUSI
Tel: 32.2.523.24.62
Fax: 32.2.520.83.09

Italy

ETNOTEAM
Tel: 39.2.26162.1
Fax: 39.2.2611075.5

United Kingdom

Real Time Products
Tel: 44.121.333.6955
Fax: 44.21.333.5433

Japan

Advanced Data Controls
Tel: 81.3.3576.5351
Fax: 81.3.3576.1772

Spain

Marben Software
Tel: 34.1.377.09.28
Fax: 34.1.377.19.93

France

SCT Electronique
Tel: 33.61.61.12.34
Fax: 33.61.61.12.22

Sweden

Avent Computer AB
Tel: 46.893.0550
Fax: 46.894.9083

SPECTRA®

Debugger, Operating System, Real-Time Tool, Utilities

Microtec

Spectra is a new generation cross-development environment that features a flexible and open software backplane. Spectra facilitates company-wide standardization by addressing the full range of embedded applications from austere, minimal-resource systems up to complex, resource intensive environments.

Using any hardware connection, Spectra's unique client-server architecture allows a developer to use any tool to develop and debug software on a target connected to the Spectra server. Spectra then services the requests/commands of each tool and manages the target designated by the tool, regardless of where the target is located and whether it is on or off the network.

Spectra's unique open design allows users to integrate user-defined and third-party tool suites and run-time environments preserving code and tool investments. Further, a fully integrated, host-based tool set is available for constrained targets radically reducing target memory consumption.

Spectra includes the KernelBuilder™ and KernelIntegrator™ tool kits. KernelIntegrator allows users to integrate proprietary in-house code with Spectra. KernelBuilder allows developers to build new kernels, emulate existing in-house kernels or customize the VRTXsa kernel.

Spectra provides several run-time options that are built around the Nanokernel™ architecture, enabling the development of kernels scaled to specific application needs

and industry-standard programmer interfaces. The first Spectra-compliant kernel, VRTXsa™, is the core of the latest VRTX/OS.

Features

- Spectra is a truly open cross-development backplane.
- Client-server architecture offers connectivity to a wide range of links including serial, Ethernet, terminal multiplexers, and customized links.
- Spectra provides the PowerPC architecture with a host target connection that is independent of the run-time system and multiple open interfaces for easy integration of tools and run-times.
- Spectra is an excellent software platform for company-wide standardization. Standardization sharply reduces training, maintenance and upgrade costs, while promoting code reusability.
- Spectra features VRTXsa, an advanced upward-compatible, scalable kernel that permits reuse of code across diverse applications.

Cross-Development Environments (Embedded)

Hosts Supported

- Sun workstations.
- HP9000-700 workstations.

Availability

- Available now.

Contact

Microtec

2350 Mission College Blvd
Santa Clara, CA 95054
Tel: (408) 980-1300
Toll Free: (800) 950-5554
Fax: (408) 982-8266
Web: <http://www.mri.com>

Domestic Offices

Nashua, New Hampshire
Tel: (800) 933-3036
Fax: (603) 891-3193

Maryland

Tel: (301) 921-1990
Fax: (301) 921-1994

New York

Tel: (516) 244-1497
Fax: (516) 563-1225

Connecticut

Tel: (860) 648-0681
Fax: (860) 648-1143

Dallas

Mentor/Microtec
Tel: (214) 450-2300
Fax: (214) 991-0706

Chicago

Mentor/Microtec
Tel: (847) 605-0230
Fax: (847) 605-8535

Orlando

Phone: (407) 240-1130
Fax: (407) 240-4840

Winter Park

Tel: (407) 677-9661
Fax: (407) 677-1972

Irvine

Mentor/Microtec
Tel: (714) 453-2500
Fax: (714) 453-2520

San Diego

Mentor/Microtec
Tel: (619) 597-1530
Fax: (619) 554-0023

San Jose

Mentor/Microtec
Tel: (408) 436-1500
Fax: (408) 451-5680

International Offices

Microtec Ltd.-England
Tel: +44.1256 707784
Fax: +44.1256 707786

Microtec GmbH- Germany

Tel: (49) 089 609 00 81
Fax: (49) 089 609 96 59

Microtec S.A.-France

Tel: (33) 1-30-12-02-10
Fax: (33) 1-30-12-02-20

Microtec AB-Sweden

Tel: +46-8-744 53 00
Fax: +46-8-645 53 36

Microtec-Italy

Tel: 39-2-33-21-71
Fax: 39-2-39-00-25-00

Microtec-Israel

Tel: 972-9-552636
Fax: 972-9-552627

Nihon Microtec, K.K.- Japan

Tel: (81) 3-5210-3050
Fax: (81) 3-5210-3180

Nihon Microtec, Kansai Japan

Tel: (81) 6-359-1620
Fax: (81) 6-359-1625

Hankuk Microtec-Korea

Tel: (82) 2-517-0838
Fax: (82) 2-517-0839

China Microtec- Beijing

Tel: (86) 10-6202-2744
Fax: (86) 10-62020135

Microtec-Taiwan

Tel: 886-2-7576020-5
Fax: 886-2-7576027

Microtec- Australia/New Zealand

Tel: 61-2-413-4600
Fax: 61-2-413-4622

XRAY MasterWorks®

Compiler, Debugger, Utilities

Microtec

The XRAY MasterWorks integrated development environment provides point-and-click access to a variety of tightly integrated embedded systems tools to speed up the edit-compile-debug cycle. XRAY MasterWorks gives you the benefits of automated program building, program analysis and debugging, and rapid response to code changes throughout the development phase. The tight integration of tools enables a rapid edit-compile-debug process leading to higher productivity.

XRAY MasterWorks works with the complementary Spectra backplane. Spectra is the first application of a client-server architecture to real-time embedded software development and provides highly efficient host-target connectivity for a wide range of applications.

Included in XRAY MasterWorks are the XRAY MasterWorks productivity tools, XRAY Debugger, and the C and C++ cross compiler package. XRAY MasterWorks Productivity Tools consist of a graphical source code manager and a graphical make tool that can generate and update makefiles.

Features

- *XRAY MasterWorks*
 - Easy to use X Windows GUI.
 - Speeds up edit-compile-debug cycle.
 - Manages work environment from a central location for improved quality.
- *XRAY Master*
 - Automatic makefile generation and build capabilities.
 - Graphical source-code management interface to SCCS and RCS, customizable for other file management systems.

- Control panel for managing work sessions and tools.

- *XRAY Debugger*

- Source-level debugging of optimized code.
 - ANSI, C, C++, and assembly language debugging.
 - Window-oriented user interface.
 - D expression evaluator including interactive execution of the target function.
 - Simple and complex breakpoints (access, read, write, and instruction).
 - Simulated I/O and interrupts.
 - Single-step execution, including statement-stepping across complex expressions, loops, and multiple statements per line.
 - User-definable windows.
- *C/C++ Compiler*
 - Supports ANSI C/C++ with extension for embedded systems.
 - Produces symbolic information for debugging of optimized code.
 - C++ template support.
 - EABI compliant.

XRAY Debugger

The XRAY Debugger operates on C++, ANSI C, or assembly application code letting you completely control and monitor the flow of program execution. The XRAY Debugger displays multiple windows simultaneously for quick analysis of different views of the target system. The ability to debug optimized code at source level is unique to XRAY.

A powerful command language provides simple and complex breakpoint setting, single-stepping, code patching, and continuous variable monitoring. The XRAY Debugger also

Cross-Development Environments (Embedded)

provides you with a powerful high-level macro language. Macros consisting of ANSI C and C++ statements, expression, and debugger commands can be composed either within the XRAY Debugger environment, the XRAY MasterWorks environment, or externally using your favorite text editor.

Compilers

The ANSI C/C++ cross-compiler assists in the development of efficient, portable, and easy to maintain programs for microprocessor-based systems. The compiler generates assembly language code that is further processed by

Microtec's assembler and linker. It also produces debugging information for use with the XRAY Debugger. The compiler supports multiple code and global data models. It also provides extensive diagnostic and warning messages at compile time for superior code checking.

Hosts Supported

- Sun SPARCstations.
- HP9000-700 workstations.

Availability

- Available now.

Contact

Microtec

2350 Mission College Blvd
Santa Clara, CA 95054
Tel: (408) 980-1300
Toll Free: (800) 950-5554
Fax: (408) 982-8266
Web: <http://www.mri.com>

Domestic Offices

Nashua, New Hampshire
Tel: (800) 933-3036
Fax: (603) 891-3193

Maryland

Tel: (301) 921-1990
Fax: (301) 921-1994

New York

Tel: (516) 244-1497
Fax: (516) 563-1225

Connecticut

Tel: (860) 648-0681
Fax: (860) 648-1143

Dallas

Mentor/Microtec
Tel: (214) 450-2300
Fax: (214) 991-0706

Chicago

Mentor/Microtec
Tel: (847) 605-0230
Fax: (847) 605-8535

Orlando

Phone: (407) 240-1130
Fax: (407) 240-4840

Winter Park

Tel: (407) 677-9661
Fax: (407) 677-1972

Irvine

Mentor/Microtec
Tel: (714) 453-2500
Fax: (714) 453-2520

San Diego

Mentor/Microtec
Tel: (619) 597-1530
Fax: (619) 554-0023

San Jose

Mentor/Microtec
Tel: (408) 436-1500
Fax: (408) 451-5680

International Offices

Microtec Ltd.-England
Tel: +44.1256 707784
Fax: +44.1256 707786

Microtec GmbH- Germany

Tel: (49) 089 609 00 81
Fax: (49) 089 609 96 59

Microtec S.A.-France

Tel: (33) 1-30-12-02-10
Fax: (33) 1-30-12-02-20

Microtec AB-Sweden

Tel: +46-8-744 53 00
Fax: +46-8-645 53 36

Microtec-Italy

Tel: 39-2-33-21-71
Fax: 39-2-39-00-25-00

Microtec-Israel

Tel: 972-9-552636
Fax: 972-9-552627

Nihon Microtec, K.K.- Japan

Tel: (81) 3-5210-3050
Fax: (81) 3-5210-3180

Nihon Microtec, Kansai Japan

Tel: (81) 6-359-1620
Fax: (81) 6-359-1625

Hankuk Microtec-Korea

Tel: (82) 2-517-0838
Fax: (82) 2-517-0839

China Microtec- Beijing

Tel: (86) 10-6202-2744
Fax: (86) 10-62020135

Microtec-Taiwan

Tel: 886-2-7576020-5
Fax: 886-2-7576027

Microtec- Australia/New Zealand

Tel: 61-2-413-4600
Fax: 61-2-413-4622

FasTrak

Compiler, Debugger, Real-Time Tool, Utilities

Microwave Systems Corporation

Microwave's FasTrak is a comprehensive software programming and management environment designed to increase the efficiency of OS-9® real-time system development.

FasTrak's highly integrated toolset simplifies and automates the task of creating, debugging, analyzing and managing complex real-time software development projects.

FasTrak is much more than just an edit-compile-debug package. FasTrak's expanded functionality addresses all phases of product development, from initial code creation to software version control. This focus on the entire product life cycle means reduced time-to-market and improved project management.

FasTrak's host toolkit is logically divided into five functional modules:

- Workbench.
- Text Editor.
- Makefile Editor.
- FastFix Debugger.
- Target System Tool.

The Workbench is the primary interface to FasTrak where you can automatically build, execute and debug your application at the touch of a button. By providing a graphical front-end to your favorite text editor, the FasTrak Text Editor allows quick transition and quicker source-code correction with its auto repair function. FasTrak's Makefile Editor automates the tedious process of creating and maintaining program makefiles. Just point and click to specify the tools, options, procedures and I/O files needed to build your programs. The Debugger accelerates the software testing process with its push-button features, wide range of displays, multiple tasking, and multiple

targeting. FasTrak's tight integration with OS-9 makes it possible to provide application and system performance information that is not possible with other cross development packages. The Target System Tool monitors the performance of application modules as well as CPU and network utilization.

Ultra C and Ultra C++ Compilers

FasTrak contains a copy of Microwave's Ultra C or Ultra C++ compiler, the only highly-optimizing C and C++ compilers designed expressly for real-time applications by an RTOS vendor.

Ultra C and Ultra C++ are advanced-technology C and C++ compilers that perform inter-procedural, global and local optimizations to maximize performance for embedded applications. They produce compact, ROMable, position-independent code compatible with the OS-9 object module format.

Ultra C complies fully with ANSI X3J11 1989 and ISO/IEC 9899:1990 specifications for the C programming language and is the only C real-time compiler that has passed the Plum Hall ANSI C/ISO Validation Suite v6.0.

Ultra C++ is tracking ANSI X3J16 draft.

Features

- Software productivity multiplier targeting OS-9.
- Addresses all phases of the project development cycle.
- Automatically generates makefiles.
- Automated edit, build and repair facilities.
- Workbench files store working parameters for individual projects.
- X Windows System graphical user interface.

Cross-Development Environments (Embedded)

- TCP/IP Ethernet and serial (SLIP) communications.
- On-line help.
- Ultra C and Ultra C++ advanced-technology compilers.
- Hosted on both Windows and UNIX-based systems.

System Requirements

- UNIX workstations, including Sun 4, IBM RS/6000, SGI, and HP 9000 Series 700.
- Windows 3.x, Windows 95, Windows NT, Windows for Workgroups.

Availability

- Available now.

Contact

United States

Microware Systems Corporation
Corporate Headquarters
1900 N.W. 114th Street
Des Moines, IA 50325-7077
Tel: (515) 224-1929
Fax: (515) 224-1352
Email: info@microware.com
Web: <http://www.microware.com>

Western Regional Office
2055 Gateway Place, Suite 400
San Jose, CA 95110
Tel: (408) 451-3999
Fax: (408) 451-3998

Northeastern Regional Office
One Crank Road
Hampton Falls, NH 03844
Tel: (603) 929-4107
Fax: (603) 929-4233

Southeastern Regional Office
2611 N.E. 6th Street
Pompano Beach, FL 33062-4926
Tel: (305) 946-9280
Fax: (305) 946-9350

South Central Regional Office
Great Hills Corporate Center I
Suite 220
9020 Capital of Texas Highway North
Austin, TX 78759
Tel: (512) 794-0247
Fax: (512) 794-0251

United Kingdom

Microware Systems (U.K.) Limited
Beech Court
27/33 Summers Rd
Burnham SL1 7EP
United Kingdom
Tel: (44) 1628 667578
Fax: (44) 1628 667579

France

Microware Systems France
Chateau de la Saurine
Pont de Bayeux
13590 Meyreuil, France
Tel: (33) 42.58.63.00
Fax: (33) 42.58.62.28

Japan

Microware Systems K.K.
17-3, Sotokanda 2-Chome
Chiyoda - Ku
Tokyo 101, Japan
Tel: (81) 3-3257-9000
Fax: (81) 3-3257-9200

Germany

Dr. Rudolf Keil, GmbH
Gerhart-Hauptmann-Str.30
D-69221 Dossenheim
Germany
Tel: (49) 6221-862091
Fax: (49) 6221-861954

Switzerland

Elsoft AG
Tafernstr. 20
5405 Baden - Dattwil
Switzerland
Tel: (41) 56-83-3377
Fax: (41) 56-83-3020

Australia

Microprocessor Consultants Pty. Ltd.
23 Norma Road
Palm Beach 2108
NSW Australia
Tel: (61) 2-974-4917
Fax: (61) 2-974-4900

SDS C and C++ Compilers

Compiler, Debugger, Libraries, Utilities
Software Development Systems, Inc.

SDS offers several easy-to-use compiler suites that integrate seamlessly with our debugging environment for embedded real-time development. Our C and C++ compilers generate fast, compact, code. This optimized code is superior in its reliability.

These compilers are integrated with SDS's SingleStep source-level debugger. SingleStep's intuitive graphical interface runs seamlessly under both Windows and UNIX.

SingleStep also offers an innovative kernel-aware API that gives you point-and-click kernel awareness for both internally developed and off-the-shelf real-time kernels and operating systems. Kernel awareness is available today for many different kernels including pSOSystem, VxWorks, C EXECUTIVE, Nucleus, RTEK, RTX, OSE, MQX, AMX, and SuperTask!

SingleStep is available in many different varieties, including:

- *Advanced Simulator/Debugger* lets you develop your software and hardware in parallel.
- *On Chip Debugger* provides a simple target connection through JTAG and JTAG-like ports and offers you extremely fast downloading speeds.
- *Target Monitor Debugger* is available for many off-the-shelf boards and can be easily adapted to any custom hardware configuration.
- Versions that talk to Ethernet and various emulator and emulator-like products are also available.

Features

- Superior and reliable code optimization.
- Extremely responsive support.
- Runs seamlessly under Windows and UNIX (Motif and OpenLook).
- Extensive support for C++, including templates and exception handling.
- Includes assemblers, linkers, librarians, and run-time library source-code.
- Full support for all PowerPC processors.
- Integrated with the SingleStep embedded, real-time debugging environment:
 - Easy-to-use debugger
 - Integrated with kernels and RTOSs
 - Advanced simulation technology
 - Fast JTAG support
 - Adaptable to any target configuration
 - Works with any editor or make utility

Cross-Development Environments (Embedded)

Processors Supported

- All PowerPC microprocessors.
- Other processor architectures are also supported.

Host Systems Supported

- Windows, Windows NT, Windows 95.
- SunOS.
- Solaris.
- HP-UX.

Availability

- SingleStep's latest version is currently available. See "SingleStep™" on page 134. For a free Starter Kit, call or visit the Software Development Systems web site at <http://www.sdsi.com>.

Contact

North America

Software Development Systems, Inc.
815 Commerce
Suite 250
Oak Brook, IL 60521
USA
Tel: (630) 368-0400
Fax: (630) 990-4641
Email: sales@sdsi.com
Web: <http://www.sdsi.com>

Europe

Software Development Systems, Ltd.
Berkhamsted House
121 High Street
Berkhamsted
Hertfordshire HP4 2DJ
UK
Tel: +44 (0) 1442 876065
Fax: +44 (0) 1442 873262
sales@sdsuk.demon.co.uk

Japan

A. I. Corporation
IIJIMA Building 6F
2-25-2 Nishi-Gotanda
Shinagawa-ku, Tokyo 140
Japan
Tel: +81 (0) 334 937981
Fax: +81 (0) 334 937993

Asia-Pacific

Beijing Xuanji S&T Co.
Dongyuan Electron Bldg
No. B 3 Xitcheng Rd.
Haiden District
100088 Beijing
Peoples Republic of China
Tel: +86 10 623 83376
Fax: +86 10 623 72872

Tornado™

Debugger, Operating System, Real-Time Tool, Utilities

Wind River Systems, Inc.

The Tornado development environment consists of the Tornado tools suite, the VxWorks® RTOS, and a full range of communications options connecting host and target. It is available for both UNIX®- and Microsoft Windows™-based hosts. All Tornado tools can be used at any stage of application development, with any level of target system resources. All tools are fully integrated and have sophisticated GUIs, and all are available regardless of target connection strategy (Ethernet, serial, ICE, ROM monitor or custom). The Tornado APIs are published, from the GUI interfaces down to the debug agent interface, to facilitate customization and third-party integration. You also can take advantage of a variety of productivity-enhancing WindPower™ Tools, including the VxSim™ simulator, the WindView™ system visualizer, and the StethoScope data monitor.

VxWorks provides fast multitasking, preemptive scheduling (with optional round-robin scheduling for same-priority tasks), and fast interrupt response. To these microkernel features, VxWorks adds intertask communications and synchronization facilities, efficient memory management, multiprocessing support, a fast I/O system, IDE and SCSI support, and MS-DOS and RT-11-compatible file systems.

Tornado networking includes 4.3 BSD UNIX TCP/IP, sockets, NFS, RPC, ftp, rlogin, telnet, and optional support for the

X Window System™. Tornado-based systems can communicate with each other and with UNIX via network connections over Ethernet, serial lines, or shared memory over a common backplane. A wide range of integrated third-party products is available through Wind River's WindNet™ Partners program, including ATM, OSI, SS7, Frame Relay, CORBA, ISDN, X.25, CMIP/GDMO, and distributed network management.

Features

- Makes all tools available regardless of target resources or connection strategy.
- Runs on UNIX workstations, or PCs using Microsoft Windows 95™ or Windows NT™.
- Offers published APIs for easy customization and third-party tool integration.
- Provides central "control panel" and productivity-enhancing GUI.
- Supports industry standards including ANSI-C, POSIX and TCL.
- Includes proven, high-performance VxWorks run-time.
- Scalable across all real-time implementations.

Availability

- Available now.

Cross-Development Environments (Embedded)

Wind River Systems, Inc.

1010 Atlantic Avenue
Alameda, CA 94501
Toll-Free: (800) 545-WIND
Tel: (510) 748-4100
Fax: (510) 814-2010
Email: inquiries@wrs.com
Web: <http://www.wrs.com>

North American Sales Offices

3504 Lake Lynda Dr., Ste. 155, Orlando, FL 32817
Tel: (407) 273-4646 Fax: (407) 273-5075

266 Cabot St., Ste. 8, Beverly, MA 01915
Tel: (508) 927-3334 Fax: (508) 927-6155

953 Countess Drive, Yardley, PA 19067
Tel: (215) 493-6365 Fax: (215) 493-7303

2516 Cliffbourne Place NW, Washington DC 20009
Tel: (202) 745-1048 Fax: (202) 745-1049

1901 No. Roselle Rd, Ste 800, Schaumburg, IL 60195
Tel: (847) 490-6062 Fax: (847) 490-6511

2550 Daniel Johnson Boulevard Suite 800
Laval (Quebec) H7T 2L1 Canada
Tel: (514) 990-0865 Fax: (514) 688-0464

3666 Paxton Rd, Ste. 14, Cincinnati, OH 45208
Tel: (513) 533-5881 Fax: (513) 533-5891

4201 Spring Valley Rd, Ste. 1400, Dallas, TX 75244
Tel: (214) 776-3555 Fax: (214) 776-3556

5201 Great America Pkwy, Ste. 321
Santa Clara, CA 95054
Tel: (408) 562-5769 Fax: (408) 562-5772

11000 SW Stratus, Ste. 330, Beaverton, OR 97008
Tel: (503) 646-5480 Fax: (503) 646-5637

4275 Executive Square, Ste 800, La Jolla, CA 92037
Tel: (619) 546-2835 Fax: (619) 558-8918

4600 South Ulster St., Ste. 700, Denver, CO 80237
Tel: (303) 486-0850 Fax: (303) 486-0853

Contact

101 East Victoria Street, Ste. 20
Santa Barbara, CA 93101
Tel: (805) 965-7901 Fax: (805) 965-1699

28202 Cabot Road, Ste. 300
Laguna Niguel, CA 92677
Tel: (714) 365-5745 Fax: (714) 365-5749

France

Wind River Systems S.A.R.L.
19, Avenue de Norvège
Immeuble OSLO, Bâtiment 3
Z. A. de Courtaboeuf
91953 Les Ulis Cédex
Tel: 33-1-60092-63-00 Fax: 33-1-60-92-65-15

Germany

Wind River Systems GmbH
Freisinger Straße 34
Postfach 1320
D-85737 Ismaning
Tel: 49-89-96-24-45-0 Fax: 49-89-96-24-45-55

United Kingdom

Wind River Systems UK Ltd
Unit 5, 2nd Floor, Ashted Lock Way
Aston Science Park
Birmingham B7 4AZ
Tel: 44-(0)-121-628-1888 Fax: 44-(0)-121-628-1889

Sweden

Wind River Systems Scandinavia
Turebergs Torg 1
S-191 47 Sollentuna
Tel: 46-8-92-15-80 Fax: 46-8-92-15-65

Japan

Wind River Systems Japan/Asia Pacific
Pola Ebisu Bldg. 11F
3-9-19 Higashi
Shibuya-ku
Tokyo 150
Tel: 81-03-5467-5900 Fax: 81-03-5467-5877

Italy

Via Morghen, 22, Torino, 10143
Tel: 39-11-741-2749 Fax: 39-11-741-2044

Application-Specific Tools

Printer Controller Reference Port

Controller, Emulator/Simulator, Interpreter

Adobe Systems, Inc.

Adobe Systems is working with IBM to develop a PowerPC reference software port that is the basis for IBM PowerPC 40x-based design efforts by original equipment manufacturers (OEMs).

The reference port accepts PostScript Language programs and drives a printer-marking engine. This constitutes a prototyping environment for use in creating engineering prototype PostScript Printers. In addition, a PowerPC-based reference controller is available, with marking engine, together constituting an engineering PostScript Printer.

The reference port can be used by OEMs to develop custom printer controllers to meet a wide range of performance requirements.

Application-Specific Tools

Availability

- Available now.

Contact

Adobe Systems Inc.
P. O. Box 7900
Mountain View, CA 94039-7900
Tel: (415) 961-4400
Fax: (415) 961-3769
Web: <http://www.adobe.com/>

PowerPC Embedded ABI Test Suite (PEATS)

Test Suite

Applied Testing and Technology, Inc.

The PowerPC Embedded ABI Test Suite (PEATS) verifies the ability of development tools to produce and consume files compliant to the PowerPC Embedded Application Binary Interface (EABI), Version 1.0:

- Verifies that C compilers produce correct objects.
- Verifies that linkers produce correct executables.
- Verifies that archivers produce correct archive files.
- Verifies that linkers and archivers understand correct input files.

Testing with PEATS facilitates product reliability as well as interoperability between tools, debuggers, and libraries from multiple vendors. PEATS performs a large series of tests covering EABI requirements for:

- ELF
- DWARF
- Data layout
- Calling conventions
- Archive file format

Testing primarily entails compilation of custom C test programs, analysis of the resultant object, linking with objects from a trusted toolset, and analysis of the resultant executable. Supplemental tests are employed which execute generated code in a PowerPC environment.

The general categories of checks made by PEATS include:

- Object-file syntactic checks.
- Source-to-object semantic checks.
- Object-to-object linker consistency checks.
- Incremental linking.
- Cross linking (mixing optimized and non-optimized modules, etc.).
- Archive syntax checks.
- Object-to-archive consistency checks.
- Archive usability checks.
- Tool set interoperability (mixing with trusted objects).
- Run-time checks of caller-callee linkage, relocation, data representation, data layout, and section combining and locating.

A unique feature of PEATS is its validation of ELF/DWARF semantics. PEATS employs a translator which reads an arbitrary C program and generates expectations about the ELF/DWARF information that should be produced when it is compiled. PEATS then compares this information to the ELF/DWARF actually produced by the compiler under test for the source program. PEATS reports any errors noticed as well as flagging inconsistent DWARF usage and deviations from recommended practice.

Application-Specific Tools

Test operation is managed by the DejaGnu test harness, a Tcl-based framework originally developed for testing GNU tools. DejaGnu offers PEATS users:

- Compliance with POSIX standard 1003.3.
- A uniform command-line interface to the testing process.
- Flexibility and extensibility for development of additional tests.
- Portability across native and cross-development platforms.

Features

- Tests ELF and DWARF syntax and semantics.
- Tests data layout, calling conventions, and archive file format.
- Includes static and run-time tests.
- Completely automated.
- Full user and programmer documentation.
- Highly configurable—works with any tool set.
- Highly extensible—users can easily add their own test extensions.
- Operates under the DejaGnu test harness.
- Extensive support and maintenance program.

System Requirements

- Runs on AIX4 and Windows 95.

Availability

- Beta availability: now.
- General availability: Q4 96.

Contact

Applied Testing and Technology, Inc.

59 North Santa Cruz Avenue
Suite U
Los Gatos, CA 95030 USA
Tel: (408) 399-1930
Fax: (408) 399-1931
Email: aptest@aptest.com
Web: <http://www.aptest.com/>

DAVID Audio/Visual Interactive Decoder

Multimedia Tool, Real-Time Tool, Utilities

Microware Systems Corporation

DAVID (Digital Audio/Video Interactive Decoder) is a standard operating system environment for interactive television decoders that can be used in telephone, cable TV and wireless networks. Created and licensed by Microware Systems Corporation, DAVID is based on Microware's OS-9[®] real-time operating system. The DAVID system supports both network and local interactive applications, graphics and user interfaces.

IBM, Philips, Zenith, ICTV, Goldstar, Samsung, Kyocera, and six other manufacturers have built DAVID-based decoder products that were deployed in networks in 1994 and 1995. Also, the DAVID system is supported by leading video server providers, such as Oracle (nCUBE), and DEC assuring an end-to-end solution for interactive television.

For everyone who will provide content for interactive networks, such as movie and TV studios, educational and government institutions, banks and retailers, the DAVID system provides a complete platform to target multimedia applications.

Developers need only program their applications once under the DAVID system. DAVID's portability on a variety of decoders, coupled with DAVID network protocol supporting the connecting decoders to various video servers, gives application developers the assurance of true interoperability across telephone and cable networks.

The DAVID development environment integrates easily into existing popular multimedia tool sets. Existing CD-i, CD-ROM, Mac- and PC-based assets can be converted quickly into DAVID system applications. The DAVID development environment is supported on low-cost platforms that allow both computer programmers and artists alike to emulate the actual network on their desktop, thus enabling not only the creation but also the validation of interactive applications.

Features

- An open system-software standard for IDTV decoders.
- Provides interoperability between cable, telephone and wireless networks.
- Provides interoperability between video servers and set-tops.
- Supports industry leading multimedia authoring tools and applications.

Video Server and Network Providers

Low-cost DAVID-based decoders are currently being manufactured and will soon be available in quantity. Existing video servers currently work with DAVID-based decoders via a common DAVID network protocol. Thus, DAVID is a complete system that can be integrated into existing switching systems, line cards and cable head-ends. For telephone, cable and wireless networks, targeting DAVID is the fastest and most comprehensive path to interactive television deployment.

Application-Specific Tools

Decoder Manufacturers

DAVID can be easily configured for use with digital video set-top and head-end decoders. The DAVID installation package consists of the OS-9 real-time operating system, a critical component for interactive television, plus all the system components necessary for decoder functionality such as network communications, MPEG decoding and user interface. The DAVID package also contains a comprehensive suite of device drivers for popular, off-the-shelf MPEG, graphics and communications hardware. Microware's nearly two-decades' worth of experience in supporting embedded systems designs, along with DAVID's portability, makes integration fast and easy.

System Requirements

- Resident OS-9 and cross-development platforms, including most popular UNIX workstations.
- For suggested decoder and platform specification, please contact a Microware representative.

PowerPC Processors Supported

- PowerPC 403GA and 403GC embedded controllers.
- PowerPC 603, 604, and 620 microprocessors.

Availability

- Available now.

Contact

United States

Microware Systems Corporation
Corporate Headquarters
1900 N.W. 114th Street
Des Moines, IA 50325-7077
Tel: (515) 224-1929
Fax: (515) 224-1352
Email: info@microware.com
Web: <http://www.microware.com>

Western Regional Office
2055 Gateway Place, Suite 400
San Jose, CA 95110
Tel: (408) 451-3999
Fax: (408) 451-3998

Northeastern Regional Office
One Crank Road
Hampton Falls, NH 03844
Tel: (603) 929-4107
Fax: (603) 929-4233

Southeastern Regional Office
2611 N.E. 6th Street
Pompano Beach, FL 33062-4926
Tel: (305) 946-9280
Fax: (305) 946-9350

South Central Regional Office
Great Hills Corporate Center I
Suite 220
9020 Capital of Texas Highway North
Austin, TX 78759
Tel: (512) 794-0247
Fax: (512) 794-0251

United Kingdom

Microware Systems (U.K.) Limited
Beech Court
27/33 Summers Rd
Burnham SL1 7EP
United Kingdom
Tel: (44) 1628 667578
Fax: (44) 1628 667579

France

Microware Systems France
Chateau de la Saurine
Pont de Bayeux
13590 Meyreuil, France
Tel: (33) 42.58.63.00
Fax: (33) 42.58.62.28

Japan

Microware Systems K.K.
17-3, Sotokanda 2-Chome
Chiyoda - Ku
Tokyo 101, Japan
Tel: (81) 3-3257-9000
Fax: (81) 3-3257-9200

Germany

Dr. Rudolf Keil, GmbH
Gerhart-Hauptmann-Str.30
D-69221 Dossenheim
Germany
Tel: (49) 6221-862091
Fax: (49) 6221-861954

Switzerland

Elsoft AG
Tafernstr. 20
5405 Baden - Dattwil
Switzerland
Tel: (41) 56-83-3377
Fax: (41) 56-83-3020

Australia

Microprocessor Consultants Pty. Ltd.
23 Norma Road
Palm Beach 2108
NSW Australia
Tel: (61) 2-974-4917
Fax: (61) 2-974-4900

PowerPage® Level 2

Interpreter

PIPELINE

The PowerPage® Level 2 interpreter is a fully-compatible implementation of Adobe's PostScript Level 2 page description language, according to the PostScript Language Reference Manual, Second Edition. It is designed with the flexibility to drive any printer, typesetter, or display technology. All output options are supported: black & white and color on binary and continuous-tone marking engines. The PowerPage Level 2 interpreter is written in the C programming language to provide maximum flexibility and portability across platforms. The interpreter is presently shipping in OEM products configured on an embedded controller, stand-alone controller, and as a host-based soft-RIP solution. It also functions as a distiller for PostScript code and for previewing.

The code is structured so that configuration for different device-specific features (e.g. color, paper size, margins, and resolution) can be specified to the interpreter at start-up time. All standard PostScript Level 2 features are supported, such as: composite (Type 0) format fonts, device-independent color (CIE 1931), forms and form caching as well as patterns and pattern caching. The interpreter can also be configured to drive output devices directly or to write a bitmap to disk.

The PowerPage Level 2 interpreter incorporates Pipeline's TypeOne™ Rendering System, a software library used for the decryption, decoding, and rendering of Adobe Type 1 format fonts with hints.

The proprietary PowerPage Printer Operating System (PPOS) is also available for licensing with the PowerPage Level 2 interpreter. PPOS is a real-time operating system developed by Pipeline to support all

industry-standard and OEM-specific custom features. Some of the features PPOS offers are: platform independence, emulation switching, I/O handling, auto-port sensing, memory management, a file system, front panel interface, PCMCIA/JEIDA slots, and engine handling services.

PowerPage Level 2 is also available in optimized versions, customized to support specific market needs. PowerPage Level 2J, optimized for the Asian market, supports Type 4 disk-resident fonts and downloadable Kanji fonts from suppliers such as NIS, Bitstream, Morisawa, and Adobe. In addition, Level 2J supports the undocumented PostScript operators found in Adobe Kanji PostScript printers.

PowerPage Level 2C extends the Level 2 language by adding special operators to improve the processing time of CorelDRAW files while maintaining 100% compatibility. Depending upon the complexity of the image, PowerPage Level 2C processes images up to 10 times faster than similar Adobe-based printers.

PowerPage DLL is a Windows-compatible DLL version of the PowerPage Level 2 interpreter and is available to OEMs to provide easy integration into Windows applications. PowerPage DLL allows for the customization of the user interface and are designed to output raw data or BMP files, with TIFF and other format files available upon request.

Source code is available to the OEM for all PowerPage technologies.

Application-Specific Tools

Devices Supported

- Black and white printers (from 4 to 50+ ppm), facsimiles, and monitors.
- Grayscale monitors and printers.
- Single-bit/pixel color, three or four color.
- Continuous-tone, one, three or four color.
- Film recorders and imagesetters.

Processors Supported

- IBM PowerPC 400 Series.
- IBM PowerPC 600 Series.

Hosts Supported

- PowerPage Printer Operating System (PPOS).
- System 7.5 PowerMac.
- MS-DOS.
- Windows 3.1, Windows 95, Windows NT.
- UNIX.
- OS/2.
- Embedded operating systems.

Code Size

- Approximately 1.75 MB ROM (includes 35 Type1 fonts).
- Minimum RAM requirements are typically 1.5 MB for cache, VM, runtime data structures, plus framebuffer space (varies depending on rendering model used).

Supplied Fonts

- 35 ATM-compatible fonts, royalty-free.

Font Rasterizers

- Built-in Type 0, Type 1, and Type 3 (user defined) font support.
- Proprietary Type 1 grayscale font rasterizer (TypeOne® Rendering System).
- Type 4 (disk resident) format fonts (PowerPage Level 2J).

Rendering Models

- Frame device (full memory).
- Band device (display list).
- PowerBand memory reduction model requires only one-fourth the memory to image pages without requiring a hard disk.

Image Enhancement Technologies

- PowerSmooth gradient smoothing technology for 1-bit/pixel output devices.
- Error diffusion technology for less than full continuous-tone output devices.
- Anti-aliasing technology for text and graphic images on grayscale and continuous-tone output devices.

Options

- Source code.
- Custom engineering.
- Direct Pipeline technical support.
- Corel Optimized Printing.
- Asian font support.

Availability

- Available now.

Contact

PIPELINE

2740 Route 10 West
Morris Plains, NJ 07950
Tel: (201) 267-3840
Fax: (201) 267-3715
Email: info@powerpage.com

PowerPage PCL 5C

Interpreter

PIPELINE

The PowerPage PCL 5C emulation is a fully compatible implementation of Hewlett-Packard's PCL 5C printer language based on their Color LaserJet 5M printer. This emulation contains the complete set of color commands developed by HP to expand the capability of any color printer and specifically supports color palette caching, device independent color, and selectable resolution. PowerPage PCL 5C includes support for the 35 scalable Intellifont typefaces and 10 scalable TrueType typefaces compatible with those included in the Color LaserJet 5M printer. A custom PCL 5C Windows driver, with optional built-in ColorSmart compatibility and user-friendly screen calibration interface, is also available.

The code is structured so that the configuration for different device-specific features (e.g. resolution, paper size, etc.) can be specified to the emulation at start-up time. Source code is available to the OEM to allow integration into existing environments, as well as to allow the OEM to modify, enhance, and maintain the emulation if so desired.

Pipeline's implementation of PCL 5C is designed to be hardware and software independent. The interpreter is also compatible with Hewlett-Packard's LaserJet IIIsi and LaserJet 5 Plus printers for monochrome applications.

PowerPage PCL 5C includes the three modes defined by HP to provide color compatibility for color output devices. The first is the "simple color" mode. In this mode, a device can handle 3-bit data. The second is invoked by the "imaging color" command. This mode enables an output device to handle up to 24-bits of calibrated color data. Finally, color capability can be accessed using the existing color commands in HP-GL/2.

PowerPage PCL 5C also includes the built-in halftoning capability found in the HP Color LaserJet printer. Five different halftoning patterns are available, including: pattern dithering, cluster dithering, error diffusion, and programmable dither that permits users to set the dither matrix to one of four sizes. Each of these halftoning patterns can be used in color or monochrome mode.

Application-Specific Tools

Compatibility

The PowerPage PCL 5C emulation is a fully compatible implementation of Hewlett-Packard's PCL 5C printer language based on their Color LaserJet 5M printer.

Devices Supported

- Three or four color one-bit per pixel output devices.
- Black & white printers, facsimile, and monitors.

Supplied Fonts

- 35 scalable Intellifont typefaces.
- 10 scalable TrueType typefaces.
- Line printer PCL bitmap font.
- Font rasterizers must be licensed directly from the respective foundries.

Processors Supported

- IBM PowerPC 400 Series.
- IBM PowerPC 600 Series.

Hosts Supported

- PowerPage Printer Operating System (PPOS).
- MS-DOS.
- Windows 3.1, Windows NT, Windows 95.
- UNIX.
- Embedded operating systems.

Rendering Models

- Frame device (full memory).
- PowerBand patented memory reduction model.

Options

- PCL 5C Windows Driver complete with optional ColorSmart capability.
- Custom Color Screen Calibration utility.
- Proprietary selectable resolution feature.
- Custom engineering.
- Direct Pipeline technical support.

Availability

- Available now.

Contact

PIPELINE

2740 Route 10 West,
Morris Plains, NJ 07950
Tel: (201) 267-3840
Fax: (201) 267-3715
Email: info@powerpage.com

PowerPage PCL 5e

Interpreter

PIPELINE

The PowerPage® PCL 5e emulation is a fully compatible implementation of Hewlett-Packard's PCL 5 printer language as described in the PCL 5 Printer Language Technical Reference Manual. The feature set supported by this emulation is based on the HP LaserJet 5 Plus printer. Significant enhancements were made to the PCL 5 printer language (PCL 5e) with the introduction of the LaserJet 4 printer. All enhancements are supported by PowerPage PCL 5e and include: 600 dpi support for higher quality printing, 35 scalable Intellifont typefaces, and 10 scalable TrueType typefaces for fast Windows printing and greater type variety. Agfa's MicroType font format is also supported by PowerPage PCL 5e, which dramatically reduces the OEM's ROM requirements as well as ensures the fastest times possible for rasterizing text.

Pipeline also offers extensions to the PCL 5e language to support an optional hard disk. This includes support for downloading fonts and macros to the hard disk from a host CPU.

The emulation offers OEMs total control over their hardware/software design and is totally written in the C programming language to provide maximum flexibility and portability across platforms. The code is structured so that the configuration for different device-specific features (e.g. resolution, paper size, etc.) can be specified to the emulation at start-up time. Source code is available to the OEM allowing integration into existing environments, as well as to allow the OEM to modify, enhance, and maintain the emulation if so desired.

Pipeline's implementation of PCL 5 is designed to be hardware and software independent. The emulation is also compatible

with Hewlett-Packard's LaserJet IIIsi printer and Color LaserJet 5M printer for color applications. All versions of the emulation make use of two different rendering models: frame device for full memory and the patented PowerBand® memory reduction technology. PowerBand compression/decompression software processes images in one-fourth the amount of memory typically needed to process a full frame. PowerBand is table-driven, making it easy to plug in new compressors. It uses lossy compression techniques assuring all pages can be imaged. PowerBand is also available in ASIC form.

PowerPage PCL 5e also includes:

- Support for new graphics commands for faster and better curves and shading quality
- Bi-directional I/O for easier use and sharing by providing printer status to software applications
- Improved PCL and HP-GL/2 performance for faster graphics and text printing and support for Logical Operations (ROP3).

The proprietary PowerPage Printer Operating System (PPOS) is also available for licensing with the PowerPage PCL 5 emulation. PPOS is a real-time operating system developed by Pipeline to support all industry-standard and OEM-specific custom features while guaranteeing a one-stop solution for all application support. Some of the features PPOS offers support for are: platform independence, emulation switching, I/O handling, auto-port sensing, memory management, a file system, front panel interface, PCMCIA/JEIDA slots, and engine-handling services.

Application-Specific Tools

Pipeline offers PCL 5 Windows drivers that can be customized for special paper handling and unique printer features. These drivers are available for Windows 3.1, Windows 95, and Windows NT environments. B-directional monitor software can also be licensed directly from Pipeline. OEM's can therefore turn to Pipeline for a COMPLETE PCL printing solution.

Compatibility

The PowerPage PCL 5e emulation is a fully compatible implementation of Hewlett Packard's PCL 5 printer language as defined in the PCL 5 Printer Language Technical Reference Manual and is based on their LaserJet 5 Plus printer.

Devices Supported

- Black & white printers, facsimile, and monitors.
- Color printers, through PowerPage PCL 5C.

Supplied Fonts

- 35 scalable Intellifont typefaces.
- 10 scalable TrueType typefaces.

Processors Supported

- IBM PowerPC 400 Series.
- IBM PowerPC 600 Series.

Hosts Supported

- PowerPage Printer Operating System (PPOS).
- MS-DOS.
- Windows 3.1, Windows 95, Windows NT as a DLL.
- UNIX.
- Embedded operating systems.

Rendering Models

- Full-frame memory.
- PowerBand patented memory reduction model.

Options

- Source code.
- Hard disk support.
- Custom engineering.
- Direct Pipeline technical support.
- Customizable drivers for Windows 3.1, Windows 95, and Windows NT.

Availability

- Available now.

Contact

PIPELINE

2740 Route 10 West,
Morris Plains, NJ 07950
Tel: (201) 267-3840
Fax: (201) 267-3715
Email: info@powerpage.com

USNET

Code, Real-Time Tool, Utilities

U S Software

USNET is a processor-independent network protocol set specifically designed for use with real-time, embedded applications. Drop-in support is provided for the PowerPC processor and the most popular toolchains.

USNET is reentrant to insure proper operation with real-time multitasking systems such as MultiTask!. USNET may be used in applications where another RTOS is already in place, or where an operating system is neither an option nor a consideration. As with all U S Software products, source code is included and highly structured for versatility and user customization.

Features

- Client/server functions for the internet protocol suite.
- OS-independent
- Processor-independent
- Compact implementation
- User-configurable
- Drop-in toolchain support
- ROMable and reentrant
- Full source code
- BSD sockets
- Client/servers:
FTP, TFTP, TELNET, BOOTP, DHCP
- Protocols:
TCP, UDP, IP, ICMP, ARP, RARP, SLIP, PPP
- Ethernet drivers
- Serial drivers
- ARCnet drivers
- PCMCIA card and socket support
- SNMP Version 1 and Version 2

User Interface

Applications may interface to USNET in a number of ways including a client/server function interface, a dynamic protocol stack interface, and BSD sockets.

Drop-in Target Support

Drop-in support is provided for many popular target processors and toolchains. This support includes toolchain makefiles, drivers, interrupt code, sample timer/display code, and sample startup code.

Device Drivers

USNET includes drivers and network link layers for Ethernet, serial (SLIP, PPP) and ARCnet.

Configuration

Code and data space are usually at a premium in a real-time embedded system. USNET may be configured to only use those client/servers, protocols, link layers, and drivers needed by your application. The complete TCP/IP protocol including all needed routines takes about 25K of code space on most target processors. The fixed RAM requirement is typically less than 29K. Each active connection requires buffer space.

Test Programs

USNET includes test programs to verify installation and communications.

Implementation Services

U S Software offers product implementation and customization services.

Application-Specific Tools

Availability

- Available now.

Contact

U S Software

14215 NW Science Park Drive
Portland, OR 97229
Tel: (800) 356-7097
Tel: (503) 641-8446
Fax: (503) 644-2413
Email: info@ussw.com
Web: <http://www.ussw.com>

GOFAST Floating-Point Libraries

Code, Libraries

U S Software

U S Software's world renowned numeric technology offers "link and go" solutions for the PowerPC processor as well as a family of GOFAST libraries. Fast, reentrant and ROMable, the libraries can dynamically detect and select a hardware coprocessor if it exists, even when resident in ROM.

The GOFAST IEEE 754 Floating-Point Libraries are composed of single precision (32 bit format) and double precision (64 bit format) floating point routines in modular source assembly form.

Features

- Emulator: PPC602, general version.
- Libraries: EABI interface, ANSI C.
- Optimized for speed
- Floating point operations include: add/subtract, multiply, divide, square root, sine, cosine, tangent, arctangent, exponentiation, log, natural log.
- ASCII and Integer conversion routines.
- Source code.
- Conformance and testing accuracy within one bit for arithmetic functions and two bits for transcendental functions.

Application-Specific Tools

Custom Libraries

U S Software supports OEM's with specifically tailored libraries to suit their specific needs.

Availability

- Available now.

Contact

U S Software

14215 NW Science Park Drive
Portland, OR 97229
Tel: (800) 356-7097
Tel: (503) 641-8446
Fax: (503) 644-2413
Email: info@ussw.com
Web: <http://www.ussw.com>

FDS-Mate

User Interface, Utilities

w-CUBE Software Corporation

FDS-Mate is a graphical tool supporting PowerPC development that is applicable to a wide spectrum of applications. It provides a variety of GUI components such as color images, various figures, graph tools, and an integrated spread sheet. It is specifically designed for high up-time, high reliability, real-time applications where rapid updating of screen data is critical. This makes FDS-Mate very suitable for use in plant control, communications, production management, Factory Automation (FA) and Laboratory Automation (LA) applications where continuous, 24-hour-per-day usage is essential.

FDS-Mate provides a dynamic development environment under X-Windows on UNIX and UNIX-like operating systems. It is a Dynamic Data Visualization Tool (DDVT) which supports a rich selection of windowing environments. It is fully optimized for performance and covers high-end stand-alone systems as well as deeply embedded systems of a highly complex nature.

FDS-Mate provides an easy-to-use, totally integrated, on-line development system that allows you to layout screens, define the interfaces needed, test the GUI and then generate optimized code. The FDS-Mate Window Lib shortens training and reduces the time spent on application maintenance. This highly optimized Window Lib runs on minimized functions that are 1/8 to 1/5 less than that of Xlib, Xt, and Xm.

With an understanding of the fundamentals of the C language, you can use FDS-Mate to design and build applications smoothly and easily. Productivity is significantly increased while the total training period is greatly reduced and maintenance is simplified.

Functions of the FDS Window Library

- *Unified management of the Window's functions*—Controls various window functions such as rise-up, icon, and dependent management of a window function or window functions between different processes.
- *Abundant event handling*—Can start the registered processing program automatically, with precise judgement of various events such as messages, window events, key input events and mouse events. It also can accept and handle events of Xlib or non-Xlib directly.
- *Graph tool*—Circle, bar, solid, cylinder and radar-chart graphs are supported.
- *Maximum performance with a minimum of functions*—The overall size of the FDS Windows Library is approximately 1/4 that of the Motif toolkit, making it easier to use.
- *Provides interfaces to OSF/Motif and OpenLook*—Supports Motif and OpenLook applications you may have already developed. FDS-Mate functions can be used in existing application software.
- *High speed drawing and shared memory*—Configured for high speed drawing and real-time systems. Program size is minimized by a shared memory architecture.
- *Acts as an easy-to-use layout editor*—The display layout can be developed from your image through simple keyboard and mouse operations. Various functions such as move, copy, cut & paste, undo, etc. are provided.
- *Image printing and output*—Display images can be printed at a PostScript printer as they are being developed.

Application-Specific Tools

- *Extensive color support*—Flexible color support is provided through a “palette mode” (selects a color from the color database supported by X-Windows) and “custom mode” (you produce custom colors by the direct combination of RGB).
- *Immediate test function*—You define GUI display images that can be tested immediately with the real movement of event components, color, etc.
- *Automatic C source code generation*—Automatically generates C source programs from the GUI display image. This becomes the interface information to the FDS Window Library, allowing for prompt execution and verification of the program.

FDS-Mate Development Phases

- Using Drawing Objects, you graphically build the application program as it is to appear on the display screen.
- For each GUI Object, you define the interface (display attribute and application interface).
- You can test the GUI Object for a look and feel and produce a hard copy of the GUI display on a PostScript printer.
- When the GUI is completed to your satisfaction, FDS-Mate will generate C language source code of the GUI panel.

FDS-Mate allows PowerPC application development and prototyping to be performed quickly and easily. Displays may be modified without coding and recompiling data source programs, thereby reducing development time.

FDS-Mate's flexibility in GUI application development allows PowerPC developers to combine buttons, text and menus with spread sheets, graphs and other object drawings easily and efficiently in a WYSIWYG environment.

FDS-Mate provides complete compatibility of source code among different types of workstations, CPU architectures, and operating systems.

Operating Systems Supported

- Solaris.
- SunOS.
- AIX.
- OSF/1.
- Solaris x86.
- UnixWare.
- USIX.
- LynxOS.
- HP-UX.
- Windows NT (Future).
- Windows 95 (Future).

Availability

- Available now.

Contact

w-CUBE Software Corporation

Rebecca Davis
499 Colusa Avenue
Berkeley, CA 94707
Tel: (510) 528-0592
Fax: (510) 528-0593

Modular Multifunction Peripheral Controller Design

Controller, Interpreters, Code

Xionics Document Technologies, Inc.

Xionics Document Technologies, in partnership with IBM Microelectronics, has designed XipChip™, an application-specific integrated circuit (ASIC) optimized for raster image processing. XipChip is part of Xionics' Intelligent Peripheral System™ for multifunction peripherals (IPS-MFP), a fully integrated, low-cost controller solution for a wide range of office-quality products. XipChip implements a PowerPC 403GA core, integrated co-processors for copy, scan and fax, and a multi-channel DMA control unit that provides access to a single, ultra-high-speed memory system. This highly integrated single-chip solution lowers controller costs and provides balanced (print, copy, scan and fax speeds the same) and concurrent operation of multiple system applications.

IPS-MFP features Xionics' modular IPS Dataflow Imaging Architecture, PCL® and PostScript™ print technology, and high-quality copy, scan and fax application modules. The scalable IPS-MFP software and hardware lower manufacturing costs compared to designs based on discrete, off-the-shelf components. IPS-MFP also minimizes long-term cost of ownership by enabling OEMs to amortize up-front costs, and it permits value-added software development across multifunction and multiple single-purpose controller development projects.

The IPS Dataflow Imaging Architecture includes a core set of controller services that provide specialized image processing and data management for a variety of intelligent multifunction products.



PHOTO #5
(location marker only—
do not use keyline)

Application-Specific Tools

Core services such as the IPS graphics kernel, memory, options, file, font, menu and print queue management, network services, printer state and system tasker are shared by the PCL and PostScript printer languages and other MFP applications. This extensible design reduces time-to-market and preserves investments in controller software development through the use of a single technology base in complete families of color and monochrome products. IPS-MFP streamlines the integration of customized products by enabling OEMs to add proprietary print, copy, scan and fax applications to the system without modifying the basic IPS architecture. Xionics' XipPower™ application programming interface (API) provides an interface between the embedded applications and the IPS Dataflow Imaging Architecture core services.

IPS-MFP's built-in peripheral expansion port supports an off-the-shelf network interface card (NIC) for EtherTalk™, Novell® NetWare™ and TCP/IP network operating systems and includes multi-channel bi-directional communications for multifunction peripherals. For direct-connect configurations, IPS-MFP includes the XipChannel™ single-cable, host-to-device driver system. XipChannel permits standard host print, scan and fax applications to operate as if the host were connected to a single-purpose printer, scanner or fax device.

IPS-MFP can include Xionics' optional MFP application toolbox. XipApp™ includes a customizable Windows™ application and OCX drivers that facilitate the development of host-

based, value-added Windows application software that provides a graphical user interface to the MFP.

Features

- Integrated PowerPC 403GA ASIC controller for optimized raster image processing in multifunction peripherals. Supports concurrent and balanced system processing.
- Modular IPS Dataflow Imaging Architecture reduces time-to-market and development costs for complete families of products.
- Fully integrated, hardware-assist copy, scan and fax applications provide a complete multifunction controller solution.
- XipPower™ API accelerates custom product development and speeds time-to-market.
- Xionics' PCL and PostScript printer language interpreters provide reliable, high-quality color and monochrome printing at variable resolutions.
- Peripheral expansion port supports off-the-shelf network interface card (NIC) for connectivity with a range of network operating systems.
- Value-added XipApp host software applications provide remote front panel and graphical user interface.

Availability

- Available now.

Contact

Xionics Document Technologies, Inc.

Bob Brauer
70 Blanchard Road
Burlington, MA 01803
Tel: (617) 229-7000
Fax: (617) 229-7121

Application-Specific Tools

Hardware Development Tools

TimingDesigner®

Analyzer

Chronology Corporation

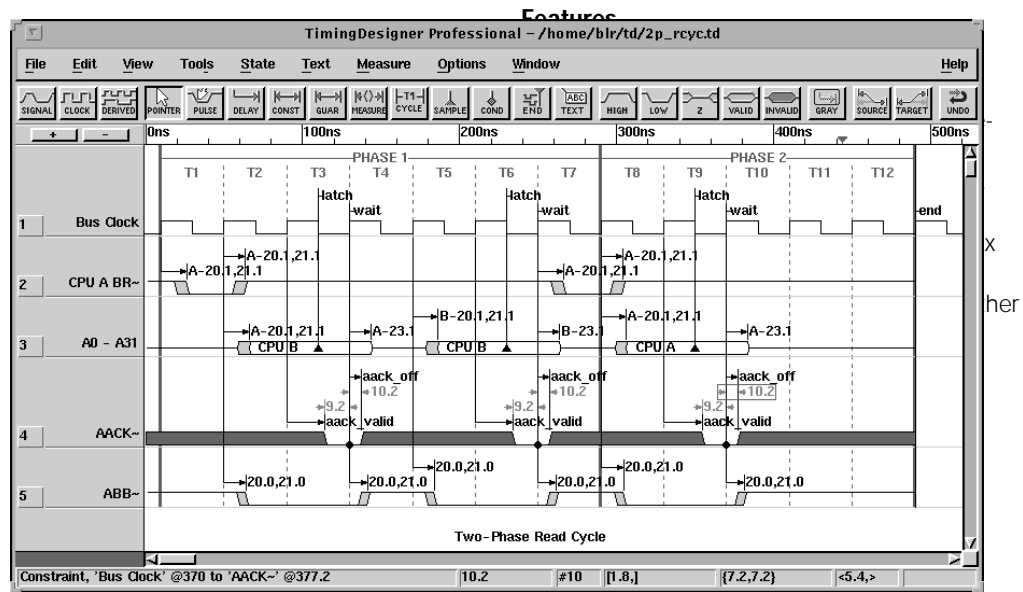
TimingDesigner is software for accurately modeling, visualizing, analyzing, and documenting digital circuit timing. Over 10,000 engineers at almost every major electronics company in the world use TimingDesigner. TimingDesigner is used with any type of design—chip, board, or system—where timing is important, or where accurate timing and interface specifications must be communicated to others.

TimingDesigner models complex digital circuit timing by combining an interactive timing diagram editor with a special purpose timing spreadsheet. You first create a timing diagram with the timing diagram editor, which shows the waveforms (sequence of events), delays (cause-and-effect relationships), and timing constraints of a proposed design. The

spreadsheet is then used to enter the min/max values of each delay and constraint. These values may be complex formulas—including min/max variables—so that path delays, different rise/fall times, loading, temperature, and other effects can be accurately modeled.

After each modification, TimingDesigner's static timing engine traces all of the delay paths specified in the timing diagram, removes common delays, adjusts for delays which track, selects the critical paths, and then computes the worst-case timing margins by comparing the total delay along each critical path to the minimum or maximum allowable value specified in each constraint. Effects of design changes are seen instantly with TimingDesigner, allowing many alternatives to be evaluated in a short time.

Hardware Development Tools



Devices

supported

Devices supported include:

- PowerPC 601 microprocessor
- PowerPC 604 microprocessor

Hardware Development Tools

Availability

- Available now.

Contact

Chronology Corporation

8405 165th Ave NE
Redmond, Washington 98052 U.S.A.
Tel: (206) 869-4227
Toll free: 1-800-800-6494
Fax: (206) 869-4229
Email: sales@chronology.com
Web: <http://www.chronology.com>

SCANTEST™

Test Suites

Corelis

SCANTEST™ is a family of IEEE-1149.1 standard compatible boundary-scan test products for development, manufacturing, and service for use with PowerPC™-based designs. The products offer solutions for design, test development, test execution, and diagnosis of components, PCBs, and systems that include a PowerPC microprocessor and other boundary-scan compatible components. With the

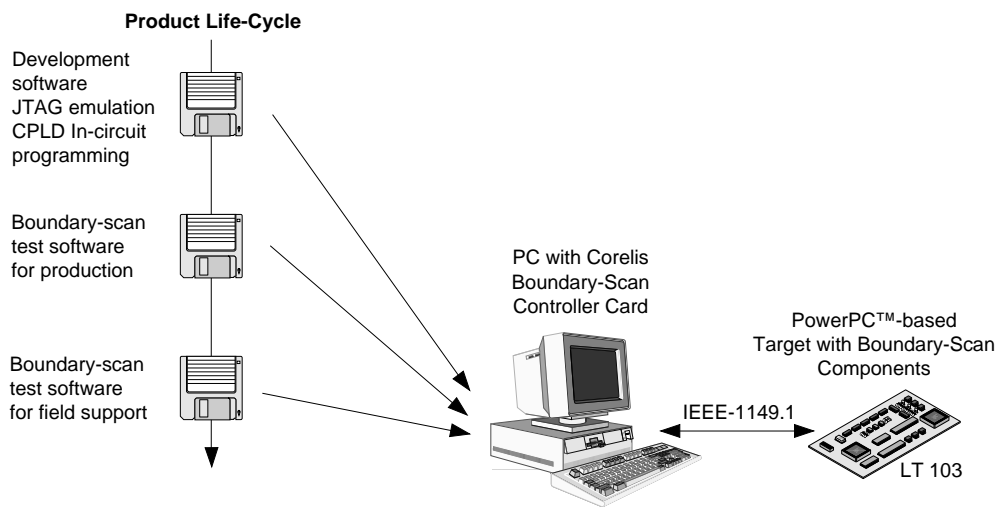
SCANTEST hardware and software products, engineers who are incorporating the PowerPC microprocessor into their designs can quickly debug their prototypes and develop efficient test procedures for interconnect tests.

The SCANTEST automatic boundary-scan test pattern generator creates test vectors for interconnect tests directly from a netlist and from boundary-scan description language (BSDL) component files. These patterns are later applied to the Unit Under Test via one of the SCANTEST boundary-scan controllers.

A comprehensive boundary-scan diagnostics package provides the location of the fault in the user's name terms for netlist, IC name, and pin number.

When any of the Corelis PowerPC family of emulators is used, the SCANTEST family of test software products can be used to provide support tools for the duration of the life-cycle of the product. This includes design and development, production, and field service and support. Please contact us for additional information.

Hardware Development Tools



Contact

Corelis Inc.

12607 Hidden Creek Way
Cerritos, CA 90703
Tel: (310) 926-6727
Fax: (310) 404-6196
Email: sales@corelis.com

Ireland

BIC Systems
Europa House
Harcourt St.
Dublin 2, Ireland
Tel: 353-14754-223
Fax: 353-14754-778

Sweden

Pelcon Electronics AB
Girovagen
S-175 06 Jarfalla
Sweden
Tel: 8-796-9870
Fax: 8-760-7685

Japan

Techno-Port Co. Ltd.
Nakagin Bldg. 10-2
Higashi-Shingashi 2-chome
Mianto-ku, Tokyo
Tel: 81-3-3434-3671
Fax: 81-3-3434-3897

Germany

Synatron
Technopark Neukeferich
Bretonischer Ring 13
D-85630 Grasbrunn
Tel: 89-460-2071
Fax: 89-460-5661

Canada

Testforce Systems
5990 Vanden Abeele
St. Laurant, Quebec
Canada H4S 1R9
Tel: (514) 856-0970
Fax: (514) 856-6983

Hardware Development Tools

Features

- BSDL Syntax and Semantics Checker.
- Automatic Test Pattern Generator.
- Test Access Port Integrity Tests.
- Interconnect Tests.
- Cluster Tests.
- BIST.
- Boundary-Scan Functional Tests.
- Boundary-Scan Diagnostics.
- Boundary-Scan Parallel I/O for Testing Edge Connectors and Non-Scannable Devices.
- Extensive consulting services, test vector translation and generation, BSDL file development and verification, training, and on-site seminars.

Platforms Supported

- PC Laptop Systems.
- SUN and HP Workstations.
- VXI/VME Systems.

Devices Supported

- PowerPC™ 403GA, PowerPC 403GB, PowerPC 603, PowerPC 603e, and PowerPC 604 microprocessors.

Availability

- Available now.

Technical Support

- Full-time product support staff, available to address technical questions and problems. Support via telephone, e-mail, and fax.

UI-MPC601 Universal Interface

Analyzer Interface

Corelis

The UI-MPC601 Universal Interface provides a complete interface between a target system with a PowerPC™ 601 microprocessor and a variety of Hewlett-Packard logic analyzers. The configuration software for the PowerPC 601 processor sets up the format specification of the logic analyzer for compatibility with the PowerPC 601 processor. Since the Universal Interface board passively probes the PowerPC 601 processor, the UI-MPC601 can be used for timing analysis as well as state analysis. During state analysis the logic analyzer samples the PowerPC 601 processor signals on every rising edge of the PCLK signal and the logic analyzer sample rate equals the microprocessor clock rate. This state-per-clock capability is especially useful for hardware debugging and analysis.

Features

- Compatible with the PowerPC 601 microprocessor.
- Quick and easy connection of the logic analyzer pods to the target system.
- Low capacitance probing.
- Set-up and storage on built-in logic analyzer disk drive.
- Multi-layer, low noise PCB construction with ground and power planes.

Hardware Development Tools

- Trace data hard copy via RS-232 serial port.

Specifications

- *Signal Line Loading*—20 pF @100 Kohms.
- *Logic Analyzer Required*—Hewlett-Packard HP 1650, 16500, 1660, or 1670.
- *Maximum Acquisition Speed*—limited only by the speed of the PowerPC 601 microprocessor. The maximum speed of the logic analyzer is 100 MHz state and 500 MHz timing.
- *Supplied Equipment*—includes a universal interface module, configuration software and operating manual.

Technical Support

- Full-time product support staff, available to address technical questions and problems. Support via telephone, email, and fax.

Availability

- Available now.

Contact

PHOTO
(for location)
Corelis Inc.
not use k12607 Hidden Creek Way
Cerritos, CA 90703

Hardware Development Tools

Tel: (310) 926-6727
Fax: (310) 404-6196

Ireland

BIC Systems
Europa House
Harcourt St.
Dublin 2, Ireland

Tel: 353-14754-223
Fax: 353-14754-778

Sweden

Pelcon Electronics AB
Girovagen
S-175 06 Jarfalla
Sweden
Tel: 8-796-9870
Fax: 8-760-7685

Japan

Techno-Port Co. Ltd.
Nakagin Bldg. 10-2
Higashi-Shingashi 2-chome
Mianto-ku, Tokyo
Tel: 81-3-3434-3671
Fax: 81-3-3434-3897

Germany

Synatron
Technopark Neukeferich
Bretonischer Ring 13
D-85630 Grasbrunn
Tel: 89-460-2071
Fax: 89-460-5661

dli Personal Line Logic Analyzer Family

Analyzers

dli-digital logic instruments gmbh

The Personal Line (PL Series) Logic Analyzer Family is a set of flexible tools for development and debugging real-time applications using the PowerPC architecture. They feature up to 320 channels per mainframe, a memory depth up to 32K, external clock rate up to 100 MHz, and internal clock rate up to 1 GHz. A full range of triggering capability with interactive data stimulus allows the system to work as an ideal ATE system for your specific application. The system can be stand-alone or slaved to a PC running as an application under Microsoft Windows.

Capabilities include full time-correlated dual processor tracing (expandable to 16 processors), a software interface to control and operate the Personal Line from user-written programs, and a 10-nsec time stamp for time correlation of all buses (processors) being monitored.

Hardware Development Tools

Features

- 32 to 320 channels with external clock rate
- time-correlated clock sources.
- 32K memory depth with full channel count, 64K at half the channels.
- Internal clock rates up to 1 GHz for 72 channels or 144 channels with 500 MHz.
- High-impedance active logic probes for easy adaptation to PowerPC systems and minimum loading.
- 15-level high-speed trigger with physical trigger outputs to trigger external devices.
- Intelligent disassemblers for reverse assembly of PowerPC data not directly recorded from processor pins for cases in which adaptation to processor pins is impossible.
- Easy-to-use graphical user interface running under Microsoft Windows 3.1x and Windows 95.
- High-level language manager for debugging PowerPC systems at the source-code level.
- Software interface for user-written control and data display programs.
- Easy documentation through full compatibility with Windows programs such as WinWord.

Availability

- Available now.

Contact

of 100 MHz, configurable in 16-channel steps sharing either a single clock source

or two

dli-digital logic instruments gmbh

Voltastrasse 6
D-63128 Dietzenbach, Germany
Tel: (49) 6074 4002-0
Fax: (49) 6074 4002-77/24
Email: 100065.366@compuserve.com

Distributors

Austria

Walter Rekirsch-Elektronische
Geräte Ges.mbH & Co. Vertriebs-KG
Obachgasse 28
A-1220 Wien
Tel: (43) 1 2597270
Fax: (43) 1 2597275

Benelux

Tech5 B.V.
Rivierdijk 654
NL-3371 EE Hardinxveld-Giessendam
Tel: (31) 1846/15551
Fax: (31) 1846/15451

Denmark

StanTronic Instruments
Ormhojgardvej 16
DK-8700 Horsens
Tel: (45) 75 64 33 66
Fax: (45) 75 64 40 80

Great Britain

Reflex Technology Ltd.
9 Buckingham Place
Bellfield Road, High Wycombe
Bucks HP13 5HW
Tel: (44) 1494/465907
Fax: (44) 1494/465418

Finland

Caltest Oy
Karelantie 21
SF-00430 Helsinki
Tel: (358) 566/1166
Fax: (358) 566/2998

Ireland

Atron Electronics Ltd.
18 Sanyford Office Park
Sandyford, Dublin 18
Tel: (353) 1 2953000
Fax: (353) 1 2952870

Hardware Development Tools

Israel

DAN-EL Technologies Ltd.
9, Haruge Hamalchut St.
Tel-Aviv 69714

Italy

DELO Instruments
Via Piemonte 14

I-20090 Fizzonasco Pieve EM
Tel: (39) 2/907 22441
Fax: (39) 2/907 22742

Korea

B & P International Co. Ltd.
Geopyung Town A303, 203-1 Nonhyung
Kangnam-Ku, Seoul 135-010
Tel: 0082/2/546 1457
Fax: 0082/2/546 1458

Norway

Nortronicom a/s
Postboks 33 Manglerud
N-0612 Oslo
Tel: (47) 22 680910
Fax: (47) 22 681887

Spain

Eurocomercial, Informatica y Comunicaciones SA
Velazquez, 51
E-28001 Madrid

Sweden

Pronesto AB
Finlandsgatan 18, S-16406 Kista
Tel: (46) 86326570
Fax: (46)87514111

Switzerland

Computer Controls AG
Neubrunnenstr. 55
CH-8050 Zurich
Tel: (41) 1/3130616
Fax: (41) 1/3130622

USA

Ward/Davis Associates
2623 Manhattan Beach Blvd.
Redondo Beach, CA 90278
Tel: 1 (310) 643-6977
Fax: 1 (310) 643-6035

dli Professional Line High-Performance Logic Analyzer Family

Analyzers

dli-digital logic instruments gmbh

The Professional Line (proLine Series) Logic Analyzer Family is a set of flexible tools for development and debugging real-time applications using the PowerPC architecture. They feature up to 512 channels per mainframe, a memory depth up to 128 K transitional (optionally 2 M linear/transitional), external clock rate up to 180 MHz, and internal clock rate up to 720 MHz. A full range of 180 MHz high-speed triggering capability allows the system to work as an ideal test system for high speed and high performance digital circuits. The system is slaved to a PC running as an application under the popular MS Windows user interface.

Capabilities include full time-correlated dual processor tracing (expandable to 8 processors), a software interface to control and operate the Professional Line from user-written programs, and a 5-nsec time stamp for time correlation of all busses (processors) being monitored.

Hardware Development Tools

Features

- 64 to 512 channels with external clock rate
- time-correlated clock sources.
- 128 K transitional memory depth.
- Optional 2 M linear/transitional memory depth.
- Internal clock rates up to 720 MHz for 512 channels.
- High-impedance active logic probes for easy adaptation to PowerPC systems and minimum loading.
- Powerful 180 MHz high-speed trigger with physical trigger outputs to trigger external devices.
- High-speed real-time compare on the fly.
- Intelligent disassemblers for reverse assembly of PowerPC data not directly recorded from processor pins for cases in which adaptation to processor pins is impossible.
- Easy-to-use graphical user interface running under Microsoft Windows NT and Windows 95.
- High-level language manager for debugging PowerPC systems at source-code level.
- Software interface for user-written control and data display programs.
- Easy documentation through full compatibility with Windows programs such as WinWord.

Availability

- Available now.

of 180 MHz, configurable in 64-channel steps sharing either a single clock source

or two

Contact

dli-digital logic instruments gmbh

Voltastrasse 6
D-63128 Dietzenbach, Germany
Tel: (49) 6074 4002-0
Fax: (49) 6074 4002-77/24
Email: 100065.366@compuserve.com

Distributors

Austria
Walter Rekirsch-Elektronische
Geräte Ges.mbh & Co. Vertriebs-KG
Obachgasse 28
A-1220 Wien
Tel: (43) 1 2597270
Fax: (43) 1 2597275

Benelux
Tech5 B.V.
Rivierdijk 654
NL-3371 EE Hardinxveld-Giessendam
Tel: (31) 1846/15551
Fax: (31) 1846/15451

Denmark
StanTronic Instruments
Ormhojgardvej 16
DK-8700 Horsens
Tel: (45) 75 64 33 66
Fax: (45) 75 64 40 80

Great Britain
Reflex Technology Ltd.
9 Buckingham Place
Bellfield Road, High Wycombe
Bucks HP13 5HW
Tel: (44) 1494/465907
Fax: (44) 1494/465418

Finland
Caltest Oy
Karelantie 21
SF-00430 Helsinki
Tel: (358) 566/1166
Fax: (358) 566/2998

Ireland
Atron Electronics Ltd.
18 Sanyford Office Park

Hardware Development Tools

Sandyford, Dublin 18
Tel: (353) 1 2953000
Fax: (353) 1 2952870

Israel
DAN-EL Technologies Ltd.
9, Haruge Hamalchut St.
Tel-Aviv 69714

Italy
DELO Instruments
Via Piemonte 14
I-20090 Fizzonasco Pieve EM
Tel: (39) 2/907 22441
Fax: (39) 2/907 22742

Korea
B & P International Co. Ltd.
Geopyung Town A303, 203-1 Nonhyung
Kangnam-Ku, Seoul 135-010
Tel: 0082/2/546 1457
Fax: 0082/2/546 1458

Norway
Nortronicom a/s
Postboks 33 Manglerud
N-0612 Oslo
Tel: (47) 22 680910
Fax: (47) 22 681887

Spain
Eurocomercial, Informatica y Comunicaciones SA
Velazquez, 51
E-28001 Madrid

Sweden
Pronesto AB
Finlandsgatan 18, S-16406 Kista
Tel: (46) 86326570
Fax: (46)87514111

Switzerland
Computer Controls AG
Neubrunnenstr. 55
CH-8050 Zurich
Tel: (41) 1/3130616
Fax: (41) 1/3130622

USA
Ward/Davis Associates
2623 Manhattan Beach Blvd.
Redondo Beach, CA 90278
Tel: 1 (310) 643-6977
Fax: 1 (310) 643-6035

CLAS 4000 Logic Analyzer

Analyzer

Embedded Performance/Biomation

The CLAS 4000 Logic Analyzer provides measurement capability for examining high-speed CISC, RISC, ASIC, and general logic design, including PowerPC system design.

Operation is quick and simple—users click on the icon representing the PowerPC disassembler setup and the Logic Analyzer will be configured. The setup assigns channels to all of the processor's signals, arranges the channels into address, data, and status groups, and sets up the clocking for the PowerPC microprocessor. Predefined trigger patterns are also provided so that users can quickly specify which samples they want captured.

Hardware Development Tools

Users can view data captured on the Logic Analyzer in several windows simultaneously, with each window displaying the data in a different format. The Logic Analyzer displays results as symbolic, hex, decimal, octal, binary, and ASCII radices in a state window, as waveforms in a timing window, and as decoded mnemonics in a disassembly window.

Users can add or change display radices at any time without taking a new measurement. The Logic Analyzer displays decoded instructions for the PowerPC microprocessor in the disassembly window. Logic Analyzer probes are connected directly to the target system test points (provided by the user).

Features

- Timing and state measurements made through the same connection.
- Simultaneous display of state, timing, and disassembly.
- Users choose to display or delete unexecuted instructions.
- Finds and identifies all internal traps, and displays them as comments.
- Full-speed operation for clock and data rates.
- Supports multiple bus masters.
- 96-channel module with 50/100/200 MHz capture.

-
- Measure

ment widths of up to 384 channels.
Recording depths up to 4M samples.
 - Full windowing interface running under UNIX® or Macintosh® System 7 operating systems.
-

Hardware Development Tools

- Configure one to four Logic Analyzers.
- Full-speed triggering with multi-level Trace Control.
- Time-stamped transitional recording.
- Optional 1 GHz timing modules.

Specifications

- *Signals Monitored*—Two Pyramid Measurement Modules per CPU allow all 130 signals to be monitored and used in trigger patterns. Up to four Pyramid Modules may be installed in a CLAS 4000 chassis.
- *Input Impedance*—The input impedance of all signals is 1Mohm shunted by 8pF.
- *External Clock Sampling*—DC to 50MHz.
- *Setup Time Sampling*—7.0ns—typical (reduced to 4.0ns with Timebase Sync Probe)
- *Hold Time Sampling*—0ns.
- *Internal Clock Sampling*—100ms to 5ns.

Warranty

All Biomation products are warranted against defects in materials and workmanship for a period of one year from date of delivery.

Ordering information

- A71051 PowerPC Microprocessor Analysis Package.

Availability

- Available now.

Contact

Embedded Performance/Biomation

1860 Barber Lane
Milpitas, CA 95035
Tel: (800) 934-2466
Tel: (408) 434-2210
Fax: (408) 435-7970

Synthesizable and Simulation Models for PowerPC Bus Interface

Simulation Models

Eureka Technology, Inc.

The PowerPC bus interface models and simulation models from Eureka Technology greatly simplify the design of any PowerPC-based system. Eureka Technology offers several stand-alone interface models: bus master, bus slave, bus arbiter, cache controller and DRAM controller. These models are available in Verilog and VHDL, and they can be synthesized to any ASIC or FPGA technologies through logic synthesis.

All models support the advanced features of the PowerPC host bus such as pipeline supports, independent address and data bus tenure, and address retry. All models can also be customized to support specialized customer-specific features.

Eureka Technology also offers bus simulation models such as bus master and bus slave to simplify system-level simulation of PowerPC-based systems. These simulation models function as bus exercisers to test the entire system during functional simulation. The bus master model generates bus requests based on user input to simulate different bus transactions. The slave simulation model

Hardware Development Tools

Features

- Supports PowerPC 60x microprocessors and related microcontrollers.
- Designed for ASIC and FPGA logic synthesis.
- Independent address bus and data bus tenure.
- Two simultaneous outstanding bus accesses.

Bus Master

- Automatic bus request generation.
- Supports zero wait-state data transfer.
- Single and burst data access.
- Supports transaction termination due to address retry and data transfer error.
- Efficient and easy-to-use internal interface.

Bus Slave

- Supports address pipeline.
- Single and burst data access.
- Supports address retry and termination due to data error.
- Direct support for SRAM and EPROM devices.
- Fast asynchronous SRAM access.
- Support second-level system cache.

Arbiter

- Address bus and data bus arbitration.
- Fast bus grant and bus parking.
- Rotating or fixed priority schemes.
- Flexible number of masters supported.

Cache Controller

- Fast look-aside second-level cache.
- Unrestricted cache size.
- Zero wait-state burst access.
- Pipeline burst or flow-through burst SRAM support.
- High-performance with address pipeline.
- Low-cost external memory devices for tag and data.

DRAM Controller

- EDO and fast page-mode DRAMs.
- Multiple memory banks.
- External cache system support.

Simulation Models

- User specific transaction requests.
- Programmable transaction controls such as data size, transfer type, cache support.
- Address pipeline.
- Programmable wait-state generation.
- Simulates address retry and data transfer error.
- Second-level cache support.

Availability

- Available now.

Contact

Eureka Technology, Inc.
4962 El Camino Real, #108
Los Altos, CA 94022
Tel: (415) 960-3800
Email: info@eurekatech.com

HP 16500 Series Modular Logic Analysis System

Analyzer, Debugger

Hewlett-Packard Company

The Hewlett-Packard 16500 Series Modular Logic Analysis System can capture real-time interaction between PowerPC system hardware and software. The system helps determine the cause of defects and includes several measurement modules for debugging problems. The system has been tuned for software debugging and has a user interface that helps users learn the system quickly and easily.

Features

- 102 channels of synchronous analysis at 100 MHz, and 68 to 204 channels at 110 MHz.
- 204 channels can share a single timebase, and over 1000 channels can fit into a system.
- Asynchronous sampling mode that runs at up to 500 MHz, useful in detecting timing problems across multiple buses.
- Up to 1 Mb of memory per channel.
- Full-featured digitizing oscilloscope samples at 1 Gsample/s to aid in diagnosing digital problems, which at high speed, are often the result of analog effects.
- Intermodule bus (IMB) for triggering other measurement modules in connection with a module where the symptom appears. Helpful when the symptom is known, but not the underlying problem.
- Inverse assemblers to filter measurement data; for example, the software developer can filter out unexecuted code or show only jumps or subroutine calls.
- Automatic symbol readers and an 540 MB hard disk, which can be used for symbol storage, to aid in symbolic debugging.

- Networking support for Ethernet with TCP/IP and NFS, allowing designers to move measurement data from the logic analysis system to their computer system through a copy command. The system is fully programmable over Ethernet or other standard buses (RS-232-C and HPIB).
- Presentation of listing data in an ASCII format and waveform data in TIFF format. Real-time date and time stamps on listings.
- Easy-to-learn, easy-to-remember, consistent user interface, supported by a training manual and training board that help get users up and running quickly.
- Touch screen that provides quick access to any field on the screen; users have the option of disabling the touch screen and using a mouse and/or keyboard.

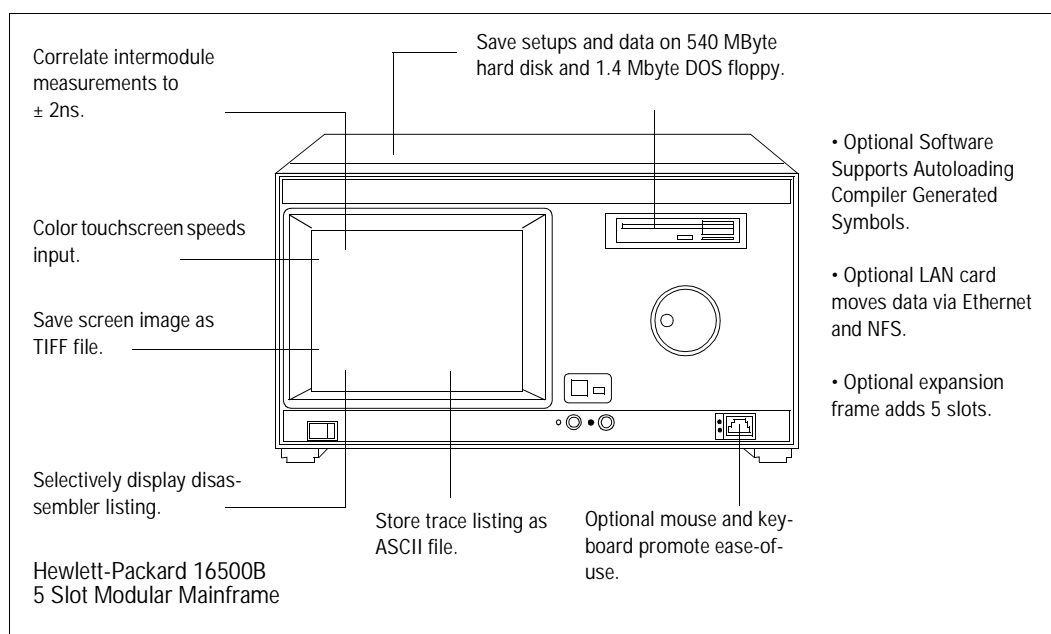
Ordering Information

- HP 16500B Five -Slot Logic Mainframe Analysis System.
- HP 16500 H Ethernet interface module.
- HP 16550A 102-Channel, 100 MHz State and 500 MHz Timing Module.
- HP 16554A, 70 MHz State and 250 MHz Time Module.
- HP 16555A 68-Channel, 1 Mb/Channel, 110 MHz State and 500 MHz Timing Module.
- HP 16556A, 100 MHz State and 400 MHz Timing Module.
- HP 16517A 16-Channel, 4-GSa/s Timing and 800 MSa/s Synchronous State Module.
- HP 16534A 2-Channel, 2 GSa/s Oscilloscope Module.
- HP 16522A 40-Channel, 200 MVector/s, 258,048 depth, 50Mb/s Pattern Generator Module.

Hardware Development Tools

Availability

- Available now.



Contact

Hewlett-Packard Company

Test & Measurement
Mail Stop 51LSJ
PO Box 58 199
Santa Clara, CA 95052-9952
Web: <http://www.hp.com>

International Offices

Austria, Tel: 43 (0222) 2500-0
Belgium/Luxembourg, Tel: 32 (02) 778 31 11
Denmark, Tel: 45 (45) 99 10 00
France, Tel: 33 (1) 69.82.65.00
Germany, Tel: 49 (06172) 16 0
Italy, Tel: 39 (02) 92 122 241
Netherlands, Tel: 31 (020) 547 6669
Norway, Tel: 47 (67) 159 700
Spain, 34 900 123 123
Sweden, 46 (08) 750 20 00
Switzerland, Tel: 41 (057) 31 21 11

HP 16505A Prototype Analyzer

Analyzer

Hewlett-Packard Company

The HP 16505A Prototype Analyzer and HP 16500 Modular Logic Analysis System combination allows you to capture and analyze real-time data from your PowerPC-based system. Your time-to-insight into critical system problems is accelerated by a complete overview of your system's functionality and performance provided through a variety of measurement functions incorporated into the HP 16505A/16500C system.

Track tough system integration problems to root cause by viewing data in domains ranging from source code view to signal integrity view. Team members can see fully time-correlated measured data in the form most suited to their disciplines.

View activity on both the PowerPC bus and other system buses, such as PCI, simultaneously, using the HP 16505A Prototype Analyzer's visual measurements environment. Make time-correlated measurements across both buses and filter the bus activity to reduce megabytes of captured data into just the information you need to see.

The HP 16505A Prototype Analyzer is an analysis and display processor for the HP 16500 modular logic analysis system. The Prototype Analyzer provides multiple windowed views of data and powerful data post-processing using a visual measurements paradigm. You can rapidly set up and tear down measurements as you determine the nature of the problem. You can control and view data, and perform post-processing analysis from the prototype analyzer's windows interface.

Central to the HP 16500C Logic Analysis System is the HP 16500C mainframe that supports up to 5 independent measurement modules. An optional expansion frame

supports an additional 5 modules. Refer to the HP 16500C Modular Logic Analysis System datasheet in this catalog for measurement module information.

Hardware Development Tools

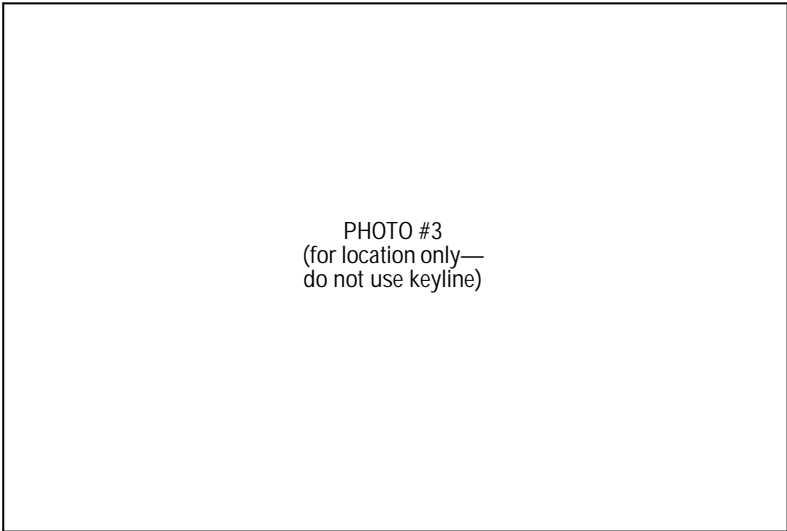


PHOTO #3
(for location only—
do not use keyline)

Features

- See the processor instruction flow of interest to you; filter out unused prefetches using flexible inverse assembly filters available for popular processors.
- Trace your system activity across multiple domains simultaneously using the multiple windows of the HP 16505A.
- Debug your system using symbolics generated directly from your source code using a symbol utility reader, standard with the HP 16505A. The optional B4620A Software Analyzer tool set provides real-time correlation between a microprocessor execution trace and the corresponding high-level source code.
- View and control the HP 16505A/16500C

Contact

Hewlett-Packard Company

Test & Measurement
Mail Stop 51LSJ
PO Box 58199
Santa Clara, CA 95052-9952
Web: <http://www.hp.com>

International Offices

Austria, Tel: 43 (0222) 2500-0
Belgium/Luxembourg, Tel: 32 (02) 778 31 11
Denmark, Tel: 45 (45) 99 10 00
France, Tel: 33 (1) 69.82.65.00
Germany, Tel: 49 (06172) 16 0
Italy, Tel: 39 (02) 92 122 241
Netherlands, Tel: 31 (020) 547 6669
Norway, Tel: 47 (67) 159 700
Spain, 34 900 123 123
Sweden, 46 (08) 750 20 00
Switzerland, Tel: 41 (057) 31 21 11
UK, Tel: 44 (0344) 362 367

HP E2449B Inverse Assembler

Analyzer Interface, Disassembler, Real-Time Tool

Hewlett-Packard Company

The HP E2449B Inverse Assembler configures the Hewlett-Packard 16550A, 16554A, 16555A, 16556A, 1660C/CS and 1670A Logic Analysis Systems for the analysis of systems based on the PowerPC 601 microprocessor. The Inverse Assembler labels address, data, and status lines. When a state trace is displayed, the data is disassembled and listed in PowerPC 601, 603, or 403GA mnemonics.

The HP E2449B operates in several modes:

- *State-per-address or data-cycle mode*—The Logic Analyzer records only those states in which one or more of the strobes (AACK, ARTRY, TA, DRTRY, TEA) are asserted. This mode filters wait states and exposes the PowerPC 601's decoupled address and data buses.
- *State-per-clock mode*—Address, data, and status are captured on each CPU clock. This mode is useful in hardware validation and when debugging system crashes.
- *Timing-analysis mode*—All active signals are sampled every 4 ns. This mode is used when accurate timing measurements are needed.

Features

- Real-time debug of PowerPC 601 systems.
- Compatible with PowerPC 601, 603 and 403GA processors and processor evaluation boards.
- Full mnemonic disassembly of processor instructions.
- Queue flush instructions identified and marked for all bus sizes.
- Prefetched instructions that are not executed are marked in the state listing.
- Disassembly is synchronized at branch addresses.

Specifications

- Both the 50- and 66-MHz versions of the PowerPC 601 processor are supported at full speed. Contact your HP sales representative for current information on support of later versions.
- Input capacitance is approximately 8 pF.

Hardware Development Tools

HP Logic Analyzers Supported

- HP 16550A, 16554A, 16555A, 16556A, 1660C/CS and 1670A.
- Eight, 16-channel probes are required for complete state disassembly. An additional two probes can monitor the remainder of the signal pins for timing measurements. One termination adapter is required for each logic analyzer probe if the probes are not terminated on the user's target system.

Technical Support

- Local applications engineers.

Availability

- Available now.

Contact

Hewlett-Packard Company

Test & Measurement
Mail Stop 51LSJ
PO Box 58199
Santa Clara, CA 95052-9952
Web: <http://www.hp.com>

International Offices

Austria, Tel: 43 (0222) 2500-0
Belgium/Luxembourg, Tel: 32 (02) 778 31 11
Denmark, Tel: 45 (45) 99 10 00
France, Tel: 33 (1) 69.82.65.00
Germany, Tel: 49 (06172) 16 0
Italy, Tel: 39 (02) 92 122 241
Netherlands, Tel: 31 (020) 547 6669
Norway, Tel: 47 (67) 159 700
Spain, 34 900 123 123
Sweden, 46 (08) 750 20 00
Switzerland, Tel: 41 (057) 31 21 11
UK, Tel: 44 (0344) 362 367

HP E2455A Preprocessor Interface for the PowerPC 603 and 603e Microprocessors

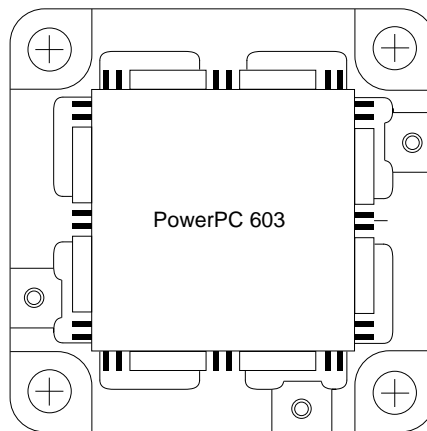
Analyzer Interface

Hewlett-Packard Company

The HP E2455A preprocessor interface for the PowerPC 603 or 603e microprocessor allows you to easily connect an HP 16550A, HP 16554A, HP 16555A, HP 16556A, HP 1660C/CS or HP 1670A logic analyzer to your target system. Configuration software is provided with preprocessor labels, addresses, data, and status lines. When a state trace is displayed, instructions are disassembled and listed in PowerPC 603 mnemonics.

The HP E2455A operates in several modes:

- *State-per-address or data-cycle mode*—The logic analyzer records only those states in which one or more of the strobes (AACK, ARTY, TA, DRTRY, TEA) are asserted. This mode filters wait states and exposes the PowerPC 603/603e microprocessor's decoupled address and data buses.
- *State-per-clock mode*—Address, data, and status are captured on each CPU clock. This mode is useful in hardware validation and debugging of system crashes.
- *Timing-analysis mode*—All active signals are sampled every 4 ns. This mode is used to obtain accurate timing measurements.



Preprocessor locator base shown with PowerPC 603 package

Hardware Development Tools

Features

- Real-time debug of PowerPC 603 systems.
- Compatible with PowerPC 603/603e processor packages.
- Full mnemonic disassembly of the processor instruction set.

Specifications

- Up to 66-MHz versions of the PowerPC 603 processors are supported at full speed. Contact an HP sales representative for current information on support of other versions.
- Component keep-out area: preprocessor locator base footprint; a square, 1.753 in (44.53 mm) on a side, centered on PowerPC 603 or 603e package.
- Preprocessor mounting holes (optional): four 0.147 in +.003/-0 in diameter holes through printed circuit board at corners of a square, 1.458 in (37.04 mm) on a side, centered on PowerPC 603 or 603e package.

HP Logic Analyzers Supported

- HP 16550A, HP 16554A, HP 16555A, HP 16556A, HP 1660C/CS and HP 1670A.
- Eight, 16-channel probes are required for complete state disassembly. Additional two probes can monitor the remainder of the signal pins for timing measurements.

Technical Support

- Local applications engineers.

Availability

- Available now.

Contact

Hewlett-Packard Company

Test & Measurement
Mail Stop 51LSJ
PO Box 58199
Santa Clara, CA 95052-9952
Web: <http://www.hp.com>

International Offices

Austria, Tel: 43 (0222) 2500-0
Belgium/Luxembourg, Tel: 32 (02) 778 31 11
Denmark, Tel: 45 (45) 99 10 00
France, Tel: 33 (1) 69.82.65.00
Germany, Tel: 49 (06172) 16 0
Italy, Tel: 39 (02) 92 122 241
Netherlands, Tel: 31 (020) 547 6669
Norway, Tel: 47 (67) 159 700
Spain, 34 900 123 123
Sweden, 46 (08) 750 20 00
Switzerland, Tel: 41 (057) 31 21 11
UK, Tel: 44 (0344) 362 367

HP E2468A Preprocessor for PowerPC 403GA and 403GC Embedded Controllers

Analyzer Interface

Hewlett-Packard Company

The Hewlett-Packard E2468A preprocessor interface provides an easy way to connect a Hewlett-Packard logic analyzer to a target system using the IBM PowerPC 403GA or 403GC microprocessor. All necessary clocks are passed through by the preprocessor to the logic analyzer, ensuring that data is captured at the correct time.

Software is shipped with the product that automatically configures the logic analyzer, generating labels for address, data, and status signals. Included with the software is a disassembler which displays execution traces in PowerPC 403GA/GC microprocessor mnemonics. Instructions which are pre-fetched, but not executed, are marked in the trace display. Three modes of operation are available to the user: state-per-clock, which provides a complete display of all bus activity; state-per-transfer, which filters out wait and idle states; and timing analysis up to 500 MHz. Channel-to-channel skew is 1 ns.

Inverse Assembler Features

All processor instructions are supported. In addition, disassembly is synchronized at branch addresses.

- *State per address or data cycle*—The logic analyzer records only those states in which the strobe (IOTV, TS6) is asserted. This mode filters wait and idle states.
- *State per clock mode*—Address and data are captured on each CPU clock. This feature is useful in hardware validation and debugging of system crashes.
- *Timing mode*—All address, data and status lines are labeled on the logic analyzer display when making accurate timing measurements.

Logic Analyzers Supported

HP 16550A (1 required); HP 16554A, HP 16555A, HP 16556A: (2 required); HP 1660C/CS, 1670A

Number of Probes Required

Five, sixteen-channel probes are required for complete state disassembly. An additional three probes will monitor the remainder of the signal pins for timing measurements.

- *Target Signal Timing*: Data must be valid for a 3.5 ns window with respect to the logic analyzer clock, which strobes the data into the logic analyzer on the rising edge.
- *Termination required*: no user-supplied termination is necessary because the logic analyzer probes are terminated on the preprocessor.
- *Evaluation Board compatibility*: The IBM Microelectronics' PowerPC 403GA/GC Evaluation Board, which includes 20-pin termination headers for an HP logic analyzer, is supported by the 403GA/GC configuration file of the HP E2468A. Note: HP E2449B, a software-only product, is also available for this application.

Processor Supported

IBM PowerPC 403GA or 403GC embedded controller in a 160-pin PQFP package up to 50 MHz. Note: HP E5335A PQFP adapter is required to probe the 160-pin PQFP package.

Signal Line Loading

- 10 pF and 100 kohms on all signals.

Technical Support

- Local applications engineers.

Hardware Development Tools

Availability

- Available now.

Contact

Hewlett-Packard Company

Test & Measurement
Mail Stop 51LSJ
PO Box 58199
Santa Clara, CA 95052-9952
Web: <http://www.hp.com>

International Offices

Austria, Tel: 43 (0222) 2500-0
Belgium/Luxembourg, Tel: 32 (02) 778 31 11
Denmark, Tel: 45 (45) 99 10 00
France, Tel: 33 (1) 69.82.65.00
Germany, Tel: 49 (06172) 16 0
Italy, Tel: 39 (02) 92 122 241
Netherlands, Tel: 31 (020) 547 6669
Norway, Tel: 47 (67) 159 700
Spain, 34 900 123 123
Sweden, 46 (08) 750 20 00
Switzerland, Tel: 41 (057) 31 21 11
UK, Tel: 44 (0344) 362 367

HP E2465A Preprocessor Interface

Analyzer Interface, Disassembler

Hewlett-Packard Company

The HP E2465A preprocessor interface for the PowerPC 604 microprocessor allows you to easily connect the HP 16550A, 16554A, 16555A/D, 16556A/D, 1660C/CS, or 1670A logic analyzer to your target system. Configuration software is provided to set up the logic analyzer for compatibility with the preprocessor interface. An inverse assembler is included that enables you to obtain displays of the microprocessor operations in PowerPC 604 mnemonics.

The HP E2465A preprocessor interface has a Pin Grid Array (PGA) pattern connector. You remove the PowerPC 604 chip from the target system and plug it into the socket on the preprocessor interface. Then you plug the preprocessor interface into the target's PGA socket.

Features

- Real-time debug of PowerPC 604 microprocessor systems.
- Full mnemonic disassembly of the PowerPC 604 microprocessor instruction set.
- 289 pin PGA package probing.
- Supports normal, Fast-L2, and direct store modes.

Data Sampling Modes

- *State-per-ack mode*—The logic analyzer uses trigger sequencer store qualifications to capture only address and data acknowledge cycles. The logic analyzer records only those states in which one or more of the strobes (AACK, ARTRY, TA, TS, DRTRY) are asserted. This mode happens to be the default set by the configuration files. It provides the greatest information density in the logic analyzer acquisition memory.
- *State-per-clock mode*—Every clock cycle is captured by the logic analyzer, including idle and wait states between and during tenures. Address, data, and status are captured on each CPU clock. This mode is useful in hardware validation and when debugging system crashes.
- *Timing-analysis mode*—The logic analyzer samples the microprocessor pins asynchronously, typically with 4 ns resolution. This mode is used when accurate timing measurements are needed.

Hardware Development Tools

Inverse Assemble Features

- Address and data alignment.
- Disassembly synchronization at branch address.
- General purpose, floating point, condition, and special purpose registers are displayed.
- Full PowerPC 604 instruction set decode.
- Support of extended mnemonics like conditional traps, add-immediate, subtract-from, and rotate-left, among others.

HP Logic Analyzers Supported

- HP 16550B, 16554A, 16555A/D, 16556A/D, 1660C/CS and 1670A.
- Eight 16-channel probes are required for complete state disassembly. Three additional probes can monitor the remainder of the signal pins for timing measurements.

Specifications

- Compatible with PowerPC 604 PGA microprocessor packages.
- Supports PowerPC 604 microprocessor clock speeds up to 66 MHz.
- Full mnemonic disassembly of the processor instruction set.

Equipment Supplied

- E2465A preprocessor interface.
- Configuration and inverse assemble software.
- User's Guide.
- Pin protector.

JTAG Connector

The E2465A has a JTAG connector on board for easy connection to the PowerPC 604 processor's JTAG port. This connector can be used to hook up a run control tool like HP's Processor Probe.

Technical Support

- Local application engineers.

Availability

- Available now.

Contact

Hewlett-Packard Company

Test & Measurement
Mail Stop 51LSJ
PO Box 58199
Santa Clara, CA 95052-9952
Web: <http://www.hp.com>

International Offices

Austria, Tel: 43 (0222) 2500-0
Belgium/Luxembourg, Tel: 32 (02) 778 31 11
Denmark, Tel: 45 (45) 99 10 00
France, Tel: 33 (1) 69.82.65.00
Germany, Tel: 49 (06172) 16 0
Italy, Tel: 39 (02) 92 122 241
Netherlands, Tel: 31 (020) 547 6669
Norway, Tel: 47 (67) 159 700
Spain, 34 900 123 123
Sweden, 46 (08) 750 20 00
Switzerland, Tel: 41 (057) 31 21 11
UK, Tel: 44 (0344) 362 367

HP E3494A and HP E3477A Processor Probes

Debuggers

Hewlett-Packard Company

The HP E3494A and E3477A Processor Probes are primarily hardware products that provide in-circuit software debugging of embedded PowerPC 603 and 603e targets, respectively. The Processor Probe utilizes the debug capability built into the PowerPC 603/603e silicon to perform debug functions. More specifically, it provides code downloading, setting breakpoints, and access to memory or register display modification. You can control program execution through single stepping, start/stop, run/break, set/modify breakpoints, or run code a full speed in target.

The Processor Probe is controlled over RS232 or your local area network and is connected to your target through a dedicated 16-pin connector. The Processor Probe is designed specifically for code developers who are creating software for the PowerPC 603 or 603e microprocessors in an embedded target. It understands the processors' instruction set mnemonics and unique registers. Unlike in-circuit emulators, the Processor Probe only accesses the debug pins, affecting no other user signals and ensuring stable operation. Probing through a connector reduces physical connection problems.

Interfaces

The user can control the processor probe through a high-level language debugger from one of Hewlett-Packard's Third Party Software Vendors. By using a high-level language debugger, you can modify variables using C expressions, control the Processor Probe from the familiar context of your source code and symbolically modify memory locations. In addition, you can set a breakpoint simply by pointing to a source line and clicking a mouse button.

Debugger Connection

The E3494A and E3477A can be controlled by a third-party source-level debugger to provide a high-level language view of software debugging. Through use of a debugger from Green Hills Software or Software Development Systems (SDS), you can view source code, set breakpoints, single step, examine variables, and modify source-code variables.

HP evaluates and validates third-party source-level debuggers. HP provides technical assistance to our partners and validates the end-result to ensure that the debugger communicates correctly with the processor probe. HP has an aggressive third-party program where new vendors are being added continually. You are encouraged to contact HP for the availability of the most recent third-party debuggers.

Integrated with HP's Analysis Tools

Through the use of the Processor Probe's BNC connector, it can trigger or be triggered by other HP development tools. Used in conjunction with the HP 16500C (with 1655xA/D modules), 1660C/CS or 1670A logic analyzer, the probe can be used to execute a test program. The analyzer can detect an event and cause the probe to stop the target.

The logic analyzer can trace external bus activities such as memory or I/O accesses, and measure timing waveforms. The E3450A Distributed Emulator bundle for the PowerPC 603 processor is recommended for a more robust, coordinated solution that provides logic analysis and timing measurements as well as run control. The E3450A bundle is a convenient method of ordering an emulator-level solution. The bundle includes the

Hardware Development Tools

E3494A Processor Probe, a 1670A logic analyzer, an E2455A Preprocessor, and B3740A Software Analyzer software. The PowerPC 603e bundle (E3451A) is also available. The E3451A contains the same components as the E3450A, except the E3494A Processor Probe is replaced with the PowerPC 603e Processor Probe (E3477A).

A Hewlett-Packard Logic Analyzer may be connected to the PPC603/603e 240 pin QFP SMT package with an optional HP E2455A Preprocessor Interface. The HP E2455A requires the target system to have a minimum of 6 mm clearance around the outside of the processor pins.

Specifications

- *Physical connections:*
 - Ethernet—10baseT.
 - RS-232—1200-115200 Kbaud rates supported.
- *Number of breakpoints:*
 - Virtually unlimited software breakpoints, or
 - One hardware breakpoint.
- *Physical size*—155 mm width x 161 mm depth x 65 mm height.

Technical Support

- Local applications engineers.

Availability

- Available now.

Contact

Hewlett-Packard Company

Test & Measurement
Mail Stop 51LSJ
PO Box 58199
Santa Clara, CA 95052-9952
Web: <http://www.hp.com>

International Offices

Austria, Tel: 43 (0222) 2500-0
Belgium/Luxembourg, Tel: 32 (02) 778 31 11
Denmark, Tel: 45 (45) 99 10 00
France, Tel: 33 (1) 69.82.65.00
Germany, Tel: 49 (06172) 16 0
Italy, Tel: 39 (02) 92 122 241
Netherlands, Tel: 31 (020) 547 6669
Norway, Tel: 47 (67) 159 700
Spain, 34 900 123 123
Sweden, 46 (08) 750 20 00
Switzerland, Tel: 41 (057) 31 21 11
UK, Tel: 44 (0344) 362 367

SmartModel® Library and Hardware Modeling Systems

Libraries, Simulation Models

Logic Modeling®

Logic Modeling's comprehensive solution to your simulation model needs includes the industry-standard LM-family™ and ModelSource™ hardware modeling products, the SmartModel library of behavioral models, and the VHDL SourceModel™ Libraries.

Both the LM-family and ModelSource hardware modeling systems and the SmartModel Library support the simulation of designs based on the PowerPC 600 series and PowerPC 403 processors on every major commercially available simulator. Both products are fully interoperable in VHDL simulation environments.

SmartModel Library

The SmartModel Library contains both FoundryModel support and/or Hardware Verification model support for several of the devices in the PowerPC Family.

The FoundryModel provides the full range of the device function including all instructions and cycles, interrupts, and I/O capabilities and is useful for the development of diagnostics software, an operating system kernel, or device driver software. These FoundryModels are only supported on the IBM RS6000, Sun and HP workstation platforms.

The Hardware Verification model is an easy-to-use, high speed model designed to verify the functionality of microprocessor-based systems by simulating the processor's bus cycles.

LM-family and ModelSource Hardware Modeling Systems

The LM-family and ModelSource modeling products use the actual device to represent the device's behavior during simulation, thereby ensuring simulation model accuracy and increased model performance. Ready-to-use hardware models are available for over 650 complex VLSI devices. Each hardware model includes the device on an adapter ready for mounting in LM-family or ModelSource systems, shell software to provide initialization and timing information, and a complete set of test vectors to ensure model functionality. Optional ModelTools™ software and blank device adapters allow you to create your own hardware models of standard devices or ASICs.

Hardware Development Tools

Simulators Supported

- AT&T.
- Cadence Design Systems.
- Chronologic Simulation.
- Intergraph.
- FrontLine.
- IBM.
- IKOS Systems.
- Mentor Graphics.
- Model Technology.
- Nextwave.
- Summit Design (SML only).
- Synopsys.
- Teradyne (HWM only).
- Vantage.
- VEDA Design.
- Viewlogic Systems.
- Zuken (SML only).
- Zycad Corporation (HWM only).

Hosts Supported

- IBM RISC System/6000 workstation.
- Sun SPARC 4.
- Sun SPARC 5 (Solaris 2.X).
- HP 9000 Series 700.
- DEC 3000 Model 600.
- NEC EWS4800 Series (RISC) (HWM only).
- Sony NEWS (SML only).

Technical Support

- Local offices provide on-site assistance.
- Customer support hotline.
- Bulletin board service.
- Training Classes.
- Consulting Services.

Availability

- Available now.

Contact

Synopsys, Inc.
Logic Modeling Products
19500 N.W. Gibbs Drive
Beaverton, OR 97006
Tel: 503-690-6900
Fax: 503-690-6906
Email: modelinfo@synopsys.com

Europe
Stefan-George-Ring 6
D-81929 Munich
Germany
Tel: 49-89-99-39-12-30
Fax: 49-89-99-39-12-32

Asia Pacific
#31-02 The Concourse
300 Beach Road
Singapore 199555
Tel: 65-296-7433
Fax: 65-297-1272

Signal Integrity Analysis Tools for High-Speed Designs

Libraries

Quad Design Technology

Over the past decade, very large-scale integration technology has resulted in the creation of ICs and PCBs with faster clock speeds and greater functional complexity. These higher speeds have made timing behavior a determining factor in overall system operation while simultaneously increasing the likelihood of timing-related problems.

In response to this dilemma, Quad Design has an innovative family of tools created specifically to resolve the timing errors associated with advanced digital designs—from ASICs to multiboard and backplane systems. Our software, which includes PDQ, TLC, XTK and PowerPC buffer models can be used independently or together to correct errors while your design is still a vision.

Knowing all timing and signal integrity errors before they occur ensures a successful first build, which reduces redesign costs and dramatically increases engineering productivity.

Features

- *Pre-Route Delay Quantifier*—Analyzes all signal paths before routing. Another industry first, PDQ (Pre-route Delay Quantifier) evaluates and specifies component placement strategies from a signal delay perspective. In addition to quantifying signal interconnect delays, PDQ automatically determines the optimal signal delay paths between components for minimizing such delays and maximizing system performance.
- *Transmission Line Calculator*—Simulates all transmission line effects before prototyping. An advanced system simulation tool, TLC (Transmission Line Calculator) simulates lossless transmission line effects on system timing and signal quality for a single circuit net or a complete digital system. TLC can be used to analyze wire wrap, coaxial cable and ribbon cable layouts in addition to PCB traces. As with Quad Design's other system simulation tools, TLC ensures fewer design iterations, improved time to market and higher quality designs.
- *Crosstalk Tool Kit*—Predicts all signal distortion effects before they occur. The Crosstalk Tool Kit (XTK) is a suite of tools that simulates lossy coupled transmission lines and predicts the effects of signal distortions on the performance of ICs and PCBs. XTK takes into account signal coupling, skin effect, and ohmic and dielectric losses. XTK also performs both a timing and system-level signal quality analysis for multiboard and backplane designs, calculates and simulates parasitic parameters associated with PCBs or multi-chip modules (MCMs) operating at ultra-high frequencies, and pinpoints signal-integrity problems arising from increased use of fine-line wiring and MCMs to pack more components into less board space.

Hardware Development Tools

Hosts Supported

Major UNIX/X Windows platforms, including those from Sun, HP, MIPS and IBM. For information on specific platform and operating system support, contact Quad Design.

Availability

- Available now.

Quad Design Technology

1385 Del Norte Road
Camarillo, CA 93010
Tel: (805) 988-8250
Fax: (805) 988-8259
Web: <http://www.quaddesign.com>

Contact

PowerPC 601 VHDL Model

Simulation Model

Sand Microelectronics, Inc.

Sand Microelectronics provides a comprehensive set of models designed to meet the simulation requirements of system designers. The PowerPC 601 VHDL Model is included in this offering. It is available in source code format and is fully interoperable in VHDL environments.

The PowerPC 601 VHDL Model is a behavioral model which simulates the bus-cycle protocols of the PowerPC 601 microprocessor. The model is used primarily to exercise and debug the design of components or systems based on the PowerPC 601 microprocessor. The objective of the model is to aid in the functional verification process and to minimize functional design errors prior to silicon tapeout.

The model provides full system-level simulation and debug capability. Data comparators flag any data errors when memory or I/O reads mismatch with expected data. The model can be instantiated more than once to assist in the simulation and verification of multi-processor environments. The model provides a convenient command-file interface to specify the bus-cycle commands.

Because of the PowerPC microprocessor's independent address and data tenures, two built-in ROMs are provided which can be pre-loaded with instructions and data. A high-level command language is provided for instruction coding.

Features

- VHDL source code model.
- Convenient command-file user interface.
- Accurate bus timing and protocol:
 - Supports 50/66 MHz timing.
 - Incorporates timing checks.
- Supports multiple instantiation for multi-processor.
- Supports the following cycles:
 - Memory Read.
 - Memory Write.
 - Memory Burst Read.
 - Memory Burst Write.
 - I/O Read.
 - I/O Write.
 - Inquire, Snoop Hit/Miss, Invalidate.
- 1 Kbyte first-level cache.
- Test bench.

Hardware Development Tools

Simulators Supported

- Viewlogic®
- Synopsys®

Hosts Supported

- Sun 3
- Sun 4

Technical Support

- Customer support option.
- Consulting services available to customize model.

Availability

- Available now.

Contact

Sand Microelectronics, Inc.

Attn: Anand Naidu
3350 Scott Boulevard, #24
Santa Clara, CA 95054
Tel: (408) 235-8600
Fax: (408) 235-8601
Email: sales@sandmicro.com
Web: <http://www.sandmicro.com>

3000 Series Logic Analyzers

Analyzers, Debuggers

Tektronix, Inc.

The 3000 series Logic Analyzers are general-purpose instruments for design applications. This series includes the 3001 monolithic unit and the 3002 modular mainframe. Both units offer a 127 MB hard disk and an MS-DOS compatible floppy disk drive for data storage, a keyboard, and a variety of monochrome and color displays. The 3000 series offers 80-160 channels of 80 MHz state acquisition, 200 MHz transitional timing analysis on all channels, 16-32 channels of 1 GHz timing acquisition (32K deep), true simultaneous state and timing analysis without double-probing, ROM emulation, real-time performance analysis, and links to high-level languages such as C, C++, Pascal and Ada.

Features

- Real-time symbolic debug and performance analysis of PowerPC systems.
- Powerful triggering to quickly determine the root cause of the problem.
- 1 ns timing resolution with 32K of memory depth to capture intermittent problems.
- 80-160 channels of simultaneous state and timing acquisition through the same probe. Double-probing is not required.
- Label your traces for efficient data viewing.
- Links to high-level languages such as C, C++, Pascal and ADA.

Hardware Development Tools

Microprocessors Supported

- All available PowerPC microprocessors.

Availability

- Available now.

Technical Support

- Local application engineers.
- Technical support hotline.

Contact

Tektronix, Inc.

P.O. Box 4600
Mail Station 94-860
Beaverton, OR 97076-4600
Tel: (800) 426-2200 ext 316
Tel: (503) 682-3411 ext 316
Fax: (503) 690-3959
Web: <http://www.tek.com/Masurement/Products/>

Europe

Tel: 44 (0628) 486000
Fax: 44 (0628) 47 4799

Japan

Tel: 81 (3) 3448-4611
Fax: 81 (3) 3444-0318

Asia

Tel: 852 2585 6688
Fax: 852 2511 3459

TLA500, DAS/NT and DAS/XP

Analyzers, Debuggers

Tektronix, Inc.

The TLA500, DAS/NT and DAS/XP analyzers and PowerPC support products provide a simple connection to your PowerPC target systems for real-time monitoring of instruction execution and bus timing. Trace data is first analyzed to show actual execution and branch behavior, then displayed in a variety of symbolic formats rather than just disassembly of prefetched instructions. You can choose to display only subroutine calls and returns, all taken branches, only executed instructions, or all bus cycles.

The products also provide deep real-time trace and hardware breakpoints to popular software debuggers, such as XRAY, from Microtec Research, Inc. Symbols can be easily extracted from popular object formats and transferred over the network.

The TLA500, DAS/NT and DAS/XP analyzers are modular instrumentation platforms that can be operated locally using a color X-terminal or from a workstation or PC via a standard X11 server. All come standard with a high-performance Ethernet interface.

The TLA500, DAS/NT and DAS/XP use a family of highly integrated acquisition modules designed specifically to address the requirements of fast, wide, complex RISC-microprocessor buses. 96 channels of 100 MHz synchronous acquisition on each module allows the use of multiple modules to support wider buses (up to 288 channels per bus), multiplexed bus configurations, and multiple microprocessors, with no compromises in speed or timing. Memory depths from 8K to 512K samples permit capturing both the symptom and cause of complex problems. The 10ns resolution time stamp on every cycle allows you to determine accurate timing relationships of any activity over a two-day range.

Software performance analysis provides an overview of actual code activity while executing at full-speed. Histograms show graphically which portions of code are time-intensive. Setup can be automated by importing complete symbol tables. Software and hardware events such as interrupt latency, service-routine execution times, bus timing and other measurements can be analyzed using the Event Measurement capability.

Hardware Development Tools

Features

- Real-time symbolic debug of PowerPC-based systems.
- 100 MHz synchronous acquisition.
- Trace depths to 512K bus cycles.
- Timing analysis on all channels through same probe adapter.
- Operate from stand-alone X-terminal or from workstation or PC.
- Performance analysis.
- Links to high-level languages.
- Ethernet Interface.

Microprocessors Supported

- All available PowerPC microprocessors.

Hosts Supported

- Any host platform with Ethernet (thick or thin), TCP/IP protocol, and an X11/R4-compatible server.

Technical Support

- Local application engineers.
- Technical support hotline.

Availability

- Available now.

Contact

Tektronix, Inc.

P.O. Box 4600
Mail Station 94-860
Beaverton, OR 97076-4600
Tel: (800) 426-2200 ext 316
Tel: (503) 682-3411 ext 316
Fax: (503) 690-3959
Web: <http://www.tek.com/Masurement/Products/>

Europe

Tel: 44 (0628) 486000
Fax: 44 (0628) 47 4799

Japan

Tel: 81 (3) 3448-4611
Fax: 81 (3) 3444-0318

Asia

Tel: 852 2585 6688
Fax: 852 2511 3459

TLS216

Analyzers, Debuggers

Tektronix, Inc.

The TLS216 Logic Scope seamlessly combines the analog acquisition system of a high-speed digital storage oscilloscope (DSO) with the triggering and display systems of a logic analyzer in a single instrument. The 500 MHz, 2 GS/s TLS216 addresses a wide range of applications, and is useful for debugging the high performance digital hardware typical of the computer telecommunications, medical imaging and computer peripheral industries. It also simplifies debugging hardware for moderate performance embedded systems such as engine, traffic or industrial control applications.

In addition to edge, pulse, glitch and pattern triggering, the TLS216 provides two new trigger resources which allow the instrument to directly trigger on common digital

circuit behavior. The time interval or sequence trigger type monitors the time between two events allowing the instrument to easily trigger on setup-time violations, hold-time violations or unexpected propagation delays. The powerful time-out trigger type can detect when an event is missing or does not complete. It also can be used to capture incomplete handshake sequences or to trigger instruments when the system under test hangs.

The Logic Scope offers three display formats to simplify the process of identifying logic timing anomalies or violations. Acquired data can be displayed as either 8-bit analog waveforms (like a traditional DSO), as dual-threshold timing diagrams, or as BusForms (similar to a logic analyzer).

Hardware Development Tools

Features

- 16 analog/digital acquisition channels.
- 2 GS/s simultaneous sampling across *all* channels.
- 500 MHz real-time bandwidth.
- ± 100 ps timing accuracy across all channels.
- 2.5 pF/1 M Ω podlet-style FET probes which fit PowerPC family probe adapters directly.
- Sophisticated, time-qualified triggering including four 16-bit word recognizers.
- Time-correlated mixed signal data display.
- 7-inch internal color monitor.

Microprocessors Supported

- All available PowerPC microprocessors.

Technical Support

- Local application engineers.
- Technical support hotline.

Availability

- Available now.

Contact

Tektronix, Inc.

P.O. Box 4600
Mail Station 94-860
Beaverton, OR 97076-4600
Tel: (800) 426-2200 ext 316
Tel: (503) 682-3411 ext 316
Fax: (503) 690-3959
Web: <http://www.tek.com/Masurement/Products/>

Europe

Tel: 44 (0628) 486000
Fax: 44 (0628) 47 4799

Japan

Tel: 81 (3) 3448-4611
Fax: 81 (3) 3444-0318

Asia

Tel: 852 2585 6688
Fax: 852 2511 3459

Thermal Management Solutions

Hardware Accessories

Thermalloy, Inc.

Thermalloy, Inc. offers a line of thermal management solutions for PowerPC microprocessors. Thermalloy, Inc. is ISO 9001 certified.

Features

- Pin fin heat sinks provide effective cooling for the PowerPC 601, 603, and 604 CQFP and CBGA microprocessors.
- Heat sinks are available with a “Z Spring” integral spring clip, making one component for easy assembly to the PC board.
- Solderable J1 “J Clips” accommodate the Z Spring and fit easily into the PC board. The J1 clip provides a quick, reliable way to attach the heat sink and microprocessor to the PC board. The J1 clip may also be used for electrical grounding.
- Other attachment springs are available for board-space and location considerations.
- Conducta-Cote pre-coated aluminum thermal grease carrier is also available. Conducta-Core improves overall system

performance by reducing the interface resistance to approximately one-third that of a bare joint.

- TCM's® (patented pin fin heat sink with DC brushless, ball bearing fan) are also available where additional cooling is needed.

TCM Information

The following TCM's are available for PowerPC 604 microprocessors. All use the 57-77-1 CAP Conducta-Cote.

<i>TCM</i>	$R_{\theta SA}$	<i>Z Spring</i>
2319B-TCM45S	1.67	PF15
2319B-TCM42S	1.67	PF15
2321B-TCM45S	1.50	PF17
2321B-TCM42S	1.50	PF17

PHOTO #4
(for location only—
do not use keyline)

Hardware Development Tools

Heat Sink Information (Natural Convection)

<i>Processor</i>	<i>Speed (MHz)</i>	<i>Package Style</i>	<i>Heat Sink</i>	$R_{\theta SA}$	<i>Z Spring</i>	<i>Conducta-Cote</i>
PowerPC 601	100	304 CQFP	2333B	7.2	PF17	57-77-1 CAP
PowerPC 601	100	304 CQFP	3332B	6.9	PF17	57-77-1 CAP
PowerPC 603	66/80	240 CQFP	2328B	15.0	PF14	57-77-1 CAP
PowerPC 603	66/80	255 CBGA	2328B	15.0	PF11	57-77-6 CAP

Heat Sink Information (Forced Convection)

<i>Processor</i>	<i>Speed (MHz)</i>	<i>Package Style</i>	<i>Heat Sink</i>	$R_{\theta SA}$	<i>Z Spring</i>	<i>Conducta-Cote</i>
PowerPC 601	50/60/80	304 CQFP	2330B	4.5	PF15	57-77-1 CAP
PowerPC 601	50/60/80	304 CQFP	3332B	4.0	PF17	57-77-1 CAP
PowerPC 601	100	304 CQFP	2319B	6.5	PF17	57-77-1 CAP
PowerPC 601	100	304 CQFP	3320B	5.6	PF17	57-77-1 CAP
PowerPC 603	66/80	240 CQFP	2328B	5.2	PF14	57-77-1 CAP
PowerPC 603	66/80	255 CBGA	2328B	5.2	PF11	57-77-6 CAP
PowerPC 604	100/120	304 CQFP	2335B	3.2	PF18	57-77-1 CAP
PowerPC 604	100/120	304 CQFP	3334B	3.5	PF20	57-77-1 CAP
PowerPC 604	100/120	255 CBGA	2335B	3.2	PF18	57-77-6 CAP
PowerPC 604	100/120	255 CBGA	3334B	3.5	PF20	57-77-6 CAP

Availability

- Available now.

Contact

Thermalloy, Inc.
2021 W. Valley View Lane
Dallas, TX 75234-8993
Tel (toll free): (888) HEATSINK (432-8746)
Tel (toll free—transfer to local rep): (888) THM-REPS (846-7377)
Web: <http://www.thermalloy.com>

Boards

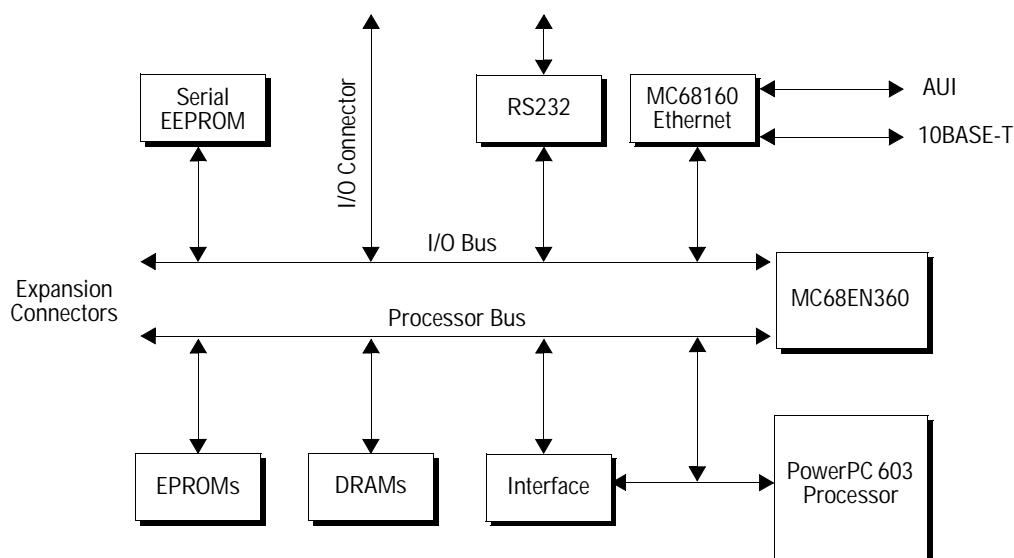
SBC603

Board

Arnewsh, Inc.

The SBC603 is a single-board computer with a PowerPC 603 microprocessor and the MC68EN360 Quad Integrated Communication Controller (QUICC) running in companion mode. It is ideal for training, evaluation and development of microprocessor-based products. It has four byte-wide sockets for EPROMs. The board comes with four 32Kbyte 27C256 EPROMs preprogrammed with a monitor and debugger. You can replace these EPROMs with four 32 KB, 64 KB, 128 KB, 256 KB, 512 KB or 1 MB EPROMs, for up to 4 Mbytes.

The board also has one 72-pin SIMM socket for dynamic RAMs which can be 246Kx32, 1Mx32 or 4 M x 32 SIMMs for a total of up to 16 Mbytes of RAM. The board uses one Serial Management Channel (SMC) channel of the MC68EN360 to provide one full-duplex serial communication channel with software-programmable baud-rate generators. One serial cable is included. One MC68160 Enhanced Ethernet Transceiver with both AUI and 10BASE-T Twisted-Pair Interface connectors. All the processor's signals are available for expansion off the board (not buffered).



Boards

Features

- PowerPC 603 processor running at 25 MHz (bus) and 50 MHz (CPU) in 32-bit mode.
- MC68EN360 Quad Integrated Communication Controller (QUICC) running at 25 MHz. Some of the built-in features of the MC68EN360 are:
 - Multi-protocol support including UART and Ethernet protocol.
 - Four Serial Communication Channels (SCCs).
 - Two Serial Management Channels (SMCs).
 - One SPI channel.
 - Fourteen serial-channel DMAs.
 - Two general-purpose DMAs.
 - Four general-purpose timers.
 - Background debug.
- Four byte-wide EPROMs with monitor and debugger. User-expandable to 4 Mbytes.
- 1 Mbytes of DRAM standard. User-expandable to 16 Mbytes.
- One Motorola 68180 Enhanced Ethernet Transceiver with AUI and 10BASE-T Twisted-Pair interface and connectors.
- One RS232 channel with software-programmable baud rates. One cable is included.
- Socket for one serial EEPROM.
- All I/O channels and functions of MC68360 are available to user.
- Single +5 volts supply is needed.

Specifications

- Board dimensions (approx., in inches): 6.2 x 10.2 x 1.3.
- Power requirement: +5 volts, less than 3 amp., depending on options active.

Availability

- Available now.

Contact

Arnewsh, Inc.
P. O. Box 270352
Fort Collins, CO 80527-0352
Tel: (970) 223-1616
Fax: (970) 223-9573

PowerEngine™ VMTR2x and CVME60x

Boards

CETIA™, Inc./Thomson-CSF™

CETIA is shipping a wide range of VME products based on the PowerPC 601, PowerPC 603 and PowerPC 604 microprocessors. This PowerPC-based family of products, which goes under the name of PowerEngine, includes several single board computers with peripheral and network communication interfaces.

The PowerEngine family features two different architectures:

- **VMTR2x**—the VMTR2x series based on the PowerPC 601 and the PowerPC 604 processors. The VMTR2x series features VME and VSB interfaces. The architecture adopted for these products optimizes memory management functions and interface mechanisms onto the microprocessor bus in order to reap maximum performance from the PowerPC 601 and PowerPC 604 microprocessors. The VMTR2x boards offer up to 256MB onboard DRAM and 8MB Flash for embedded systems. They feature special CETIA-developed ASICS and support a multiprocessor mode under AIX and LynxOS operating systems. Ruggedized versions are also available.
- **CVME60x**—the CVME60x series based on the PowerPC 603 and the PowerPC 604 processors. The CVME60x series features VME and two onboard PCI/PMC interfaces with a high-performance VME64-to-PCI bridge. An additional two PCI/PMC interfaces are also offered. The board is 100% PREP compliant.

In addition to the PowerPC microprocessors, these boards feature:

- 8 to 256MB DRAM.
- 3/4 asynchronous I/Os.
- 1 parallel port (Centronics).
- 1 Ethernet Interface.
- 1 SCSI2 interface.
- VME, VSB, PCI/PMC interfaces.

These two PowerEngine board series allow CETIA to confirm and expand its leadership in the arena of PowerPC Real-Time Systems, enabling CETIA's customers to gain a tremendous performance boost with multiprocessing systems running AIX and LynxOS. By combining these various PowerPC board types in a heterogeneous multiprocessing configuration (clustering), CETIA systems provide scalability and access to the high bandwidth of the VME, VSB bus and PCI bus.

The boards are available under a wide range of UNIX and real-time operating systems: AIX, LynxOS, VxWorks, Vadscore, Adaworld, Windows NT, pSOS+, OS Open, Chorus, OSE.

Boards

Technical Support

A specialized product support team is available to answer customers' queries on VME systems (board computers or workstations) running UNIX or real time operating systems.

Comprehensive assistance and consultancy services are available, offering customers full access to CETIA's extensive customer service resources:

- Training.
- Assistance in porting.

- Assistance in migrating applications to CETIA hardware and system architecture.
- Optimizing and fine tuning of UNIX and LynxOS operating systems.
- Hotline.

Availability

- Available now.
- More products to be announced confirming CETIA's commitment to the PowerPC range of processors.

Contact

CETIA S.A.

Pierre Ravot
150 rue Marcelin Berthelot
Z I de Toulon Est - BP 244
83078 Toulon Cedex
France
Tel: (33) 94 08 80 00
Fax: (33) 94 08 80 01
Email: pravot@cetia.com
Web: <http://www.cetia.com>

CETIA, Inc.

Caroline Quercy
350 Cambridge Avenue, Suite 125
Palo Alto, CA 94306
Tel: (415) 325-6170
Fax: (415) 325-6226
Email: cquercy@cetia.com
Web: <http://www.cetia.com>

CMA Universal Development Platform

Board

Cogent Computer Systems, Inc.

The Cogent Modular Architecture (CMA) Universal Development Platform supports both software and hardware development. This system provides extraordinary flexibility for the 32-bit and 64-bit microprocessor developer. It features interchangeable CPU modules, multiple high-speed I/O slots, 32/64-bit DRAM, and built-in ethernet.

The CMA platform supports the IBM PowerPC 403GA, 403GC and 401GF embedded controllers, and the PowerPC 602, 603, 603e, and 604 microprocessors.

Features

- 32-bit PowerPC 400-family CPU modules.
- 64-bit PowerPC 600-family CPU modules.
- Interchangeable 32/64-bit slot.
- Three high-speed 32/64-bit I/O slots.
- I/O module selections include PCI, FLASH, high-speed SRAM, SCSI, floppy I/O, PCMCIA, Industrial I/O, and more.
- 33 MHz maximum bus operation.
- Up to 32 Mbytes 32/64-bit DRAM.
- 512 Kbytes user EPROM memory.
- 10 Mbits/sec twisted-pair ethernet interface with 32 Kbyte buffer.
- Battery-backed real-time clock with 2 Kbytes of battery-backed NVRAM.
- Dual RS-232 serial ports.
- 2 line x 16 character LCD display.
- Compact 7.9"x7.2" system board with standard PC-AT power supply connector.

32/64-bit Processor Slot

Each CMA Platform allows for one module of choice to be installed. Several processors from the embedded 32-bit PowerPC 400 family or the

64-bit PowerPC 600 family are supported. Contact Cogent for current pricing and availability.

Three High-Speed 32/64-bit I/O Slots

Each CMA system provides three high-speed I/O expansion slots. Each slot has a 32 Mbyte address space and individual interrupt/bus request handshake signals. The simple interface allows for low cost and ease of design. Cogent Computer Systems can provide custom design and support services.

Standard I/O Modules

Cogent provides a wide array of standard off-the-shelf I/O modules including PCI, FLASH, SRAM, PCMCIA, Industrial I/O, and others.

33 MHz Bus Operation

The maximum clock rate for the CMA Bus is 33 MHz. The actual rate is based on the external bus speed of the processor chosen. At 33 MHz the maximum burst data rate of the bus is 120 Mbytes/sec with a 64-bit CPU.

Up to 32 Mbytes 32/64-bit DRAM

The CMA platform has two 72-pin SIMM modules allowing for a minimum of 4 Mbytes and a maximum of 32 Mbytes of memory. For 64-bit CPUs the DRAM provides a burst data rate of 120 Mbytes/sec @ 33 MHz, and for 32-bit CPUs the rate is 60 Mbytes/sec @ 33 MHz.

512 Kbytes of EPROM Memory

Each CPU module has a single user-installable 40-pin EPROM memory socket. The user device can be up to 512 Kbytes in size.

Boards

10 Mbits/sec Ethernet Interface

The CMA Platform has a built-in MB86964 Ethernet Controller with Twisted Pair interface. The packet buffer size is 32 Kbytes.

Battery-Backed Real-Time Clock

A single MK48T02 provides a real-time clock/calendar and 2 Kbytes of battery-protected NVRAM. This RAM is provided for user-defined data that must be maintained during shutdown.

Dual RS-232 Serial Ports

An ST16C552 DUART provides the system with two serial I/O channels capable of up to 110 Kbaud. RS-232 transceivers interface the ports through a pair of RJ-11 connectors.

2 Line x 16 Character LCD

A CM169B provides the user with a simple display which can also be used for debug messages.

System Board

The CMA101 motherboard has compact dimensions of 7.2 inches x 7.9 inches. A standard PC-AT power supply connector provides power to the board. An 8-position dip switch is used to vary the default configuration. Reset and abort push-button switches are also provided.

Industry Standard Software Tools

The CMA Platform currently supports tools from Green Hills Software, Integrated Systems, Wind River Systems, Diab Data, and Software Development Systems. Cogent is continuing to develop support for most major tool products. Contact Cogent for a complete list of third-party vendors.

Availability

- Available now.

Contact

Cogent Computer Systems, Inc.

2 South Cove Rd.
Hubbardston, MA 01452
Tel: (508) 632-2020
Fax: (508) 632-1211
Email: cogent@cogcomp.com

SBC-403

Board

Corelis Inc.

The SBC-403 is a high-performance single board computer that is based on the IBM PowerPC 403GA/GB embedded 32-bit Embedded Controller. The SBC-403GA contains a monitor program that is resident in a byte-wide socketed EPROM. The board contains 1M byte of DRAM, 32 bits wide, that together with the monitor program makes the SBC-403 a powerful software execution and debug platform. The SBC-403 can be used in a variety of applications. As a plug-in CPU core the user can design it into his/her own custom products. Together with the optional logic analyzer preprocessor board it can also be used for software development and debug of real time applications. The built-in discrete port drives 8 LED indicators and can be used as software monitoring flags for the user's program. The built-in monitor program enables the user to set breakpoints in the code, display and/or modify memory and registers, etc., and communicate with a host computer via the RS-232 serial port. The SBC-403 is equipped with a JTAG emulator connector that is compatible with the Corelis PowerEM-403™ JTAG emulator and source level debugger, IBM's RISCWatch™ 400 development system, and with the Corelis SCANTEST™ family of boundary-scan test tools.

Features

- 25-MHz PowerPC 403GA or 403GB RISC embedded controller.
- 128 Kbyte of EPROM/EEPROM, expandable to 1 Mbyte.
- 1 Mbyte of DRAM.
- RS-232 serial port with a DB9 connector.
- JTAG access port for testing and emulation.
- Expansion interface provides access to all PowerPC 403 signals.

- Resident debug monitor program.
- Requires a single 5-volt power supply.
- Optional logic analyzer preprocessor adapter.
- Compact size 3.9 in. X 3.6 in. board.

Monitor Program

The SBC-403GA includes a monitor program that communicates with the PC host via an RS-232 serial port. The monitor program is used for low level debugging and monitoring of the target resources. It supports commands to display memory, modify memory, display registers, modify registers, insert breakpoints, go from, and download files from the host computer to the on-board DRAM memory.

Memory and Expansion

The byte-wide EPROM is plugged into a standard JEDEC compatible 32-pin PLCC socket that accepts up to 1 Mbyte of EPROM or up to 512 Kbyte of Flash EEPROM. 128 Kbyte of EPROM with the monitor program comes standard with the product. The DRAM size is 256 Kwords x 32. Should the need arise, the user could add a custom external memory daughter card that plugs above or underneath the SBC-403 and attaches to the expansion connectors. The expansion connectors are directly mounted on the PowerPC 403 microprocessor and provide the user direct access to all CPU signals that are otherwise very difficult to probe, due to the small pitch packaging of the 403 chip. Having access to all the signals on the connectors makes it easy to add additional hardware external to the SBC-403 such as additional memory, standard I/O ports, logic analyzer preprocessor interface, etc.

Boards

Optional HP Logic Analyzer Preprocessor

The PI-403 is a plug in module that attaches underneath the SBC-403 and provides a simple and easy means of connection to the HP family of logic analyzers. Special hardware on the PI-403 provides signal conditioning that is required by the HP logic analyzer in order to perform state analysis and inverse assembly display of trace data. A software diskette for the HP logic analyzer is also provided. It contains logic analyzer configuration files and a PowerPC inverse assembler.

Specifications

- *CPU*—PowerPC 403GA or PowerPC 403GB embedded controller.
- *CPU Clock*—25MHz (oscillator chip is socketed).
- *EPROM/EEPROM*—128 x 8 (27C010), expandable to 1M x 8 (27C080).
- *DRAM*—256K x 32 (two 256K x 16 devices).
- *Serial Port*—RS-232, up to 19.2K baud (SBC-403GA only).

- *Discrete Outputs*—8 bit, each controls an LED (active low).
- *Reset Switch*—Momentary push button.
- *LEDs*—Power-on (1), Discrete output port (8), all green.
- *Power Requirements*—+5V @ 400 mA max.
- *Serial Port Connector*—DB9, male.
- *Expansion Connectors*—Two 64-pin headers (2 x 32, 0.1" spacing).
- *JTAG Connector*—16 pin header, compatible with PowerEM-403 JTAG emulator and the IBM RISCWatch™ 400 development system.
- *Documentation*—User's manual, Schematics, Bill of Material.
- *Optional Accessories*—Power Supply, PI-403 preprocessor.
- *Ordering Information*—SBC-403GA (160 pin 403GA chip) SBC-403GB (128 pin 403GB chip).

Availability

- Available now.

Contact

Corelis Inc.

12607 Hidden Creek Way
Cerritos, CA 90703
Tel: (310) 926-6727
Fax: (310) 404-6196
Email: sales@corelis.com

Ireland

BIC Systems
Europa House
Harcourt St.
Dublin 2, Ireland
Tel: 353-14754-223
Fax: 353-14754-778

Sweden

Pelcon Electronics AB
Girovagen
S-175 06 Jarfalla
Sweden
Tel: 8-796-9870
Fax: 8-760-7685

Japan

Techno-Port Co. Ltd.
Nakagin Bldg. 10-2
Higashi-Shingashi 2-chome
Mianto-ku, Tokyo
Tel: 81-3-3434-3671
Fax: 81-3-3434-3897

Germany

Synatron
Technopark Neukeferich
Bretonischer Ring 13
D-85630 Grasbrunn
Tel: 89-460-2071
Fax: 89-460-5661

Canada

Testforce Systems
5990 Vanden Abeele
St. Laurant, Quebec
Canada H4S 1R9
Tel: (514) 856-0970
Fax: (514) 856-6983

RTPC 8067 Development Platform and RIO2 Line of Target Platforms

Boards

Creative Electronic Systems SA

Creative Electronic Systems has designed a complete VME processor line based on the PowerPC™ architecture and the PCI bus. The family contains both the RTPC 8067 line of Development Processors and the RIO2 806x line of Target Processors. All are fully compliant with the PREP standard, and are equipped with the PowerPC 603, or PowerPC 604 microprocessors.

The Development and Target Platforms can be delivered with a 66 MHz PowerPC 603 microprocessor up to a 166 MHz PowerPC 604 microprocessor according to performance requirements.

Development Platform Features

- CPU on mezzanine with second level cache providing up to 185 SPECint92.
- Second CPU for redundant operation and on-line diagnostics.
- VME D64 with high-speed list processor.
- VSB Interface on PMC.
- Ethernet, SCSI II, 2 x serial lines.
- One PMC Slot (1+4 PMC slots).
- Processor family: PowerPC 603 and PowerPC 604 microprocessors.
- Native Lynx with local disk on SCSI II interface or remote disk through Ethernet.
- System Support Package (SSP) including drivers and C libraries for VME, VIC, FDL, CAMAC, and FASTBUS interfaces.
- pSOS+™, CHORUS®, VxWorks® Board Support Package (BSP) also available.

Boards

Target Platform Features

- Most compact PowerPC/PCI/VME combination.
- General purpose low-cost VME platform PMC mezzanines (2+4 PMC slots).
- CPU directly on mother board (up to 160 SPECint92).
- VME D64.
- Optional High-Speed VME Block Mover.
- VSB Interface on PMC.
- Remote Reset Input.
- Processor family: PowerPC 603 and PowerPC 604 microprocessors.
- Lynx entirely PROMed or down-line loaded via Ethernet from a server (RTPC 8067 system or other).
- pSOS+™, CHORUS®, VxWorks® Board Support Package (BSP) also available.

Availability

- Available now.

Contact

Creative Electronic Systems SA

70, route du Pont Butin
Case Postale 107
1213 Petit-Lancy 1
Switzerland
Tel: +41 22 792 57 45
Fax: +41 22 792 57 48
Email: ces@lancy.ces.ch

Creative Electronics Deutschland GmbH

Struthweg, 1
D-6467 Hasselroth 1
Germany
Tel: +49 60 55 40 23
Fax: +49 60 55 82 210

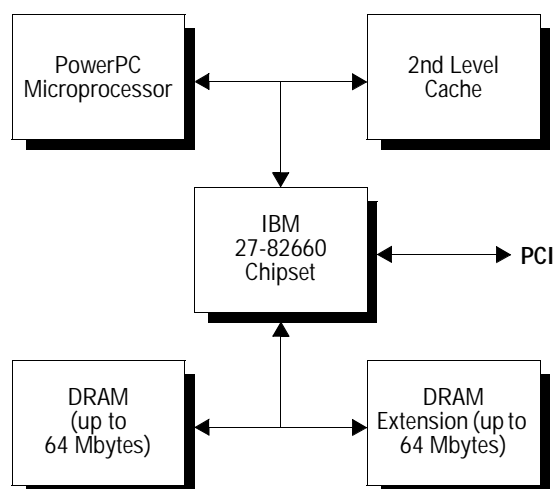
PPCM 8403 Custom Oriented Processor Board

Board

Creative Electronic Systems SA

The CPU subsystem of the PPCM 8403 Custom Oriented Processor Board is contained on a daughter card and is built around a 64-bit PowerPC microprocessor. The PowerPC processor is clocked at 66, 100, or 120 MHz and has an on-chip 2 x 8 Kbytes of first-level cache. It is interfaced to an optional external 512 Kbytes second-level cache. It is bridged to the PCI bus and interfaced to between 8 and 128 Mbytes of DRAM, using the IBM Kauai-Lanai (IBM 27-82660) chipset. Error Correction Code (ECC) is provided for the second-level cache and the DRAM.

A multiple-level write buffer minimized CPU stall cycles during writes to the memory and PCI bus. This, coupled with single-clock DRAM access during cache refills, minimizes the number of CPU cycles wasted due to CPU stalls.



Boards

Features

- 66 MHz PowerPC 603, 100 MHz PowerPC 603e, or 120 MHz PowerPC 604 microprocessor.
- 8 to 128 Mbytes DRAM.
- 512 Kbytes L2 cache (optional).
- Parity/Error Correction Code (ECC) on the entire memory.
- RTC/NVRAM.
- PCI interface to motherboard.
- 150 x 130 mm form factor.

Specifications

- Connector type: AMP Microstrip 536272-4 male.
- Power consumption
 - PowerPC 603 microprocessor: 4W @ 3.3 V, or 5W @ 5V
 - PowerPC 604 microprocessor: 5W @ 3.3V, or 15W @ 5V.

Availability

- Available now.

Contact

Creative Electronic Systems SA

70, route du Pont Butin
Case Postale 107
1213 Petit-Lancy 1
Switzerland
Tel: +41 22 792 57 45
Fax: +41 22 792 57 48
Email: ces@lancy.ces.ch

Creative Electronics Deutschland GmbH

Struthweg, 1
D-6467 Hasselroth 1
Germany
Tel: +49 60 55 40 23
Fax: +49 60 55 82 210

Powerized™ Systems

Boards, Controllers

FirePower Systems, Inc.

The mission of FirePower™ Systems is to be the premier OEM supplier of PowerPC-based systems. FirePower designs and manufactures industry-standard PowerPC-based systems with configurations ranging from system boards to turn-key systems. FirePower's Powerized Systems include both desktop and server lines. The desktop line includes the entry level Powerized ES4100 uniprocessor system and the higher-end Powerized MX uniprocessor and fully symmetrical dual processor systems. The server line will kick-off at the end of the first quarter of 1996 with the introduction of the single- and dual-processor Powerized LX line. The latest versions of Server and Microsoft's Windows NT™ Workstation are fully supported.

FirePower Powerized Systems are designed to be powerful, expandable, and flexible. Powerized MX and LX Systems offer the performance required for power-hungry applications like video editing, image editing,

and high-end graphics. The Powerized MX and LX Systems offer one or two PowerPC processors in a true symmetric multiprocessor implementation, a 128-bit wide memory bus, up to 256 megabytes of memory, a 512 KB L2 cache and PCI and ISA expansion slots. The Powerized LX has support for the fastest PowerPC processors as they become available (including the PowerPC 604e microprocessor) via an upgradeable processor card. Other features include seven peripheral slots (four PCI and three ISA with one shared slot), a fast 128-bit memory bus with built-in ECC memory protection, and an optional 512 KB cache and mini-tower chassis.

The FirePower Powerized Systems are designed from the start to be easy to configure and multi-media ready. Powerized MX Systems come equipped and pre-configured with SCSI-II, Ethernet, sound support, graphics and full size, full frame rate video capture.

Boards

Ordering Information

- Entry level desktop: Powerized ES4100.
- Higher end desktop: Powerized MX (single or dual processor).
- Server: Powerized LX (single or dual processor).

Product specifications are subject to change without notice.

Availability

- Powerized LX line, Powerized ES4100 and Powerized MX uniprocessors available now.

Contact

FirePower Systems, Inc.
Yuri Tsuchitani
190 Independence Drive
Menlo Park, CA 94025
Tel: (415) 462-6229
Fax: (415) 462-3051
Web: <http://www.firepower.com>

PowerPC 403GA™ Evaluation Board Kit

Board, Code, Compiler, Debugger, Utilities

IBM Microelectronics

The PowerPC 403GA Evaluation Board Kit is a complete general-purpose evaluation kit for the PowerPC 403GA and 403GC Embedded Controller.

The PowerPC 403 Evaluation Board Kit provides the 403GA or 403GC processor and all the hardware, software and documentation required for benchmarking and evaluating the 403GA/GC Embedded Controllers.

The PowerPC 403GA evaluation board connects to a host system via serial or ethernet for remote IPL, remote file system and source-level debugging. Supported hosts include IBM RISC System/6000, 386/486/Pentium PC and Sun.

Included in the kit is a limited capacity High C/C++™ compiler, assembler and linker that run on the host. Run-time libraries are provided for ANSI C compatibility, initialization, I/O, workstation file services and PowerPC utilities. The kit also contains source code for the ROM Monitor and samples which can be reused for developing embedded applications. Host tools are provided for building ROM and boot images which can be used to develop evaluation or embedded software.

The board contains a Eurocard expansion connector which can be used to attach custom hardware to the 403 system. Connectors are provided for RISCWatch™ and RISCTrace™. There is an ethernet 10Base2 connector and two RS-232 nine pin serial connectors.

The documentation includes all hardware schematics of the 403 evaluation board. These can be used as reference for your embedded design.

The 403 evaluation Board Kit is compatible with the PowerPC Embedded ABI. It is supported by a number of third party vendors.

Components

- PowerPC 403 evaluation board.
- Power supply and cables.
- ROM Monitor (with source code).
- Source-level debugger.
- Example source code.
- Run-time libraries.
- Limited capacity IBM High C/C++ compiler.
- PowerPC assembler and linker.
- Tools for building ROM and boot images.
- Documentation.
- Workstation file services.

Features

- PowerPC 403GA or 403GC Embedded Controller (33Mhz).
- 128KB flash memory with ROM Monitor.
- Two DRAM banks, each with a standard 72-pin SIMM slot bank 0 is populated with one 4MB SIMM.
- Integrated Ethernet interface with 10Base2 connector.
- Two RS-232 nine-pin serial ports.
- 120-pin Eurocard Type R expansion interface.
- Remote IPL using Boot Protocol (BOOTP) and Trivial File Transfer Protocol (TFTP).
- Sharing of Ethernet port between the ROM monitor and an embedded application.
- C functions for direct access to the on-chip PowerPC 403GA or 403GC serial port.
- Compatible with Embedded ABI and many third party solutions.

Boards

Host Requirements

- RISC System/6000 running AIX 3.2or 4.1.
- 386, 486 or Pentium running DOS/Windows 3.1 with a Windows Sockets compatible TCP/IP protocol stack.
- SPARC Station or equivalent running Solaris 2.3 or SUN OS 4.1.3 with OpenWindows.

Availability

- Available now.

Contact

United States and Canada

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531
Tel: (800) PowerPC
Fax: (800) POWERfax

IBM homepage:
<http://www.ibm.com>

IBM Microelectronics homepage:
<http://www.chips.ibm.com>

Fax Service: (415) 855-4121

Europe

IBM
La Pompignane BP 1021
34006 Montpellier
France
Tel: (33) 6713-5757 (French)
Tel: (33) 6713-5756 (Italian)
Fax: (33) 6713-5750*
*from Paris add 16

IBM
Informations Systeme GmbH
Laatzener Str. 1
30539 Hannover
Germany
Tel: (49) 511-516-3444 (English)
Tel: (49) 511-516-3555 (German)
Fax: (49) 511-516-3888

Japan

IBM
800, Ichimiyake,
Yasu-cho, Yasu-gun
Shiga-ken, Japan 520-23
Tel: (81) 775-87-4745
Fax: (81) 775-87-4735

PowerPC Platform Long Trail Reference Design

Board

IBM Microelectronics

The IBM Long Trail Reference Design meets the specifications of the PowerPC Platform. It uses current and future PowerPC 603e, 604 and 604e microprocessors, and advanced system logic products by VLSI Technology, Inc., making it one of the world's highest performance computing platforms. Long Trail uses PowerPC Firmware from FirmWorks. Long Trail includes all the capabilities that are expected in an advanced design, from PCI 2.1, SCSI, and EIDE communications interfaces to Advanced Graphics and 16-bit audio support. Long Trail is based on the new advanced ATX form factor—an open specification for the PC industry. The ATX specification includes a double-height rear aperture that permits use of both x86 and Apple-style I/O connectors, and makes provisions for full-length add-in cards, improving the potential for cost reduction through improved on-board I/O and physical component positioning.

The Long Trail Reference Design comes with schematics, including symbols, physical design models, software, documentation, and board-level hardware.

Processor Support

- System bus operation up to 66 MHz supported (50, 60, 66 MHz).
- Easy to upgrade the processor via ZIF PGA Socket.
- Plug-in processor with choice of IBM's PowerPC 603e, 604, or 604e microprocessor.

Core Logic Chips

- VLSI Technology, Inc. system logic chips provide:
 - Up to 33 MHz PCI operation on 4 PCI slots (PCI Revision 2.1 compliant).
 - Big-endian and little-endian mode control.
 - Support for ISA bus masters.
 - Memory controller and L2 write-through or write-back cache support.
- VLSI Technology, Inc. multi-function ISA bridge and EIDE interface chip:
 - PCI-compatible (Rev 2.1) and ISA-compatible master/slave interface logic.
 - PCI Arbiter support.
 - ISA system peripheral support.
 - DMA scatter/gather support.
 - Dual channel bus master EIDE interface in both native and compatibility mode.

Support Chips

- Mac I/O chip:
 - OpenPIC (microprocessing interrupt controller).
 - Apple Desktop Bus (ADB) for keyboard and mouse interface.
 - MESH SCSI for hard disk and CD-ROM support.
 - SCC interface to support local talk.
- National Semiconductor PC308VUL Super I/O chip:
 - Plug-N-Play support.
 - X86 peripherals support.
 - PC16C550 UARTS.
 - PC8477 floppy disk controller.
 - IEEE 1284 EPP/ECP parallel support.
 - Keyboard and mouse controller.
 - Real-time clock.

Boards

Memory Subsystem

- 168-pin DIMM sockets.
- Total memory 192MB to 768MB (using 16MB and 64 MB DRAM, respectively).
- Parity or non-parity.
- Fast page mode, EDO, burst EDO, and SDRAM capable.
- On-board 256 KB pipelined burst L2 cache.
- Upgrade to 512KB via industry standard 160-pin connector.

Boot ROM/NVRAM

- 512K flash boot ROM connected to ISA bus, with FirmWork's Power Firmware Open Firmware boot code and Run-Time Abstraction Service compatible with Windows NT, Mac OS 7.5 and 8.0.
- 8KB NVRAM connected to ISA bus (expandable to 16KB).

Macintosh Toolbox ROM

- 160-pin connector for 4MB ROM module.

Audio

- PowerPC platform-compliant 16-bit audio subsystem on-board.
- FM synthesis.
- Wave table card and 3D sound upgrade capability.

Availability

- Available now.

Contact

United States and Canada

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531
Tel: (800) PowerPC
Fax: (800) POWERfax

IBM homepage:
<http://www.ibm.com>

IBM Microelectronics homepage:
<http://www.chips.ibm.com>

Fax Service: (415) 855-4121

Europe

IBM
La Pompanne BP 1021
34006 Montpellier
France
Tel: (33) 6713-5757 (French)
Tel: (33) 6713-5756 (Italian)
Fax: (33) 6713-5750*
*from Paris add 16

IBM
Informations Systeme GmbH
Laatzener Str. 1
30539 Hannover
Germany
Tel: (49) 511-516-3444 (English)
Tel: (49) 511-516-3555 (German)
Fax: (49) 511-516-3888

Japan

IBM
800, Ichimiyake,
Yasu-cho, Yasu-gun
Shiga-ken, Japan 520-23
Tel: (81) 775-87-4745
Fax: (81) 775-87-4735

Total Power™ NuBus, Total Power PCI, and Total Freedom™

Boards

Total Impact™

Total Impact designs and markets PowerPC application accelerator boards for Apple Power Macintosh computer systems. The Total Power boards allow software developers the full access of the host Macintosh computer system while supplying additional performance with the PowerPC 604 processor. The Total Power boards can be used as an additional processor working in conjunction with the host system's processor or as a coprocessor used to run specific compute-intense tasks.

Total Power NuBus

Total Power is a NuBus application accelerator board designed to work with NuBus based Power Macintosh or compatible systems. The board is available in speeds of 100, 120 and 133 MHz with up to 128 megabytes of on-board memory. The board has bus-mastering capabilities and can also access other Total Power boards within the same system or over a network.

Total Power PCI

Total Power PCI is a PCI application accelerator board designed to work with PCI-based Power Macintosh or compatible systems. The board is available with 1, 2 or 4 PowerPC 604 microprocessors operating at 100, 120, 133 or 150 MHz. The board is available with up to 1 megabyte of Level 2 cache and up to 256 megabytes of on-board memory. The board has bus-mastering capabilities and can also access other Total Power boards within the same system or over a network.

Total Freedom

The Total Power boards are controlled by the Total Freedom operating-system interface. Total Freedom interfaces directly into the Apple Operating System ToolBox and allows application software to be launched on the Total Power accelerator the same way that it is launched within the Power Macintosh itself. Total Freedom intercepts the launching process of the Power Macintosh and directs it to the Total Power accelerator.

Total Freedom offers a multi-threaded developer environment that works directly within Apple's operating system for use with multiprocessor systems.

Because the code that is launched on the Total Power board is the same code that runs on the Power Macintosh, a separate or "special" version of a software application is not required. Virtually any software application that runs on a Power Macintosh can easily be modified to take advantage of the Total Power accelerator board, whether it is written in C, C++, FORTRAN or PASCAL.

Boards

System Requirements

- Apple Computer Power Macintosh full-size NuBus or PCI connector, System 7.5.

Availability

- Total Power NuBus: Available now.
- Total Power PCI: Available now.
- Total Freedom: Available now.
- Total Freedom NT: Available now.

Contact

Total Impact

79 Daily Drive, Suite 177
Camarillo, CA 93010
Tel: (805) 987-8704
Fax: (805) 484-9469
Email: power@totalimpact.com
Web: <http://www.totalimpact.com>

Boards

Services and Documentation

Introduction to RISC and PowerPC

Training

Apple Computer, Inc.

This interactive, color animation training course introduces the basics of RISC technology and development for Power Macintosh systems. It describes the internal architecture of the PowerPC 601 microprocessor, the run-time architecture of the Power Macintosh computers, and how to prepare your existing code for recompilation on Power Macintosh computers.

The training course is designed for any application developer interested in moving code to PowerPC, managers of development groups who wish to determine whether they should move their code to PowerPC, and anyone who just wants a basic grounding in RISC technology.

The first part of the course assumes a limited understanding of microcomputers. The second part assumes Macintosh programming experience, primarily using C.

Course Contents

- *Part 1: Introduction to RISC Technology*
 - Brief history of computing.
 - Introduction to microcomputer technologies.
 - CISC and RISC instruction sets.
 - Apple's RISC strategy.
- *Part 2: Programmer's Introduction to PowerPC*
 - PowerPC hardware architecture and instruction set.
 - Power Macintosh runtime architecture, including calling conventions, shared libraries, accessing global data, and combining 68k and PowerPC code.
 - Programming for Power Macintosh, including strategies for moving source code, porting C and C++, PowerPC compatibility issues, and performance tuning.

Services and Documentation

System Requirements

- Macintosh II or greater.
- System 6.0.7 or later.
- CD-ROM drive.
- 12" monitor (color highly recommended).

Availability

- Available now.

Ordering Information

- Order Number R0172LL/A

Contact

Apple Computer, Inc.

APDA
P.O. Box 319
Buffalo, NY 14207-0319
U.S.: (800) 282-2732
Canada: (800) 637-0029
International: (716) 871-6555
Fax: (716) 871-6511
Web: <http://dev.info.apple.com/du/online.html>

Open Firmware System ROM and Device Driver Consulting

Consulting Service

FirmWorks

Open Firmware, formally known as IEEE Standard 1275-1994, is the first non-proprietary open standard for boot firmware that is usable on different processors and buses. Open Firmware includes a processor-independent *device interface* that allows an add-in peripheral card to identify itself and to supply a single boot driver that can be used, unchanged, on any CPU using Open Firmware. Open Firmware also includes a *user interface* with powerful scripting and debugging capabilities, and a *client program interface* that allows operating systems and their loaders to make use of Open Firmware services to assist in the configuration and initialization process. Open Firmware is required by the PowerPC Reference Platform Specification and by the Common Hardware Reference Platform Specification.

Services

FirmWorks, specialists in providing Open Firmware solutions, provides the following products and services to decrease your time to market:

- Power Firmware™, Open Firmware system ROM for PowerPC systems supporting PCI, ISA and other buses.
- Off-the-shelf and custom drivers for PCI/ISA peripheral cards.
- Architectural advice for your new designs.
- Bring-up assistance with new systems.
- IEEE Standard 1275-1994 compliance testing.
- Training:
 - IEEE Standard 1275-1994.
 - Forth.
 - Open Firmware porting.
 - Writing Open Firmware drivers.
 - Writing and debugging Open Firmware client interface programs.
 - Using Open Firmware.
 - Manufacturing diagnostic use.
 - Field service diagnostic use.

Founded by Mitch Bradley, the principal architect of Open Firmware, FirmWorks can provide everything from a turnkey solution for your Open Firmware needs to assistance in the creation of your own implementation.

Services and Documentation

Technical Support

- Consulting services.
- Telephone support.
- Training:
 - At FirmWorks.
 - At your site.

Availability

- Standard products available now.
- Call us for custom products/support.

Contact

FirmWorks

Suite 115
480 San Antonio Road
Mountain View, CA 94040-1218
Tel: (415) 917-0100
Fax: (415) 917-6990

Email: ppc-tools@firmworks.com
<ftp://ftp.firmworks.com/pub>
Web: <http://www.firmworks.com>

Writing FCode Programs for PCI

Documentation

FirmWorks

Open Firmware is required by the PowerPC Reference Platform Specification and by the Common Hardware Platform Specification. Many PowerPC systems incorporate the PCI bus. To assist PCI developers in creating Open Firmware compliant products, FirmWorks has written a manual, *Writing FCode Programs for PCI*.

This manual, available exclusively from FirmWorks, is an adaptation of previously-existing FCode programming documentation that has been customized for Open Firmware and PCI. The manual clearly explains the theory and practice of writing and producing FCode programs and is filled with program examples to help you get started.

If you are ready to make the move to Open Firmware on PCI, this manual will help you make a smooth transition.

Services and Documentation

Availability

- Available now.

Contact

FirmWorks

Suite 115
480 San Antonio Road
Mountain View, CA 94040-1218
Tel: (415) 917-0100
Fax: (415) 917-6990

Email: ppc-tools@firmworks.com
<ftp://ftp.firmworks.com/pub>
Web: <http://www.firmworks.com>

Open Firmware Command Reference

Documentation

FirmWorks

Open Firmware is required by the PowerPC Reference Platform Specification. To assist users of Open Firmware compliant systems, Firmworks has created *Open Firmware Command Reference*. This manual, available exclusively from FirmWorks, is an expanded version of previously-existing OpenBoot™ documentation that has been adapted to Open Firmware. It completely describes how to use the Open Firmware user interface and will help you achieve “power user” status quickly.

This manual contains chapters on:

- The use and configuration of Open Firmware-based machines.
- How to boot a machine.
- How to work with file systems.
- The definition and use of all available user interface commands.
- How to load and execute programs.
- How to use Open Firmware debugging tools, including many shortcuts and debugging tips.

It also contains appendices on:

- Communicating with an Open Firmware system through a serial port.
- Common configuration problems and their solutions.
- Machine-specific characteristics (including Forth assembler syntax and use) of PowerPC, SPARC and 80x86 machines.

If you are making the move to Open Firmware, this manual will help you make a smooth transition.

Services and Documentation

Availability

- Available now.

Contact

FirmWorks

Suite 115
480 San Antonio Road
Mountain View, CA 94040-1218
Tel: (415) 917-0100
Fax: (415) 917-6990

Email: ppc-tools@firmworks.com
<ftp://ftp.firmworks.com/pub>
Web: <http://www.firmworks.com>

Design and Prototype Development Services

Consulting Services

Gordian

Gordian, established in 1986, provides contract engineering design and prototype development services. Over the past ten years we have designed technically sophisticated consumer and industrial products and product components for industry leaders as well as young emerging companies. Our success stems from our ability to devise innovative solutions to challenging design problems. Working in small, dedicated design teams allows us to develop integrated, well-engineered products at an accelerated time-to-market.

Services

- *Hardware Design*
 - System architecture.
 - Schematic capture.
 - FPGA/ASIC design (VHDL, schematic capture, simulation)
 - PCB layout.
- *Software Design*
 - Embedded operating systems.
 - Application level code.
 - Graphical user interfaces.
 - Device drivers.
 - Protocol stacks and routers.
 - Internet applications (Java applets).
- *Mechanical Engineering and Industrial Design*
 - Cases, enclosures, and packaging
 - Electro-mechanical systems
 - Mechanical design (system integration, manufacturability, FEA)
 - End-user research (determining both user needs and preferences)
 - Product identity (as a stand-alone product or as part of a family)

Resources

We have a multidisciplinary team of talented and highly-trained computer, electrical, mechanical, and test engineers, computer scientists, physicists, industrial designers, and technical writers. In addition to our formal training, we often seek knowledge beyond the scope of our projects in order to further our skills in related fields and technologies. We also maintain a wide array of hardware and software tools, including HP, SGI, Sun, IBM, DEC, PC, and Macintosh workstations for hardware design, software development, documentation design and development, and 3D mechanical design. We also have support and debugging equipment such as logic analyzers, oscilloscopes, serial and Ethernet protocol analyzers for testing and analysis, a spectrum analyzer, and a PAL/PROM/FPGA programmer.

Areas of Expertise

- Computer networking (LAN, WAN, serial).
- Computer peripherals.
- Operating systems.
- Digital electronic design.
- Embedded systems design.
- ASIC/FPGA gate array design.
- Specialized processors (MCUs, integrated processors, GSPs, DSPs).
- Design for manufacturability.
- Industrial design.
- Raster graphics processing.
- Optical technology and imaging.
- Electro-optical systems and imaging.
- Telecommunications.

Services and Documentation

Availability

- Available now.

Contact

Gordian

Attn: Tom Ambrose
20361 Irvine Ave.
Santa Ana Heights, CA 92707-5637
Tel: (714) 850-0205
Fax: (714) 850-0533
Internet: marketing@gordian.com
Web: <http://www.gordian.com>

PowerPC Reference Platform Specification

Specification

IBM Corporation

The PowerPC Reference Platform Specification describes the devices, interfaces, and data formats required to design and build a PowerPC-based, industry standard computer system. It is written to create a hardware specification which, coupled with hardware abstraction software provided by the operating system or hardware system vendors, allows the computer industry to build PowerPC systems that all run the same shrink-wrapped operating systems and the same shrink-wrapped applications for those operating environments.

The specification defines a system architecture that covers most traditional computer systems, from portables to servers. The specification gives system developers the freedom to choose the level of market differentiation and enhanced features required in a given computing environment.

The specification defines the minimum functional requirements needed for a compliant PowerPC Reference Platform implementation. It also provides a list of recommended hardware subsystems, devices and interfaces, which, if used in a PowerPC Reference Platform implementation, yield a level of functionality required by most operating environments.

The specification also describes a reference implementation which is a fully functional PowerPC Reference Platform system design supporting all operating systems and applications which are being ported to this reference platform. This Reference

Implementation provides an example to which system developers can compare, allowing them a better understanding of their own design goals. The Reference Implementation may be built by any system vendor seeking to reduce development expense for software and hardware. A hardware system vendor may change subsystems from those used in the Reference Implementation, but must supply abstraction software.

The specification is written primarily for hardware system vendors, but provides valuable information for operating system, device driver, adaptor, and ASIC vendors. It will also assist value-added resellers. The specification supports all 32-bit PowerPC processors. It is intended to cover the following systems:

- Portables
- Medialess systems
- Desktops
- Workstations
- Servers

The specification allows support for multiple operating systems, each using different methods of abstracting hardware variations. Finally, because the specification requires machine abstractions, it can accommodate the evolution of software and hardware technologies without losing system compatibility.

Features

- *Hardware Configuration*—Defines the minimum and recommended hardware standards and capacities required to be compliant and compatible with targeted operating environments.
- *Architecture*—Defines the minimum and recommended hardware system attributes required to design a compatible computer system.
- *Machine Abstractions*—Defines the general approaches that software should take to bridge differences within subsystems.
- *Boot Process and Firmware*—Defines the boot architecture, which supports all targeted operating systems.
- *Reference Implementation*—Describes an example implementation of a compliant system.
- *Appendices*—Several appendices describe alternate implementations (e.g., portables, servers), bi-endian design, the four operating systems hosted to this platform, and compatible devices.

Ordering Information

- Order number MPR-PPC-RPU-02.

Availability

- Available now.
- See the *PowerPC Microprocessor Common Hardware Reference Platform: A System Architecture* catalog entry for information on a follow-on architecture and implementation standard.

Contact

IBM Corporation

Tel: (800) POWERPC (769-3772)

If multilingual operators are required: (708) 296-6767

Europe, in English: 49-511-516-3444

Europe, in German: 49-511-516-3555

Asia, in Japanese: 81-755-87-4745

PowerPC Educational Courses

Training

IBM Corporation

IBM offers a comprehensive PowerPC curriculum for programmers, system designers, engineers and those in support positions. Courses can be at IBM locations or at customer locations. The curriculum has four major sections:

- Introductory Education
- Systems Development
 - PowerPC Hardware System Architecture
 - Subsystem Hardware Architecture
 - Reference Platform Specification and System Design Kit Education
 - CMOS Circuit Technology
 - Microelectronics Packaging Education
- PowerPC Assembly Level Programming
- Customized Education

Introductory Education Courses

This section is designed to introduce PowerPC Technology attributes. It provides an industry focus—defining what PowerPC is, how it evolved, its current position and expected impact in the computer industry. Courses now being offered or available for scheduling include:

- PowerPC Technology—The Bird's Eye View (N1797, 1 day)

Systems Development Courses

Courses in this section are intended for product developers and technical support personnel who need in-depth understanding of PowerPC processors, and system and subsystem architectures. Courses now being offered or available for scheduling include:

PowerPC Hardware System Architecture

- PowerPC 601 System Architecture (P1085, 3 days)
- PowerPC System Architecture Overview for System Developers (N1838, 1 day)
- PowerPC 603 Hardware System Architecture (N1835, 2 days)
- PowerPC 604 Hardware System Architecture (N1840, 2 days)
- PowerPC Embedded Controllers (P1106, 5 days)

Subsystem Hardware Architecture

- Industry Standard Architecture (ISA) (N1814, 4 days)
- PCI System Architecture (N1872, 3 days)
- PCI Software Environment (N1914, 1 day)
- Plug & Play System Architecture (N1915, 2 days)
- Introduction to Universal Serial Bus (N1967, 1 day)
- Serial Storage Architecture (SSA) (N1811, 3 days)
- Intro to Serial Storage Architecture (SSA) (N1843, 1 day)
- PCMCIA System Architecture (N1831, 2 days)
- An Introduction to SCSI (N1809, 1 day)
- Overview of Disk Drive Interfaces (N1845, 1 day)
- SCSI: The Physical Interface (N1808, 1 day)
- An In-Depth Exploration of SCSI (N1807, 3 days)
- Intro to Fibre Channel (N1911, 2 days)
- Fibre Channel Arbitrated Loop (N1912, 1 day)

Services and Documentation

Reference Platform and System Design Kit Education

- PowerPC 601 System Design Kit (N1846, 3.5 days)
- PowerPC Reference Platform Specification and 601 Design Kit Overview (N1841, 1 day)
- PowerPC 603 System Design Kit (P1093, 3.5 days)
- PowerPC 601 to 603 System Design (P1102, 1 day)
- PowerPC Platform (CHRP) (N1960, 2 days)

CMOS Circuit Technology Education

- Introduction to CMOS (N1637, 2 days)
- Advanced Techniques for CMOS Circuit Design (N1639, 1 day)
- Introduction to the Physical Design and Layout of CMOS ICs (N1856, 2 days)

Microelectronics Packaging Education

- Thermal Management of Electronics Packages (N1655, 4 days)
- PCB Design and Electrical Performance (N1730, 1 day)
- Introduction to Solder Bump Flip Chip Technology - C4 (N1731, 1 day)
- Microelectronics Package Design: New Direction (N1732, 3.5 days)

Assembly-Level Programming Courses

PowerPC Assembly Level Programming teaches the contents of the IBM PowerPC Architecture Manual using the PowerPC 603 processor as a model. Unique instructions and functions of the other PowerPC processor are highlighted. Courses now being offered or available for scheduling include:

- PowerPC Assembly Level Programming for Applications Software w/Lab (N1798, 3 days)

Customized Education

Specialized courses can be developed to meet any customer's needs. By mixing modules from existing courses and augmenting with new special requirements, courses can be developed to reflect the customer's business situation.

Contact

IBM Corporation

Hojat Shah
IBM Corporation
11400 Burnet Road
M/S 4328
Austin, Texas 78758
Tel: (512) 838-6752
Fax: (512) 838-5168
Email: hojats@vnet.ibm.com

James H. Edwards
IBM Corporation
500 Columbus Avenue
Thornwood, NY 10594
Tel: (203) 921-1816
Fax: (203) 921-1816
Email: jhedwards@vnet.ibm.com

PowerPC Microprocessor User's Manuals

Documentation

IBM Microelectronics

The PowerPC RISC Microprocessor User's Manuals provide fully-detailed technical descriptions of the microprocessors in the PowerPC RISC microprocessor family. The manuals are written for designers of hardware, systems software, and applications, as well as for in-depth evaluations of the PowerPC microprocessors or the PowerPC architecture.

Each manual includes a table of contents, glossary, appendices, index, and the following technical discussions:

- *Overview*—Feature summary, block diagram, register-to-register architecture, instruction set, cache implementation, exception processing, memory management, instruction timing, and system interface.
- *Registers and Data Types*—Register set, implementation-specific registers, and operand conventions.
- *Addressing Modes and Instruction Set Summary*—Classes of instructions, memory addressing, integer instructions, floating-point instructions, load and store instructions, flow control instructions, and others.
- *Cache and Memory Unit Operation*—Cache organization, cache operations, cache coherency, and cache control instructions.
- *Exceptions*—Exception classes, exception processing, and exception definitions and descriptions.
- *Memory Management Unit*—MMU overview, TLB description, memory and cache access modes, direct address translation, block address translation, memory segment model, hashed page tables, I/O controller interface address translation, and breakpoint facility.
- *Instruction Timing*—Instruction timing overview, the instruction queue, general instruction flow, execution unit timings, memory performance considerations, and instruction latency.
- *Signal Descriptions*—Address bus arbitration signals, address transfer signals, data bus arbitration signals, data transfer signals, system status signals, test signals, and clock signals.
- *System Interface Operation*—System interface overview, memory access protocol, address-bus tenure, data-bus tenure, timing examples; interrupt, checkstop and reset signals.
- *Instruction Set*—Instruction formats, details of the instructions, and instructions not implemented.

Services and Documentation

Ordering Information

- PowerPC 601 User's Manual
 - IBM part number SA14-2007-00.
- PowerPC 602 User's Manual
 - IBM part number SC22-9899-00.
- PowerPC 603e User's Manual
 - IBM part number SA14-2029-00.
- PowerPC 604 User's Manual
 - IBM part number SA14-2044-00.
- The PowerPC Microprocessor Family: The Programming Environments
 - IBM part number MPRPPCFPE-01.
- PowerPC 403GA User's Manual
 - IBM part number SC22-9894-00.
- PowerPC 403GB User's Manual
 - IBM part number SC22-9895-00.
- PowerPC 403GC User's Manual
 - IBM part number SC22-9896-00.
- PowerPC 401GF User's Manual
 - IBM part number SC09-3031-00.

Availability

- Available now.

Contact

IBM Microelectronics
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531
Tel: (800) PowerPC
Web: <http://www.chips/ibm/com/products/ppc>

Hardware Design Services

Consulting Services

Idealogy™, Inc.

Idealogy, Inc. was founded in 1992 and specializes in providing hardware design verification tools and services that help engineering teams verify the functionality of their PowerPC designs. Having participated in numerous PowerPC design projects employing top-down design techniques, Idealogy has the expertise to be a significant contributor to any system vendor's design staff.

Idealogy has built and maintains expertise in all phases of the hardware design cycle, but has particular expertise in design verification and all the relevant issues that form the basis of an efficient and effective design verification process. This includes device modeling, design methodology, hardware description language techniques, design/database management, and team communications. Idealogy has several products available that can be used to verify your design in any Verilog or VHDL environment. Furthermore, Idealogy can customize these products as needed to complement your existing design environment and current project needs.

Strategic Design Verification

Idealogy's principal focus is on developing project-wide verification strategies that support full-system verification and implementing the tools, models, and tests necessary to execute on the strategy. These strategies have been successfully used to verify systems in the computer, graphics and video, networking, and communications markets. By using Idealogy's tools and services, system vendors can release their designs to manufacturing with confidence that the designs will work correctly, in the target system, the first time.

Streamlined Verification Process

In addition to providing valuable design verification tools and services, Idealogy has a proven track record of streamlining the efficiency of design teams composed of multiple design engineers. Idealogy's customers can expect to receive tools and services that emphasize teamwork, customer satisfaction, and customer process improvement. And, Idealogy strives to exceed these expectations by delivering verification solutions that maximize the productivity of every individual engineer, as well as the team as a whole, from project start to manufacturing release.

Custom Model and Testbench Creation

Idealogy verification models are a critical element of an overall verification strategy. These models serve to bridge the gap between a test writer's intent and the specific detail of how a test is actually applied to the design being tested. Idealogy models have more functionality than that found in typical simulation models, allowing higher overall test productivity by covering more cases with fewer tests. Frequently, Idealogy models also have enough knowledge of the overall system that they can automatically detect bugs in the design as the simulation progresses.

Services and Documentation

PowerPC Models

Idealogy's PowerPC models (including PowerPC 601, PowerPC 603, and PowerPC 604 processors) are bus-functional models that allow you to determine if your design will operate properly under all possible transactions that might occur on the PowerPC bus. These models contain the detail necessary to support verification of cache coherency and deadlock prevention, even in multiprocessor systems of any architecture. When used with one of Idealogy's customized verification environments, these models help to ensure that your design will be error free, especially with respect to overall system-level functionality.

Additional models are available, and Idealogy can quickly develop any model on a custom basis. See Idealogy's World Wide Web home page for a listing of the models that are currently available.

Tools/Products

- Idealogy Panda™ Verification Environment. Verification productivity tools for Verilog.
- Idealogy Tomahawk™ Verification Environment. Verification productivity tools for VHDL.

Areas of Expertise

- Coherent bus protocols (including PowerPC).
- Bus to bus bridge ASICs (for example, PowerPC to PCI).
- Video and graphics systems (for example, interactive TV, games).
- Communications and network systems (for example, ATM).

Supported Design Environments

- Verilog®
 - Cadence™ (Verilog-XL®).
 - Viewlogic® (VCS™).
 - Intergraph® (VeriBest™).
- VHDL
 - Mentor Graphics® (QuickVHDL™).
 - Model Technology (V-System/VHDL Windows™).
 - Viewlogic® (ViewSim®, Vantage).

Availability

- Available now.

Contact

Idealogy, Inc.
The Design Verification Specialists
1919 14th Street, Suite 421
Boulder, CO 80302
Tel: (303) 440-8636
Fax: (303) 440-5210
Email: info@idealogy.com
Web: <http://www.idealogy.com>

Power Micro Research

Consulting Services

Power Micro Research

The PowerPC microprocessor family has established itself as the first credible challenger to the Intel monopoly on commodity PC processors. During the last 2 years many companies, from embedded systems manufacturers through desktop PC clone builders to high end MPP vendors, have picked the PowerPC as the engine for their high performance products. Power Micro Research has been involved with many of these companies and helped them successfully bring their products to market. We provide an in depth expertise in the PowerPC microprocessor and related system design issues that can help do the same for your products.

Power Micro Research provides system consulting services ranging from architecture education and design evaluations through PowerPC-based system designs and prototypes. Our primary focus is on low level software support of hardware. This includes system and processor diagnostics, embedded firmware, device drivers, OS ports, and performance analysis and tuning.

The team at Power Micro Research is comprised mainly of former IBM senior architects, designers, and implementers. We were involved either directly or in an architecture role with most of the IBM offerings in the PowerPC microprocessor, RS/6000, and AIX lines. More information about the company, the people, and the projects completed to date can be found on the Power Micro Research WEB site located at www.pmr.com

Services

- Initial system bring-up, including hardware debug, boot ROM development and hardware diagnostics.
- Custom software including operating system porting, device driver implementation, system libraries, subsystem enhancements and performance tuning.
- Hardware and software verification test suites. Compiler and run-time library enhancements including parallel programming extensions.
- Application development, porting and optimization.
- Specialty systems including embedded control systems, data collection and analysis, video servers and set top boxes.
- Seminars on PowerPC architecture/system technology and the AIX® operating system.

Services and Documentation

Availability

- Available now.

Contact

Power Micro Research

Jim Mott
213 Congress Ave.
Suite 222
Austin, Texas 78701
Tel: (512) 258-5537
Fax: (512) 258-7916
Email: jim@pmr.com
Web: <http://www.pmr.com>

PowerPC Design and Development Services

Consulting Services

Questa Consulting

Time-to-profit is the value proposition and focus of Questa's Software & Embedded Systems consulting group. Questa helps its clients expedite the development cycle of software and computer intensive products through its unique *Service Velocity* approach to product and technology development consulting. Questa further helps its clients maximize the value of advanced technology, such as PowerPC microprocessors, with its software-oriented *Silicon Integrations* services.

Today, technology such as that found in PowerPC processors is available to all companies developing products. Those companies that can consistently extract an incremental amount of additional performance and function from technology will have a competitive advantage in the marketplace. Questa brings to its clients the knowledge and experience needed to extract the true potential from technology. Questa's internal technology exploration activities enable us to develop detailed knowledge and experience with emerging technologies. Our own R&D has created a PowerPC competency group within Questa that collectively has nearly 20 man-years of hands-on PowerPC design and software experience.

Questa Consulting is a leading software and computer consulting and engineering firm that focuses on the development of high-performance, high-technology software and embedded systems for the next generation of "smart" electronic imaging products. Our competencies encompass the technologies of embedded systems, networking, and host (client) computing. Collectively, this skill and knowledge enables Questa to contribute to the development of the next generation of smart machines—internetworked and interoperating, and fully accessible from traditional PCs, workstations, LANs and the Internet.

Questa's corporate office is in Rochester, NY, the imaging capital of the world. Questa also maintains regional offices in Research Triangle Park in Raleigh, NC, Sunnyvale, CA, and Burlington, MA.

Services and Documentation

Availability

- Available now.

Contact

Questra Consulting
300 Linden Oaks
Rochester, NY 14625
Tel: (716) 381-0260
Fax: (716) 381-8098

ASIC and System Board Design Services

Consulting Services

Sand Microelectronics, Inc.

Sand Microelectronics, founded in November 1990, provides engineering consulting services in the areas of ASIC design, behavioral and synthesizable model development and system board design. The founders have over 45 years of combined experience in the management and development of VLSI ASIC and system board products. The company has successfully developed products for multi-billion dollar organizations on a turnkey project or joint-development basis.

Services

- ASIC and FPGA Design.
 - Turnkey design, specification to prototypes.
 - High-level logic design (Verilog, VHDL).
 - Logic synthesis (Synopsys).
 - Functional simulation (Verilog, Viewlogic).
 - System level simulation.
 - Static timing analysis (Motive, Veritime).
 - Test-vector generation.
 - Chip layout, floor planning, routing, and LVS.
 - ASIC re-targeting to multiple foundries.
 - FPGA designs (Altera®, Xilinx™, Actel®).
 - FPGA to ASIC conversion.
- Model Development.
 - Behavioral models for system simulation CPU, memory, and buses.
 - Synthesizable cores.
- System Board Design.
 - Turnkey design, specification to prototypes.
 - Schematic capture (Orcad, Viewlogic, Concept).
 - PCB layout, fabrication and assembly.

Resources

Our team is comprised of highly motivated, technically qualified professionals. All individuals have an MSEE or higher qualification with an average industry experience of ten years. We have successfully developed over 25 ASICs of varying complexities for a wide range of applications. Our facility is located in the heart of Silicon Valley and is equipped with state-of-the-art computing hardware and software, including high-performance Sun workstations, PCs, and CAD software.

Areas of Expertise

Sand has successfully developed products in the following areas:

- RISC CPU—PowerPC 601 microprocessor.
- CISC CPU—x86, Pentium™.
- PC desktop, notebook chipsets.
- Cache and memory-controller design.
- Bus controllers—PCI, VL, ISA, EISA, MCA.
- Graphics and video controllers.
- Video compression (JPEG, MPEG).
- Networking.
- Motherboard and adapter card designs.

Services and Documentation

CAD Tools Experience

- High-Level Design:
 - Viewlogic VHDL
 - Cadence Verilog-XL®
- Schematic Capture:
 - Orcad®
 - Viewlogic
 - Cadence Concept™
- Simulation:
 - Viewsim®
 - Verilog®
 - IKOS
 - Zycad
- Synthesis and Optimization:
 - Synopsys
 - Autologic
 - Exemplar
- Static Timing Analysis:
 - Motive
 - Veritime™
- Layout, Place and Route:
 - Cadence Opus™
 - Dracula™

Availability

- Available now.

Contact

Sand Microelectronics, Inc.

Attn: Anand Naidu
3350 Scott Boulevard, #24
Santa Clara, CA 95054
Tel: (408) 235-8600
Fax: (408) 235-8601
Email: sales@sandmicro.com
Web: <http://www.sandmicro.com>

PowerPC Design Service

Consulting Services

Tadpole Technology

Tadpole's PowerPC design service takes the risk out of using a new processor. We handle the board development and O/S porting, allowing you to concentrate on your strengths.

Services

- Fast turnaround to reduce time-to-market.
- A focused design team with over ten years' experience of custom OEM design and development.
- Extensive PowerPC design experience from ASICs to boards to complete systems.
- Comprehensive software support including UNIX and real-time operating system porting.

- In-house surface-mount manufacturing facilities for both prototypes and production.
- An extension to your team. Tadpole becomes an integral part of your product development project.
- ISO 9001-registered company.

Tadpole's design experience ranges from laser-printer engines and multi-processor flight-simulation systems to IBM's first PowerPC-based notebook, with the emphasis on high-performance, high-integration products for special-purpose applications.

Services and Documentation

Areas of Expertise

Our designs have used RISC, CISC and DSP processors from Motorola, Intel, SPARC, TI, and DEC, with bus structures including VME, Multibus I & II, SBus, ISA, PCI, PCMCIA and custom buses. ASIC technology skills include 0.6 micron geometries, up to 304-pin packages, design for low power-consumption and mixed 3/5V technology. Our software team has source code licenses for six variants of UNIX, including AIX and Solaris, and extensive experience with real-time operating systems such as VxWorks, pSOSystem and LynxOS.

Availability

- Available now.

Contact

Tadpole Technology Inc.

OEM Business Group
12012 Technology Blvd.
Austin, TX 78727
Tel: (800) 232 6656
Tel: (512) 219 2200
Fax: (512) 219 2222
Email: oem-sales@tadpole.com
Web: http://www.tadpole.com:80/Products/oem_boards/powerpc.html

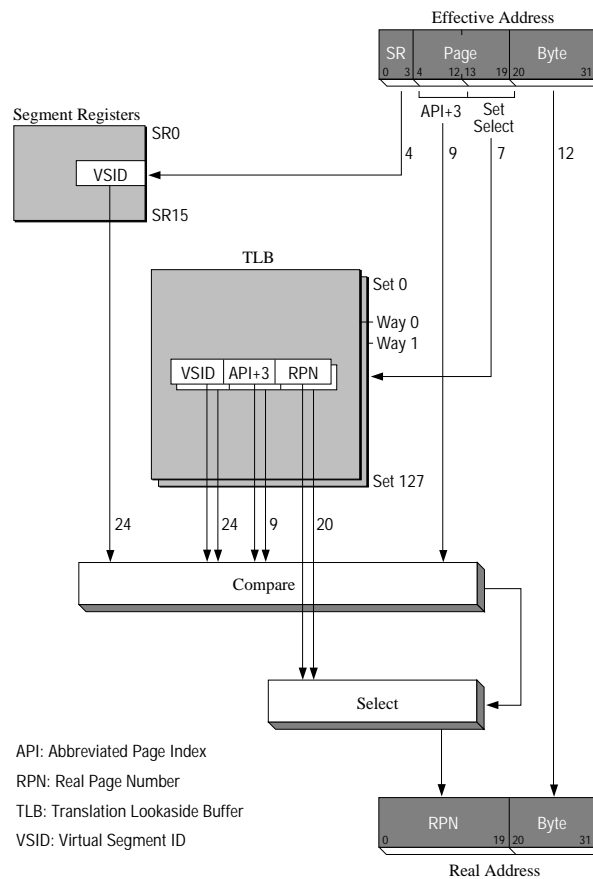
Documentation Services

Consulting Service, Documentation

Warthman Associates

Warthman Associates writes and publishes documentation about microprocessors, programming languages, system hardware and software, and electronic design automation tools. The company has served major clients for 24 years and has over four years of experience documenting products that implement or support the PowerPC Architecture™.

The diagram below, for example, is from a 750-page programmer's manual written and illustrated by Warthman Associates. The diagram shows a 32-bit implementation of a PowerPC memory management mechanism in which a memory access results in a page translation that hits in the translation lookaside buffer (TLB).



Services and Documentation

The code examples below are two of several dozen from the *PowerPC Compiler Writer's Guide*, another example of Warthman Associates' writing. These particular examples convert an integer in register R3 to a floating-

point value in register FR1. The code examples in the book are accompanied by discussions of the PowerPC Architecture and processor implementations that help compiler developers create efficient backend code generators.

Convert 32-Bit Signed Integer to Floating-Point Value

32-Bit Implementation		
# FR2 = 0x4330000080000000		
addis	R0,R0,0x4330	# R0 = 0x43300000
stw	R0,disp(R1)	# store upper half
xoris	R3,R3,0x8000	# flip sign bit
stw	R3,disp+4(R1)	# store lower half
lfd	FR1,disp(R1)	# float load double of value
fsub	FR1,FR1,FR2	# subtract 0x4330000080000000
64-Bit Implementation		
extsw	R3,R3	# extend sign
std	R3,disp(R1)	# store doubleword integer
lfd	FR1,disp(R1)	# load integer into FPR
fcfid	FR1,FR1	# convert to floating-point value

Warthman Associates edits and publishes the hardcopy and Web versions of the *PowerPC Tools* catalog. The company's hallmarks include technical depth, clear writing, illuminating graphics, on-time delivery, and information security.

Services

- *Original Manuscripts and Editing*
- *Graphic Illustration*
- *Turnkey Publishing (Hardcopy, Web)*

Availability

- Available now.

Contact

Warthman Associates
240 Hamilton Avenue
Palo Alto, CA 94301
Tel: (415) 322-4555
Fax: (415) 322-4559

Email: writers@warthman.com
Web: <http://www.warthman.com>

PowerPC Information Resources

Books, Magazines, Electronic Media

Various Vendors

The following resources may be of interest to PowerPC developers. In addition to the books and electronic media listed here, see the section titled "PowerPC Microprocessor User's Manuals" on page 334.

Books

- Title:* **The PowerPC Architecture** (priced)
Editors: Cathy May, Ed Silha, Rick Simpson, and Hank Warren
Publisher: Morgan Kaufmann Publishers, (800) 745-7323
- Title:* **The PowerPC Compiler Writer's Guide** (priced)
Editors: Steve Hoxey, Faraydon Karim, Bill Hay, and Hank Warren
Contact: IBM Microelectronics Division, (800) POWERPC
- Title:* **IBM POWER and PowerPC: Architecture and Implementation** (priced)
Authors: Shlomo Weiss and James E. Smith
Publisher: Morgan Kaufmann Publishers, (800) 745-7323
- Title:* **Inside Macintosh: PowerPC System Software** (priced)
Author: Apple Computer, Inc.
Contact: Apple Computer, Inc., (800) 282-2732 or (716) 871-6555
- Title:* **Inside Macintosh: PowerPC Numerics** (priced)
Author: Apple Computer, Inc.
Contact: Apple Computer, Inc., (800) 282-2732 or (716) 871-6555
- Title:* **Interfacing to the PowerPC Microprocessor** (priced)
Author: Ron Rahmel and Dan Rahmel
Publisher: SAMS Publishing, 201 West 103rd St., Indianapolis, IN 46290
- Title:* **PowerPC Microprocessor Developers Guide** (priced)
Authors: John Bunda, Terence Potter, and Robert Shadowen
Publisher: SAMS Publishing, 201 West 103rd St., Indianapolis, IN 46290
- Title:* **RISC System/6000 PowerPC System Architecture** (priced)
Editors: Frank Levine and Steve Thurber
Publisher: Morgan Kaufmann Publishers, (800) 745-7323

Services and Documentation

Title: **PowerPC and POWER2: Technical Aspects of the New IBM RISC System/6000** (priced)
Author: IBM Corporation
Contact: IBM Microelectronics Division, (800) POWERPC

Title: **PowerPC Programming for Intel Programmers** (priced)
Author: Kip McClanahan
Publisher: IDG Books Worldwide, Inc., (800) 434-3422 or (415) 655-3022

Title: **Optimizing PowerPC Code** (priced)
Authors: Gary Kacmarcik
Publisher: Addison-Wesley Publishing Company, (800) 238-9682

Magazines

Title: **MacTech** (priced)
Publisher: Xplain Corporation
Features: Edited technical articles on Macintosh development in general, including PowerPC platforms.
Contact: (805) 494-9797, Fax: (805) 494-9798, Email: info@xplain.com

Title: **develop, The Apple Technical Journal** (printed and CD-ROM formats) (priced)
Publisher: Apple Computer, Inc.
Features: Edited technical articles on Macintosh development in general, including PowerPC platforms.
Contact: APDA Catalog, (800) 282-2732, (716) 871-6555, Fax: (716) 871-6511

Electronic Media

Medium: **IBM PowerPC Microprocessor Web Site**—WWW on Internet (free)
Provider: IBM
Features: Various resources including latest PowerPC information, products, and technical library.
Contact: <http://www.chips.ibm.com/products/ppc/index.html>

Medium: **comp.sys.powerpc.tech**—Usenet on Internet (free)
Provider: none
Features: Unedited discussion group on PowerPC architecture, system design, and other topics.
Contact: Usenet comp.sys.powerpc.tech

Services and Documentation

Medium: **RS/6000 POWERparallel Systems WWW Server**—WWW on Internet (free)

Provider: IBM

Features: Various resources including library, calendar of events, and service center.

Contact: <http://lscftp.kgn.ibm.com/pps/>

Medium: **Embedded PowerPC Internet Resources**—WWW on Internet (free)

Provider: Eg3 Communications

Features: Links to a variety of Web sites of potential interest to embedded PowerPC developers.

Contact: <http://www.cera2.com/gatoxppc.htm>

Medium: **Developer Services and Products**—WWW on Internet (free)

Provider: Apple Computer

Features: Various resources, some of interest to PowerPC developers, including news, services, products, developer university, and information for international developers.

Contact: http://dev.info.apple.com/du/intro_to_ppc/ppc0_index.html

Medium: **MacTech Web Site**—WWW on Internet (free)

Provider: Xplain Corporation

Features: Technical articles on Mactintosh development in general, including PowerPC platforms.

Contact: <http://www.mactech.com>

Glossary

Each entry in this catalog has been categorized using one or more of the product types defined in this glossary. The product types assigned to each entry may be found beneath the product name on the first page of the entry. Product types are indexed to allow searches for products and services by product type. This glossary also defines terms used as column headings in the Quick-Find Matrix and in the major section names of the catalog's table of contents.

Analyzer—A software or hardware tool that analyzes faults, thermal characteristics, bus timing, logic states, instruction execution, performance, etc.

Analyzer Interface—A device that interfaces an analyzer either to a PowerPC-processor board or to the user of the analyzer.

Application-Specific Tools—Tools designed primarily to support development of products intended for specialized applications and/or markets.

Assembler—An assembler or macro-assembler.

Board—A board for production systems or evaluation, that includes or supports a PowerPC processor.

Books, Magazines—Printed media of relevance to development with PowerPC processors.

Chip—A controller, microprocessor, or embedded microprocessor.

Code—Source code or binary code.

Code Translator—A software tool that translates source or binary code from one language or architecture to another.

Compiler—A native- or cross-compiler for any language, including optimizing compilers.

Consulting Service—Any consulting service other than specific-product support or training. Compare *Training and Support*.

Controller—A device used for I/O, bus, memory or similar control. Compare *Embedded Controller*.

Cross—Of or relating to a tool that supports software generation or system integration on a computer, or in a source language, other than the target computer or source language. This definition encompasses cross-compilers, cross-target system integration tools, and source-code porting tools. Compare *Native*.

Cross-Development Environments (Embedded)—An integrated suite of software tools, typically including a compiler, debugger, and various utilities, that supports software generation and/or system integration for embedded systems, on a computer, or in a source language, other than the target computer or source language. Cross-development environments for desktop (vs. embedded) development are included in the category *Operating Systems and Development Environments (Desktop)*.

Debugger—A source or assembler debugger.

Glossary

- Desktop*—Of or relating to a computer system that uses a general-purpose (i.e., not embedded) microprocessor.
- Disassembler*—A tool that recovers assembly code from binary code.
- Documentation*—Information products such as software or hardware user's manuals and document libraries that are of interest to developers of products based on the PowerPC microprocessor.
- Electronic Media*—Electronic sites, primarily Usenet groups and Web sites, containing information of relevance to developers of products based on PowerPC microprocessors.
- Embedded Controller*—Same as *Embedded Microprocessor*.
- Embedded Microprocessor*—A PowerPC 400- or 600-family embedded microprocessor.
- Emulator*—A design-time or run-time hardware or software tool that mimics (or simulates) functions performed by another type of hardware or software environment. Synonymous with *Simulator*.
- Hardware Development Tools*—Software or hardware tools and accessories for analysis, testing, debugging, modeling or other support for development of PowerPC processor-based boards and platforms.
- Information Resource*—A book, magazine, document, electronic media, or specification.
- Interpreter*—A program that translates and executes each instruction of a source language, such as Java or PostScript, before it translates and executes the next such instruction.
- Libraries*—A collection of functions, calls, subroutines, or data of any type.
- Microprocessor*—A PowerPC general-purpose (desktop) microprocessor. Compare *Embedded Microprocessor*.
- Multimedia Tool*—A tool with special functions for handling high-bandwidth audio, graphics, or video I/O or processing.
- Native*—Of or relating to a tool that supports software generation or system integration for a target computer that is of the same type as the computer on which the tool itself runs. Compare *Cross*.
- Operating System*—Any operating system, including a real-time operating system, kernel or monitor.
- Operating Systems and Development Environments (Desktop)*—Operating systems and integrated software development suites intended for use on desktop computers, and in support of development for desktop platforms.
- Processors and Support Chips*—PowerPC microprocessors, PowerPC embedded controllers, or other controllers and chip sets that support development of PowerPC processor-based systems.
- Real-Time Operating Systems*—Operating systems, intended primarily for embedded systems, that support real-time functionality and real-time development tools. See also *Real-Time Tool*.
- Real-Time Tool*—A software or hardware tool that supports real-time functionality, such as fast context switching, fast interrupt response, prioritized preemptive scheduling, etc.

Glossary

Services and Documentation—Services providing consulting, training, documentation or information products in support of PowerPC-processor based development.

Simulation Model—A pre-defined software representation of processor or other hardware functions.

Simulator—Same as *Emulator*.

Software Generation and Debug Tools—Tools for developing, compiling, debugging, or testing software, without featuring a full, integrated development environment. Compare *Cross-Development Environments*.

Specification—Written statement of functionality or design such as Adobe's Printer Controller Reference Platform and IBM's PowerPC Reference Platform.

Support—A priced service that provides only support for a product. Compare *Consulting Service* and *Training*.

Test Suite—A set of design-testing tools such as boundary-scan test tools, test-pattern generators, and other verification tools.

Training—A priced service that provides training in the use of a specific product. Compare *Support* and *Consulting Service*.

User Interface—A software product in which a graphical user interface (GUI) is a principal function.

Utility—An auxiliary tool such as a device driver, network protocol, editor, I/O subsystem, browser, linker, loader, archiver, version-control environment, etc. that is not otherwise classified by another product type.

Glossary

Sales Offices

A current list of IBM Microelectronics sales offices may be found on the Web at:
<http://www.chips.ibm.com/orders/index.html>

Sales Offices

Index

Numerics

3000 Series Logic Analyzers, 288

A

Absoft C/C++ for AIX, Windows NT and Power Macintosh, 38
Absoft Corporation, 38, 40, 42
Absoft FORTRAN 77 for AIX, Windows NT and Power Macintosh, 40
Accelerated Technology, Inc., 180
Ada Development Environment for AIX Operating System, 68
AdaWorld Cross-Development Environment, 138
Adobe Systems, Inc., 232
AIX for RISC System/6000, 162
AIX SDE WorkBench/6000, 54
AIX Version 4 Licensing, 168
AIX Version 4.2, 166
AIX XL Pascal Compiler/6000, 58
AIXwindows Environment/6000, 164
AMX PPC32 Real-Time Multitasking Kernel, 196
Analyzer Interfaces, 108, 258, 272, 274, 276, 278
Analyzers, 48, 76, 84, 96, 110, 112, 114, 136, 212, 254, 260, 262, 264, 268, 270, 288, 290, 292
Apogee Software, Inc., 142, 144
Apogee-C and Apogee-C++, 142
Apogee-FORTRAN 77, 144
Apple Computer, Inc., 146, 320
Applied Microsystems Corporation, 72
Applied Testing and Technology, Inc., 234
Arnewsh, Inc., 298
ASIC and System Board Design Services, 342

B

BBN Systems and Technologies, Inc., 74, 76
Boards, 112, 298, 300, 302, 304, 306, 308, 310, 312, 314, 316
Books, 348

C

C EXECUTIVE, 194
C for AIX, 150
C Set ++ for AIX, 152
CETIA, Inc./Thomson-CSF, 300
Chorus Systems, 216
CHORUS/ClassiX, 216
Chronology Corporation, 254
CLAS 4000 Logic Analyzer, 264
CMA Universal Development Platform, 302
Code, 158, 174, 176, 244, 246, 250, 312
Code Translators, 114, 118
CodeManager, 64
CodeWarrior, 62
Cogent Computer Systems, Inc., 302
Compilers, 38, 40, 44, 56, 58, 62, 66, 68, 82, 88, 90, 92, 94, 104, 116, 120, 122, 126, 128, 130, 132, 138, 142, 144, 146, 148, 150, 152, 154, 204, 222, 224, 226, 312
Configuration Management Version Control (CMVC), 160
Consulting Services, 322, 328, 336, 338, 340, 342, 344, 346
Controllers, 12, 28, 30, 32, 34, 232, 250, 310
Corelis, 80, 256, 258
Creative Electronic Systems SA, 306, 308
Cygnus Developer's Kit, 148
Cygnus Support, 148

D

DAS/NT, 290
DAS/XP, 290

Index

DAVID Audio/Visual Interactive Decoder, 236
Debugger V2, 60
Debuggers, 38, 40, 46, 52, 54, 60, 62, 66, 68,
72, 74, 76, 78, 98, 100, 102, 108, 110, 112,
116, 120, 122, 124, 126, 128, 130, 132, 134,
136, 138, 142, 144, 146, 148, 154, 180, 182,
188, 192, 194, 204, 212, 216, 220, 222, 224,
226, 228, 268, 280, 288, 290, 292, 312
Design and Prototype Development Services,
328
Diab Data Compiler Suites, 82
Diab Data, Inc., 82
Disassemblers, 60, 108, 114, 272, 278
dli Personal Line Logic Analyzer Family, 260
dli Professional Line High-Performance Logic
Analyzer Family, 262
dli-digital logic instruments gmbh, 260, 262
Documentation, 324, 326, 334, 346
Documentation Services, 346

E

Electronic Media, 348
Embedded Microprocessors, 2, 4, 6, 8, 10
Embedded Performance/Biomation, 264
Embedded System Products, Inc., 182
Emulators/Simulators, 72, 80, 84, 86, 102, 106,
110, 112, 132, 134, 136, 232
Enea OSE Systems, 184
ENVY/*Embedded* Smalltalk, 130
Essentials•Tools•Objects, 146
Eureka Technology, 266

F

FasTrak, 224
FDS-Mate, 248
FirePower Systems, Inc., 310
FirmWorks, 158, 322, 324, 326
FlashICE, 84
FlashPort, 114
Fortner Research LLC, 44

G

GOFAST Floating-Point Libraries, 246
GoldenGate II Core Logic, 34
Gordian, 328
Grammar Engine Inc., 84, 86
Green Hills Ada, 88
Green Hills C/C++, 90
Green Hills FORTRAN, 92
Green Hills PASCAL, 94
Green Hills Software, Inc., 88, 90, 92, 94, 96,
98, 100, 218

H

Hardware Accessories, 294
Hardware Design Services, 336
Harris Computer Systems Corporation, 46, 48,
50, 52, 186
Hewlett-Packard Company, 268, 270, 272,
274, 276, 278, 280
High C/C++ PowerPC Embedded
Development Toolset, 116
HMI-200 Series In-Circuit Emulator, 102
HP 16500 Series Modular Logic Analysis
System, 268
HP 16505A Prototype Analyzer, 270
HP E2449B Inverse Assembler, 272
HP E2455A Preprocessor Interface, 274
HP E2465A Preprocessor Interface, 278
HP E2468A Preprocessor, 276
HP E3477A Processor Probe, 280
HP E3494A Processor Probe, 280
Huntsville Microsystems, Inc., 102

I

IBM Corporation, 54, 56, 58, 104, 106, 108,
150, 152, 160, 162, 164, 166, 168, 170, 188,
330, 332
IBM High C/C++, 104
IBM Microelectronics, 2, 4, 6, 8, 10, 12, 14, 16,
18, 20, 22, 24, 26, 312, 314, 334

Index

IBM Sales Offices, 355
IBM27-82660 PCI/Memory Chip Set, 12
Idealogy: ASIC Design Consultants, 336
IMSL Math and Stat Libraries v3.0, 42
Industrial Programming, Inc., 190
Interpreters, 232, 238, 240, 242, 250
Introduction to RISC and PowerPC, 320

J

JAM, 172
Jasik Designs, 60
JMI Software Systems, Inc., 194
JYACC, Inc., 172

K

KADAK Products Ltd., 196

L

Lauterbach Datentechnik, 110, 112
Libraries, 42, 62, 66, 68, 82, 88, 90, 92, 94,
120, 128, 130, 132, 138, 142, 144, 146, 148,
186, 188, 200, 202, 216, 226, 246, 282, 284
Logic Modeling, 282
Long Trail Reference Design, 314
LS FORTRAN and LS Object Pascal, 44
Lucent Technologies, 114
Lynx Real-Time Systems, 198
LynxOS, 198

M

MacNosy, 60
Magazines, 348
MetaWare Incorporated, 116
Metrowerks, 62, 64
Micro Digital Inc., 200
MicroAPL Ltd., 118
Microprocessors, 14, 16, 18, 20, 22, 24, 26
Microsoft Corporation, 120
Microsoft Visual C++, 120

Microtec, 122, 124, 202, 220, 222
Microtec C/C++ Compilers, 122
Microware Systems Corporation, 126, 204,
224, 236
Modular Multifunction Peripheral Controller
Design, 250
Motorola C/C++ SDK, 128
Motorola Hardware Abstraction Layer (HAL) Kit
for Windows NT, 174
Motorola UNIX SDK PowerPC Edition, 66
Motorola, Inc., 14, 66, 128, 174
MTOS-UX/PPC, 190
MULTI Debug Servers, 98
MULTI Development Environment, 218
MULTI Execution Profiler, 96
MULTI Source Level Debugger, 100
Multimedia Tools, 206, 236

N

NetROM, 72
NightProbe Data Monitoring Tool, 52
NightSim Application Scheduler, 50
NightTrace Analyzer, 48
NightView Source-Level Debugger, 46
Nucleus PLUS, 180

O

Object Technology Inc., 130
OC Systems, Inc., 154
Open Firmware Command Reference, 326
Open Firmware System ROM and Device Driver
Consulting, 322
Operating Systems, 162, 166, 168, 170, 180,
182, 184, 186, 188, 190, 192, 194, 196, 198,
200, 202, 204, 206, 208, 210, 212, 216, 220,
228
OS Open, 188
OS-9, 204
OSE Delta, 184

Index

P

PCI 9060ES, 28
PIPELINE, 238, 240, 242
PLX Technology, 28
PortAsm, 118
Power Firmware System ROM Code, 158
Power Micro Research, 338
Power Micro Research Consulting Services, 338
PowerAda and PowerAda/LynxOS, 154
POWERbench, 54
PowerEM Emulators, 80
PowerEngine VMTR2x and CVME60x, 300
Powerized Systems, 310
PowerPage Level 2, 238
PowerPage PCL 5C, 240
PowerPage PCL 5e, 242
PowerPC 401 CPU Core, 2
PowerPC 401GF Embedded Controller, 4
PowerPC 403GA Embedded Controller, 6
PowerPC 403GA Evaluation Board Kit, 312
PowerPC 403GB Embedded Controller, 8
PowerPC 403GC Embedded Controller, 10
PowerPC 601 RISC Microprocessor, 14
PowerPC 601 VHDL Model, 286
PowerPC 602 RISC Microprocessor, 16
PowerPC 603 RISC Microprocessor, 18
PowerPC 603e RISC Microprocessor, 20
PowerPC 604 RISC Microprocessor, 22
PowerPC 604e RISC Microprocessor, 24
PowerPC 620 RISC Microprocessor, 26
PowerPC Boot Firmware, 176
PowerPC Design and Development Services, 340
PowerPC Design Service, 344
PowerPC Educational Courses, 332
PowerPC Embedded ABI Test Suite (PEATS), 234
PowerPC Information Resources, 348
PowerPC Microprocessor User's Manuals, 334

PowerPC Platform Reference Design, 314
PowerPC Reference Platform Specification, 330
PowerPC Virtual Simulator, 106
PowerTV, 206
PowerTV, Inc., 206
PowerUX Operating System, 186
PPCM 8403 Custom Oriented Processor Board, 308
Precies Software Technologies Inc., 208
Precise Real-Time Executives, 208
Printer Controller Reference Port, 232
PromICE, 86
pSOSystem, 192
PSX, 194

Q

Quad Design Technology, 284
Questa, 340
Questa Consulting, 340

R

Rational Ada, C, C++, 132
Rational Software Corporation, 132
RealTime Craft, 210
Real-Time Tools, 46, 48, 50, 52, 108, 116, 124, 126, 134, 138, 180, 182, 184, 186, 188, 190, 192, 194, 196, 198, 200, 202, 204, 206, 208, 210, 212, 216, 220, 224, 228, 236, 244, 272
RIO2 Line of Target Platforms, 306
RISCWatch, 108
RTPC 8067 Development Platform, 306
RTXC, 182

S

Sand Microelectronics, Inc., 286, 342
SBC-403, 304
SBC603, 298

Index

SCANTEST, 256
Signal Integrity Analysis Tools, 284
Simulation Models, 106, 266, 282, 286
Simulation Models for PowerPC Bus Interface,
266
SingleStep, 134
SmartModel Library, 282
smxPPC, 200
Softex, 176
Software Development Systems, Inc., 134, 226
Specifications, 174, 330
SPECTRA, 220
STEP Engineering, 136
STEP Exceed-400, 136
SuperTask!, 212

T

Tadpole Technology, 344
TECSI S.A., 210
Tektronix, Inc., 288, 290, 292
Test Suites, 108, 174, 234, 256
Thermal Management Solutions, 294
Thermalloy, Inc., 294
Thomson Software Products, 68, 138
TimeScan, 76
TimingDesigner, 254
TLA500, 290
TLS216, 292
TollGate/VAS 96021, 32
Tornado, 228
Total Freedom, 316
Total Impact, 316
Total Power NuBus, 316
Total Power PCI, 316
TotalView, 74
TRACE32 BDM/ROM Debugger, 110
TRACE32-ICE, 112
Training, 320, 332

U

U S Software, 212, 244, 246
UDB, 78
UI-MPC601 Universal Interface, 258
Ultra C/Ultra C++, 126
User Interface, 218
User Interfaces, 50, 164, 248
USNET, 244
Utilities, 38, 40, 54, 62, 64, 66, 68, 72, 82, 88,
90, 92, 94, 104, 108, 116, 120, 122, 128, 130,
132, 138, 146, 148, 154, 158, 160, 166, 172,
174, 180, 186, 188, 192, 194, 196, 204, 206,
208, 216, 218, 220, 222, 224, 226, 228, 236,
244, 248, 312

V

V3 Corporation, 30
V400PBC, 30
VLSI Technology, 32, 34
VRTX/OS, 202

W

Warthman Associates, 346
w-CUBE Software Corporation, 248
Wind River Systems, Inc., 228
Windows NT, 170
Writing FCode Programs for PCI, 324

X

Xionics Document Technologies, Inc., 250
XL Fortran for AIX, 56
XRAY Debugger, 124
XRAY MasterWorks, 222
