A Look at Boundary Scan From a Designer's Perspective

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Abstract

Much attention has been focused in the past on the benefits of boundary scan to the manufacturing test process and the test engineer. While ultimately the decision to use boundary scan in a given project should be based on positive impact to product life-cycle cost, the benefits that accrue to the designer are often overlooked. This paper describes such benefits to designers at all levels of product design: chip, board, system. It also provides insight into special considerations for the designer who implements or uses boundary scan.

Background

Beginning in 1985, several European and North American companies banded together to form the Joint Test Action Group (JTAG). Their stated task was to solve the problem of printed-circuit board (PCB) manufacturing test, which was growing more difficult as integrated circuits (ICs) became smaller and more complex (Figures 1 and 2).[1,2] Their solution was eventually standardized as the IEEE Std 1149.1-1990 Test Access Port and Boundary-Scan Architecture. This standard provides for inclusion of required test resources into ICs themselves.[3]

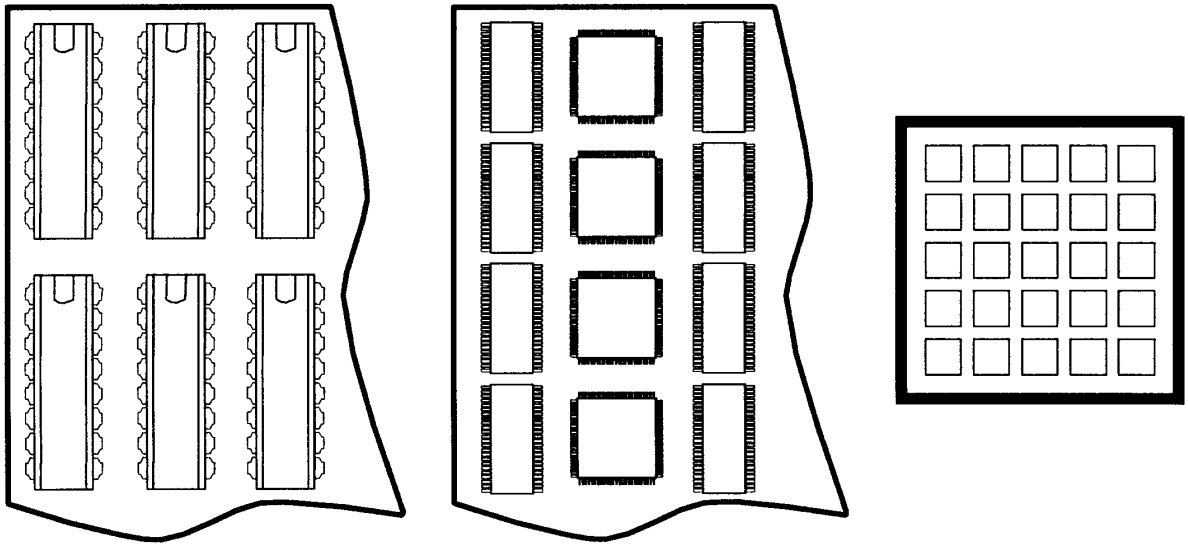

Figure 1. The Incredible Shrinking Board Results in Loss of Test Access

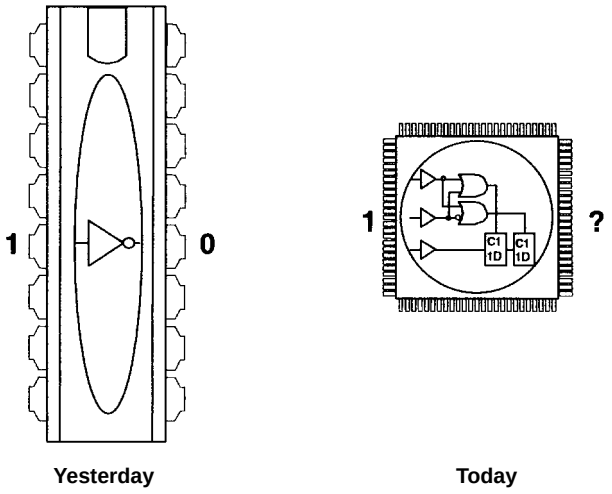

Figure 2. Increasing Integration at Chip Level Complicates Controllability

Manufacturing test of PCBs is essentially an effort to find defects (such as net-to-net shorts and solder opens) in the assembly of ICs and other components onto a board. This effort is obviously made more difficult by ICs that are both smaller and more complex. The ability of functional ("edge-connector") test to isolate PCB assembly defects to an adequate level is quickly thwarted by increased board functional density (Figure 3). Since only the primary input/output are used for the test, the difficulty of test generation and the requisite test length grow dramatically as the board complexity increases.[1,2,4]

In-circuit ("bed-of-nails") test, which was an earlier attempt to improve fault isolation in complex boards, is likewise thwarted by increased IC functional density and, further, by physical constraints (Figure 3). Since in-circuit test is based on the physical probing of (preferably all) nets internal to a PCB, smaller pin-to-pin spacing requires improvements in probe technology that are becoming increasingly more difficult and costly. In many cases, such as multichip modules (MCMs), ball-grid arrays (BGAs) and buried signal traces, physical access to internal nodes is not possible at all. Increased functional complexity of ICs causes problems because, in order to place IC outputs in known states for continuity test, the function of the device must be manipulated by often long and complex pattern sequences at IC inputs. A similar argument holds for continuity test at IC inputs.[1,2,4]

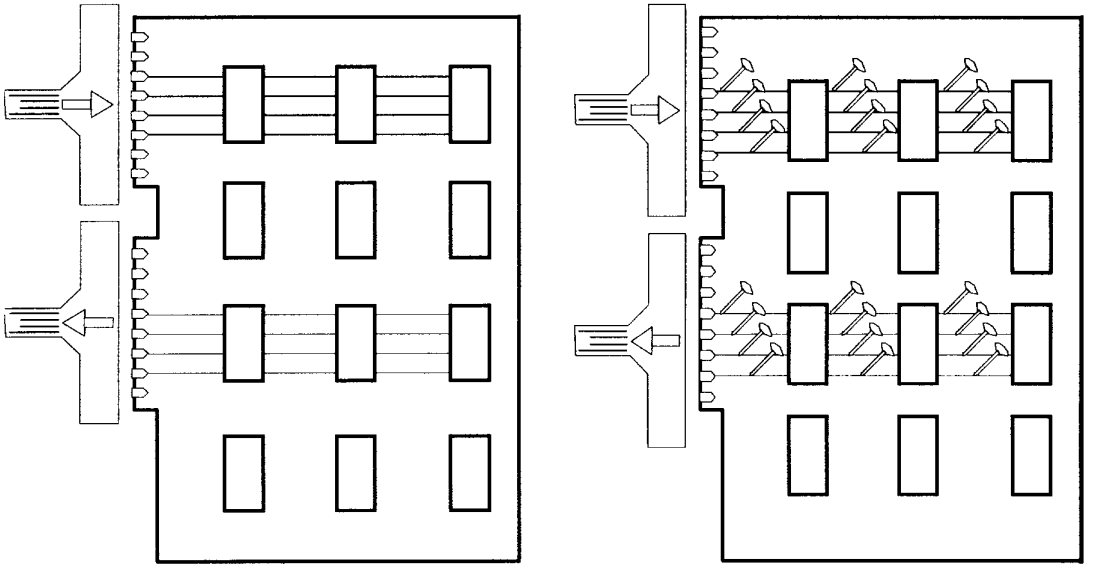

Figure 3. Traditional Methods of Board Test

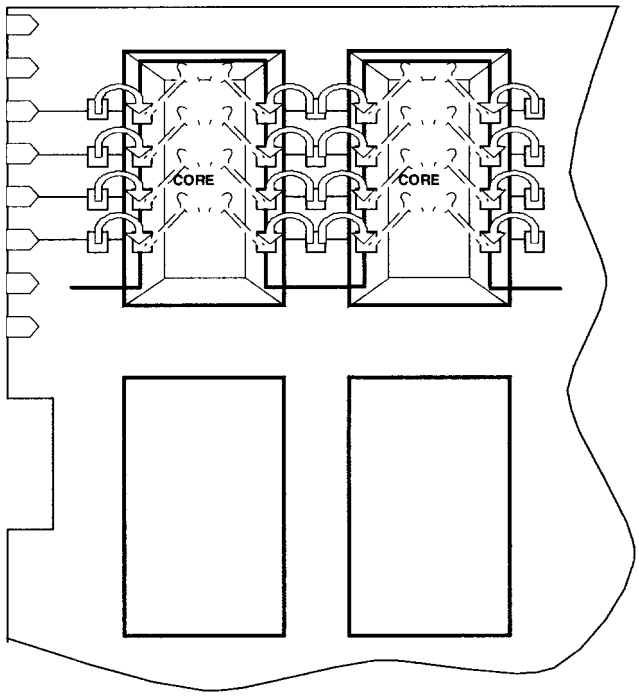

Figure 4. The Boundary-Scan Idea

The boundary-scan idea builds on the concepts of in-circuit test. However, physical probes ("nails"), which are placed mid-net, are replaced by boundary-scan cells (BSCs). These "virtual" probes are placed on-chip at IC inputs and outputs (the boundary of the IC), and are therefore placed at the net ends (Figure 4). This results in two major improvements: (1) physical access is no longer required at boundary-scan nets, and (2) continuity test is no longer subject to IC complexity. The net effect is that the goal of manufacturing test, to isolate defects in assembly process to a pin or net, can be accomplished by highly automated test-pattern generation (ATPG).[2]

Finally, in order to provide a means to arbitrarily control and observe these BSCs with minimal pin overhead, the BSCs are designed such that they can be serially concatenated to form a shift register between two IC pins, Test Data Input (TDI) and Test Data Output (TDO). The additional control structures required to select between normal and test operational modes have also been designed to minimize pin overhead and to maximize flexibility to handle test modes in addition to that used for PCB manufacturing test (Figure 5). This Test Access Port (TAP) is based on a state machine (TAP Controller) that operates synchronously to a Test Clock (TCK, to which all operations of the test logic are synchronous) and under the control of a single Test Mode Select (TMS). The TAP Controller explicitly provides for a single instruction register that controls the test modes and for any number of test data registers (including the boundary-scan register) that can be selected by specific instructions.[2]

Standardization of the TAP and TAP Controller, as well as the boundary-scan architecture, has been key to the broad acceptance of the technology across IC, tester, and computer-automated engineering (CAE) tool vendors. Thereby, this structured design-for-test (DFT) technique may be used widely across all types of board designs by all sorts of board manufacturers, even those where catalog ICs and off-the-shelf testers and tools must be used. Additionally, the flexibility of the TAP and TAP Controller allows them to be used for access to other test features built into chip, board, or system, such as on-chip scan test or built-in self-test (BIST).[2]

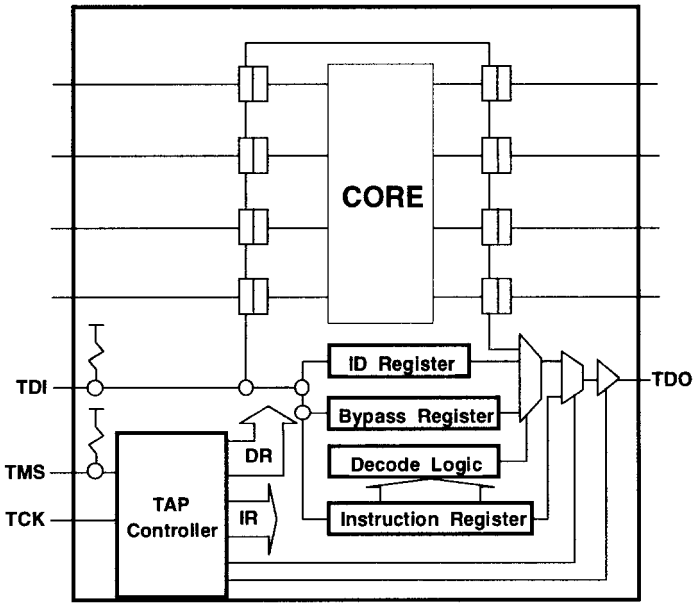

Figure 5. The Boundary-Scan Control Architecture

Use of the Standard by the Board Designer

Since the standard has been designed primarily with board-level (test) concerns in mind, we can expect many benefits for board designers. Although many designers might deny it, they do perform at least one critical "test" operation: design verification/debug. And, just as board manufacturing test benefits from increased observability and controllability, so does board design "test" (that is, verification and debug). Boundary scan, along with other DFT techniques applied at chip or board level, can greatly aid these design test functions.

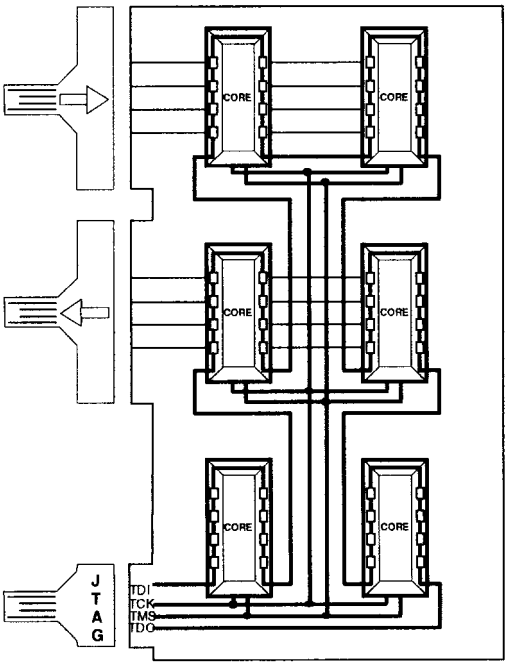

Figure 6. Board-Level Boundary-Scan Path

As in the case of manufacturing test, these benefits are derived in two fashions. Where boundary-scan access is provided, observability and/or controllability of a net may be obtained without concern for the function of the driving and/or receiving ICs. Also, no physical access to the board under test is required (Figure 6). One result is that inexpensive test equipment can be used, since tester channels are needed only for the TAP and other primary I/O ("edge connector") signals. Another, perhaps more important result, is that design test can proceed even in cases where physical access to board internal nodes is difficult or impossible (due to board physical characteristics or operating environment[5]).

In the design CAE environment, the designer could have virtually any desired level of observability and controllability to board-internal and (in case of ASICs, FPGAs, or PLDs) chip-internal nodes. With the appropriate boundary-scan and chip-internal scan facilities, the designer can enjoy this same level of access to such nodes in the prototype. Further, a structural ("assembly") test of the prototype can be generated that can be applied from this inexpensive test equipment and without need for expensive test fixturing. Such a test can be automatically generated, given the board netlist and descriptions (in the boundary-scan description language, BSDL) of the boundary-scannable devices. This simple test is available even when manufacturing test program, equipment, and fixtures are not (as is most often the case for prototypes, since they are difficult to provide for an unproved design). Such a test can save many frustrating hours (a testimonial indicates a reduction from 6 weeks to only 2 days[6]) which would normally be required to separate assembly problems from design problems. This is especially important if new and unproved assembly processes have been developed for the board.[5,7,8,9,15]

In some cases, the provision of boundary scan and DFT can permit some prototype testing to begin even in the absence of "key" components. For example, if a processor board were designed with proper planning, associated memory could be tested by emulating the processor, or vice versa.[10]

In addition, the actual design time and manufacturing cost of PCBs may be reduced by elimination of test points.[7,11] If enough test points can be eliminated (one example cites a reduction from 40 down to 4[6]), then possibly some PCB layers can be eliminated as well, which might greatly decrease PCB cost. In some cases, such elimination of test points may be critical to the very miniaturization goal that drives the choice of extremely dense packaging options such as BGAs.[6]

The board designer can obtain these benefits by specifying the use of boundary scan in proprietary ASICs and by placing boundary-scannable catalog (including user-programmable) components wherever possible. The task of finding such components is becoming less difficult daily as the number of such products grows. As of this writing, it has been reported that boundary scan is supported by 22 ASIC vendors, 24 vendors of over 120 standard components and 12 vendors of user-programmable logic (Figure 7).[12]

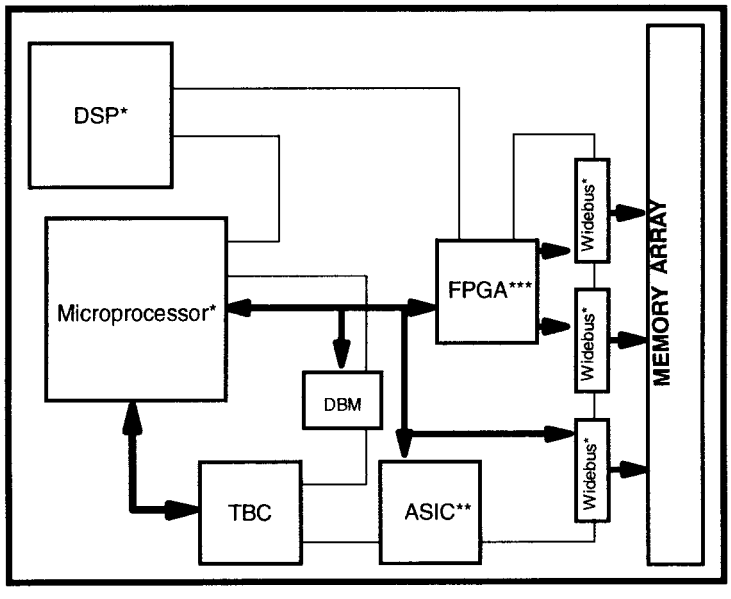

Figure 7. IEEE 1149.1 in Action

Included in such offerings are boundary-scannable bus interface devices. These reasonably inexpensive components can replace their nonscan counterparts to gain all the above benefits. It may be useful in some cases to insert such devices even where they are not required for normal system function (for example, in parallel to a bus that is not boundary-scannable for performance reasons) in order to improve test access.[13] Often such components may bound simple clusters of nonscannable logic that can be tested using the "virtual nails" of these devices for simple "virtual" in-circuit testing (Figure 8). Additionally, some vendors offer built-in parallel-output pattern generators and parallel-input signature registers that allow the board designer to implement board-level BIST capabilities that provide high fault coverage with very little test pattern generation.[7,14]

In designing the board-level scan chain, a single, simple scan chain is recommended.[4,15] Simple buffering of the TCK and TMS signals should be used, and care should be exercised in the routing, termination, and timing of these signals.[4,10,14] In the prototype, all TAP signals should be checked for signal integrity at their destinations.[10] Failure to maintain signal integrity at these signals may cause improper movement of the TAP controller and premature or unintended entry of device(s) into test modes, such as EXTEST. In such modes, the outputs of the device(s), which would be controlled from the boundary-scan register, might come into contention with those of other scannable or nonscannable devices. In general, the board designer must beware of conditions in which scannable and nonscannable drivers might be in conflict.[4]

Another key to obtaining such benefits will be access to enabling CAE tools. As of this writing, it has been reported that 14 CAE vendors supply tools that support boundary-scan test.[12] These tools fall roughly into three classes: boundary-scan insertion, access analysis, and boundary-scan ATPG. The topic of boundary-scan insertion, since it is a chip design activity, will be discussed later.

Access analysis tools examine board designs prior to layout for nets to which physical test access is not required. Such tools will identify nets in at least three categories: pure boundary-scan (all connected devices have boundary scan), mixed boundary-scan (some, but not all connected devices have boundary scan), and nonboundary-scan (no connected devices have boundary scan).[16] These nets will then be prioritized (in the stated order) for test-point elimination. Such information is then passed to a layout tool (or designer) for elimination of the test points, as required for optimal board layout and fabrication cost.[17]

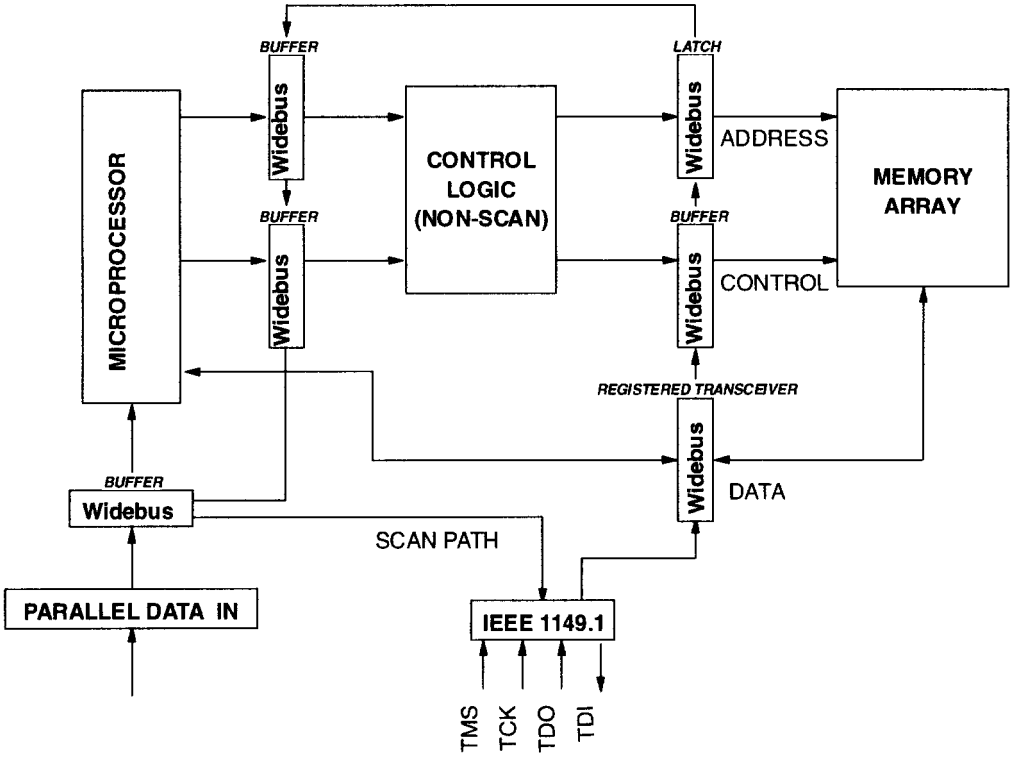

Figure 8. Logic Cluster Test

Boundary-scan ATPG tools automatically generate prototype or manufacturing tests to be applied to the board under test using the board-level TAP. Some of these tools can consider physical access (via in-circuit "bed-of-nails") as well. The best-in-class tools of this type will generate tests for TAP and BSDL validation, and board-level scan-path integrity. These tests, in combination, verify the infrastructure for applying remaining tests. The best-in-class tools generate the following additional types of test for board structural test: boundary in-circuit, virtual interconnect and interactions, and virtual cluster/component test. Boundary in-circuit test uses physical access, but utilizes boundary-scan for simple access to on-chip inputs and outputs for reduced test generation time and complexity. Virtual interconnect and virtual cluster/component tests allow for removal of some or all physical access for test of interconnect and of nonscannable logic clusters, respectively. Such tests will include diagnostics of board assembly faults to the pin. Some tools support multiple board-level scan chains, while others support only a single chain.[6,12,16,17,18]

Some means of boundary-scan test application is required. In some cases, this may be in-circuit or board-functional test equipment that is already owned, perhaps with some modifications to handle deep serial patterns. In other cases, it may be an inexpensive test adapter for PC or workstation. Such "testers" must, at a minimum, exercise the board-level TAP(s) under control of a simple vector file. In either case, to get the most out of boundary scan in design debug, an interactive scan-based diagnostic capability is desired.[10]

The best scan-based diagnostic tools will use a scan-path management database that permits interactive view and control of only those portions of the board (pin, register, bus, or user-defined signal group) that are of interest (Figure 9). Such tools completely hide the complexity of the TAP protocol and boundary-scan chain from the user and allow efficient design debug in the fashion of parallel stimulus generators and logic analyzers to which the design engineer is accustomed. In fact, the best such tools include logic-analyzer-like waveform and state table displays.[19]

Such tools should also support multiple test vector generation methods: interactive, CAE parallel (with automated serialization), and boundary-scan ATPG (based on a standard interchange format such as the Serial Vector Format, SVF). They should also describe the boundary-scan hierarchy using industry standard formats such as BSDL, the Hierarchical Scan Description Language (HSDL), and EDIF (Electronic Design Interchange Format) netlist. And, they must be sensitive to board-level constraints so that physical damage to the board, which might result from improper control of boundary-scan drivers, does not occur.[19]

Finally, they must support scan test and test reuse across all product phases. This means they must allow access to chip-internal scan and BIST, as well as board-level BIST capabilities. They must provide a flow of test information from chip to board to system. Ideally, they will provide a flow to embedded system test, enabling system built-in test based on reuse of scan-based test.[10,19]

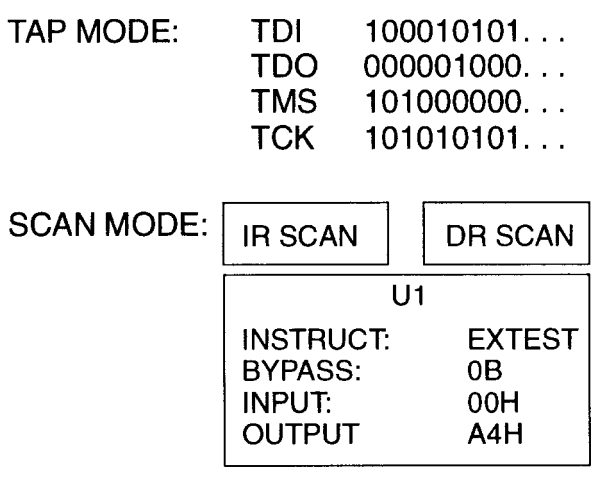

Figure 9. Scan-Path Management

Use of the Standard at Chip Level

At chip level, the standard provides most benefit in its provision for a standard test access method (the TAP) which allows access to chip-internal test facilities in addition to the required boundary-scan test facilities. Such chip-internal test facilities include internal scan path, BIST, and built-in emulation and debug.[5,7,8,10,17,20]

Chip-internal scan path involves the substitution of normal storage elements (latches and flip-flops) with scannable counterparts that can be serially interconnected for test purposes. In a full-scan approach, all such storage elements are replaced, and the circuit is thereby partitioned into blocks of combinational logic between parallel inputs and outputs of a simple shift register. Robust combinational ATPG algorithms can then be used for rigorous structural test of the chip logic. Partial scan implies the replacement of only selected storage elements. It is used in cases where chip area and performance cannot be traded-off for improved fault coverage. However, since not all storage elements are scanned, some sequential ATPG must be used. The failing of such ATPG to provide adequate fault coverage is the primary reason for adopting chip-internal scan in the first place.[21]

BIST uses on-chip stimulus generators and response monitors to eliminate the need for any test generation. Most commonly it uses pseudo-random pattern generation and signature analysis (cyclic redundancy checking) implemented in linear-feedback shift-registers (LFSRs). In such cases, care must be taken that the circuit to be tested is not resistant to pseudo-random techniques. Where the circuit is not suitable for pseudo-random techniques, deterministic BIST methods are possible.[22]

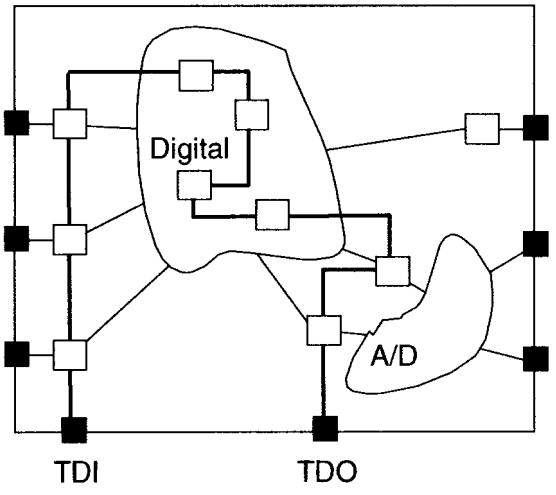

Figure 10. Boundary Scan Plus Internal Scan in Mixed-Signal Circuit

Such features are often most powerful when used in combination. For instance, if boundary-scan and chip-internal scan path are both implemented so that they may be used simultaneously in a given IC, then static test application requirements can be reduced to only the four TAP signals, since the boundary-scan register can control/observe the primary inputs/outputs to the core logic (Figure 10).[22] If internal scan path is combined with BIST, the BIST may be used for quick pass/fail testing while the internal scan is used for chip debug and failure diagnosis. Additionally, if a standard RUNBIST capability is provided, the end user may perform quick function testing while the IC is in-system.[23]

Finally, boundary scan alone can reduce test access requirements to the TAP only. The same static functional vectors that would be applied by an expensive IC tester with many parallel channels can be applied through boundary scan (if INTEST capability is provided). Setup of ICs for parametric test can also be facilitated by boundary scan. And boundary scan can be used in hostile environments where physical access is difficult or impossible.[5] For mixed-signal ICs, inclusion of boundary scan can provide a very useful partitioning of analog and digital functions, allowing each to be tested independently (Figure 10).[24]

To benefit from these capabilities, they must be designed into the chip. Several types of CAE tools can aid this process. Most such tools provide for some level of automation of internal (full or partial) scan, BIST, and boundary scan. The abstraction level at which these tools operate ranges from register-transfer level down to gate level, and the point of use ranges from pre-synthesis to post-synthesis (or schematic capture). In the area of internal scan insertion, the best tools will provide full scan insertion and partial scan insertion driven from chip area, performance, and test coverage constraints. They will also provide the combinational and/or sequential ATPG needed to capitalize on the scan path.[6,12,21]

Boundary-scan insertion tools are similarly varied. Capabilities to look for besides automated insertion of TAP and boundary-register are BSDL output, test pattern generation for standard-conformance checking and BSDL validation. Some tools use BSDL (or graphical entry) as an input, rather than an output, to the boundary-scan insertion process.[18]

The need for validation of BSDL and TAP integrity cannot be overstated since the entire test infrastructure is based upon proper operation of these components.[4,17] Special attention should be given to TAP pin placement and to considerations for proper clocking of internal scan path relative to boundary-scan path.[4,25]

Use of the Standard at System Level

Finally, the standard can bring benefits to design at system level also. Such benefits are primarily derived from the ability for TAP-accessed tests to be reused at higher levels of product integration, from chip to board to system.[1,7] These capabilities may be used for system hardware debug and hardware/software integration while chips and boards are in their normal system configuration and operating environment. Since no physical access is required, use of "extender" cards, complex connectors, and large environmental control systems is not needed.[5,7,8]

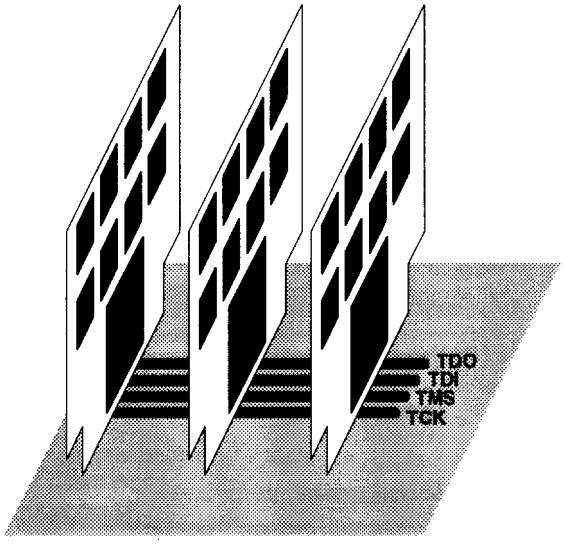

Figure 11. Multidrop System TAP

Additionally, boundary scan and other TAP-accessed test facilities may be useful in meeting system design requirements for built-in test, field service test, and remote diagnostics. Clearly, in most such cases it is desirable to limit the expense and complexity of test equipment required. Boundary scan can facilitate this by limiting test access and control requirements to an inexpensive diagnostics port (the TAP).[7,20]

Boundary-scannable bus interface devices can be useful in these applications, as well, by partitioning the system along field-replaceable unit (PCB) boundaries. Also, if the backplane interface of PCBs is scannable, then backplane connectivity and integrity testing can be performed. By using the previously mentioned pattern generation and signature analysis techniques, it is even possible to perform gross performance testing on the backplane.[14]

One problem in the area of system implementation of TAP access is referred to as the multidrop problem (Figure 11). Since TDI and TDO are serial terminals, they must be daisy-chained in simple chains. This "ring" configuration presents a problem in backplane-oriented systems, since some boards may be removed, disabling the scan chain. An alternative, proposed by the standard, is the "star" configuration which allows TDI and TDO pins on PCBs to be bussed.[3] However, since multiple TMS signals are required to prevent simultaneous scanning (and thereby contention on TDO bus) of PCBs, many backplane routing channels are required. Several alternative multidrop schemes, based on serial addressing techniques, have been proposed to alleviate this problem. The best of these techniques will enable multidrop routing of backplane signals, with minimal need for test reformatting and minimal impact on test application time.[1,4,6,7,20,26]

Conclusion

We have discussed many benefits that are available to designers through use of the Test Access Port and Boundary-Scan Architecture. These benefits are primarily in the area of design verification and debug and are enabled by improved controllability and observability into circuits, and freedom from physical access constraints provided by boundary scan. While some effort is certainly required to derive such benefits, a suite of CAE tools that reduces such effort has been presented. Designers at all levels of product integration (chip, board, system) are encouraged to evaluate boundary scan for benefits that they and their companies may derive from its use.

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