Partitioning Designs With 1149.1 Scan Capabilities

Steve Altaffer
Texas Instruments Incorporated

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Introduction

Typical 1149.1 Scan Architecture Descriptions

Star vs. Scan path system scan designs addressed in IEEE 1149.1 use either a single scan path, employing a common mode line and daisy-chained data (scan path), or separate mode lines to individually controlled independent rings and common TDI/TDO signals (star). Figure 1 depicts each configuration. Each can have advantages over the other depending on applications and design requirements.

The reduced path lengths of a star configuration simplify the scan controller design since each scan path is shorter than if the entire system were connected on a single scan path. Although the same amount of data may be necessary to control the entire system, the overhead of tracking unused elements in the scan path for a particular test is reduced. The star configuration is usually recommended for systems that require individualized control over independent functions or shorter scan-path lengths to simplify the scan controller design. The star configuration also has an inherent fault tolerance as an advantage. Because each of the rings in a star configuration is isolated from the system, a fault within the scan path itself does not corrupt the entire system scan path as would be the case in a scan-path configuration. A multi-board system employing a scan-path configuration has the ability to control all of the elements in a scan path regardless of the board on which they are located. A system that is backplane bus intensive or has functions spread across board boundaries would most likely employ a scan-path configuration to simplify board boundary and functional testing.

Scan-Path Linker (SPL) and Scan-Path Selector (SPS) Overview

Theory of Operation

The scan ring family of devices (SPS and SPL) provide the ability to create a hybrid star-scan-path architecture in a system while maintaining the advantages of both. The devices can be used to bypass an entire scan path on a board or select up to four independent rings (SPL) on the board. A single scan path can be selected and scanned or a combination of rings can be linked together in series, depending on the scan ring support device being used. Figure 2 depicts the SPS as it would be connected in a system.

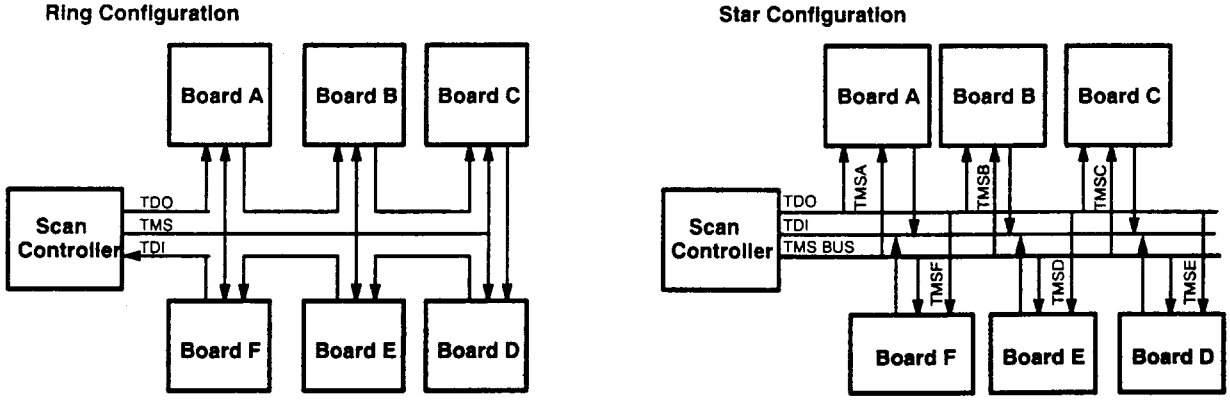


Figure 1. Ring and Star Configurations

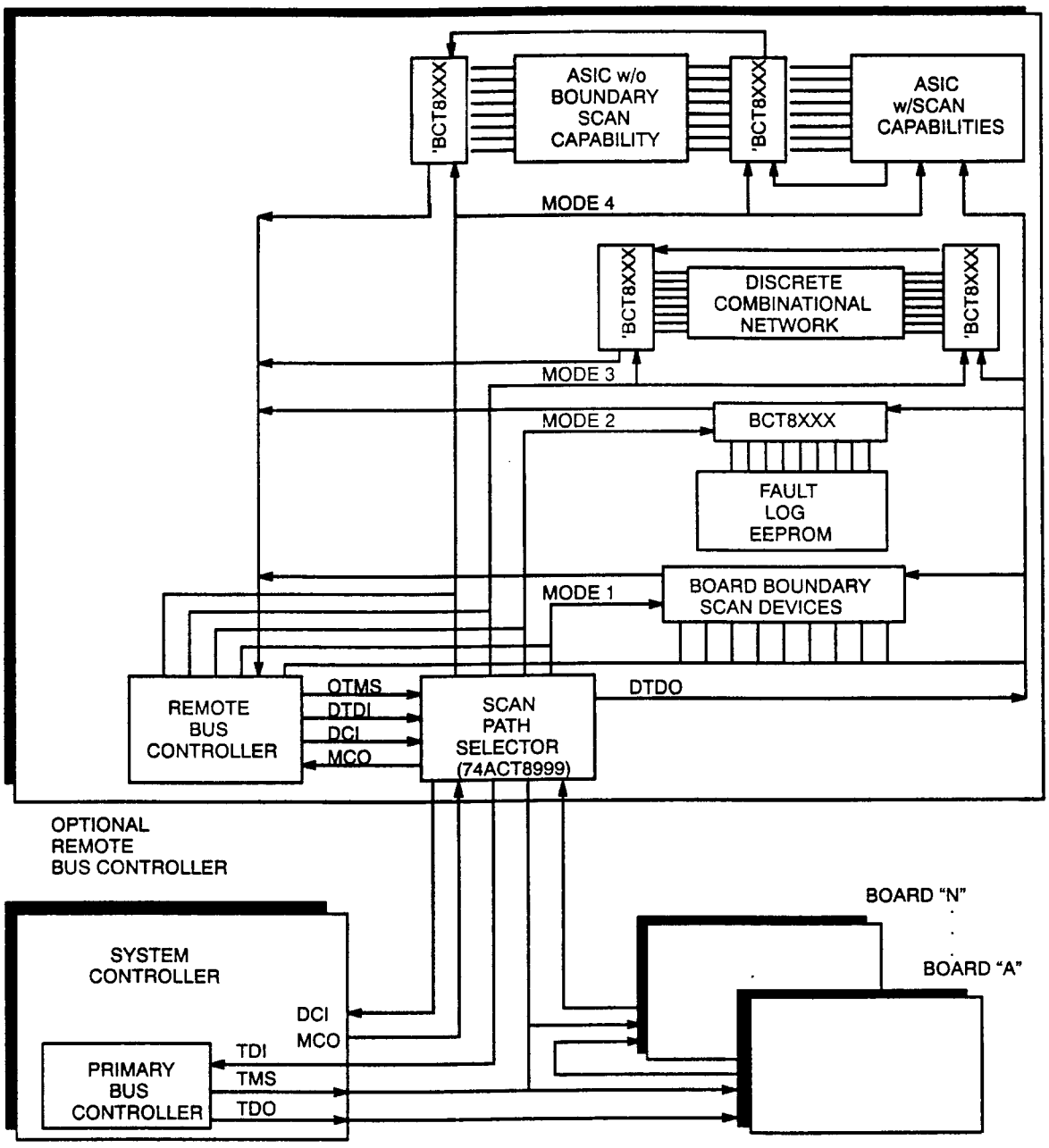


Figure 2. SPS System Scan Design

Note that each board is in a scan-path configuration while internal to the board, a star configuration is created by the SPS. A feature of the scan ring support devices is the ID bus that uniquely identifies a board to a system controller. The ID bus in the SPS (SN74ACT8999) also serves as a bidirectional data bus (BiD), capable of communicating with a remote bus controller or other on-board controller through the scan interface.

The 'ACT8999 also has a remote controller input that can be used to share the board's scan buses between the Primary Bus Controller (PBC) and a Remote Bus Controller (RBC) on the board. The remote input can select any of the four scan rings on a board while maintaining the primary path through the device to the rest of the system. In order to properly handshake with the board for remote-control handoff, ID bus operation,

or status/interrupt capabilities, a four-wire status bus is included in the devices. Those wires are labeled Master Condition Input (MCI), Master Condition Output (MCO), Device Condition Input (DCI) and Device Condition Output (DCO). The DCI pin also serves as the clock input to an 8-bit internal programmable counter. Properties such as the polarity of the clock, up/down counting, and latch-on-zero in the countdown mode are all programmable. The DCO pin can serve as the terminal count (MAX/MIN) output to allow cascading or interrupting the scan controller.

Select Register Operation

The SELECT data register is an 8-bit control register that determines the output of each of the DEVICE TEST MODE SELECT (DTMS) signals (2 bits per output). The select decoding for a single DTMS is shown in Table 1.

Table 1. Select Register Decoding

Select Bit MSB	LSB	DTMS Output
0	0	High (STRAP)
0	1	Low (IDLE)
1	0	OTMS *
1	1	TMS

* For devices without OTMS input, TMS is transferred to DTMS.

It is the same for each of the other DTMS outputs. For the case of a scan-path device not having an OTMS (remote) input, the device will route the primary TMS to the selected DTMS output. When an output or outputs are selected to convey TMS, the scan-path device waits until the primary TMS enters the IDLE state before multiplexing the TMS and TDI to the secondary scan path. This ensures proper state synchronization between the primary and board scan path(s) with respect to the TAP controllers on each. Any other means to "open" a secondary scan path would result in scan-path corruption and asynchroneity of data and control, and therefore is not allowed within the scan-path device hardware. This must be clearly understood by the software or firmware controlling the scan-path device so that the hardware is configured as the software believes it is. Referring to Figure 3, when a secondary scan path is opened, the TMS is driven directly to the output with internal delays only. Due to the routing of the data path directly from TDI to DTDO, it is necessary to sample the data on the rising edge of TCK and output to the secondary scan paths on the falling edge of TCK to comply with IEEE 1149.1 specifications. This creates an extra bit of data in the path whenever an external scan path is selected, but it is necessary to ensure data synchronization to the rings at high TCK frequencies. This sync bit will be present in all data and instruction scans and must be recognized by the scan bus controller whenever a secondary scan path is opened. The data from the scan path is then fed to the "normal" input of the scan-path device data or instruction registers and output to the primary scan path. For the SPL (SN74ACT8997), much the same data path is created.

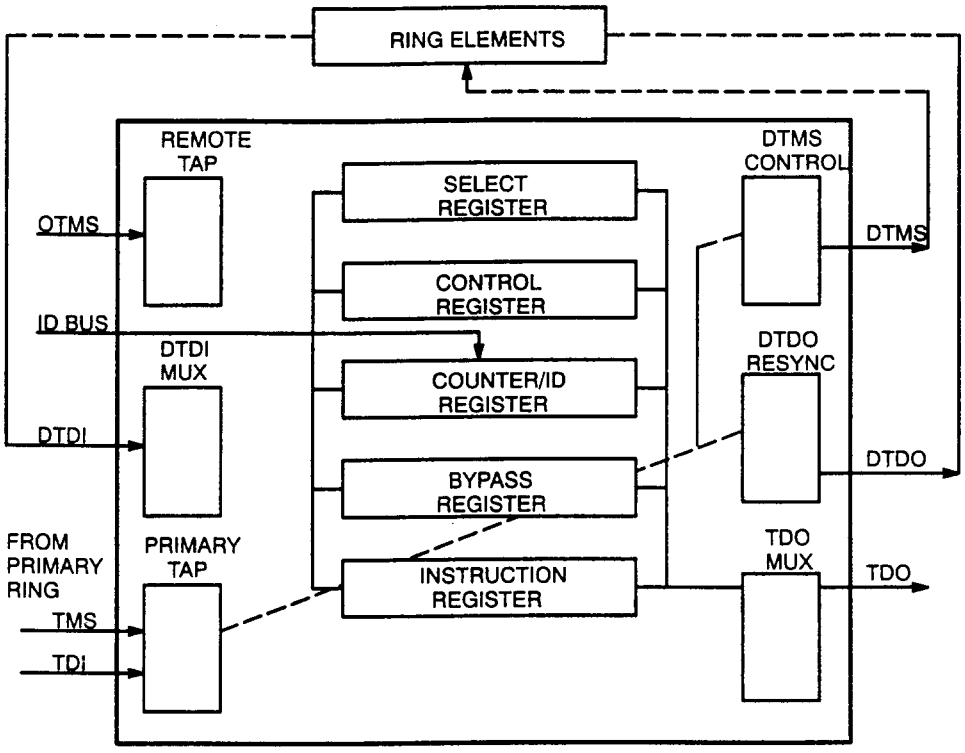


Figure 3. Scan-Path Selector (SPS) Scan-Path Ring with Ring Selected

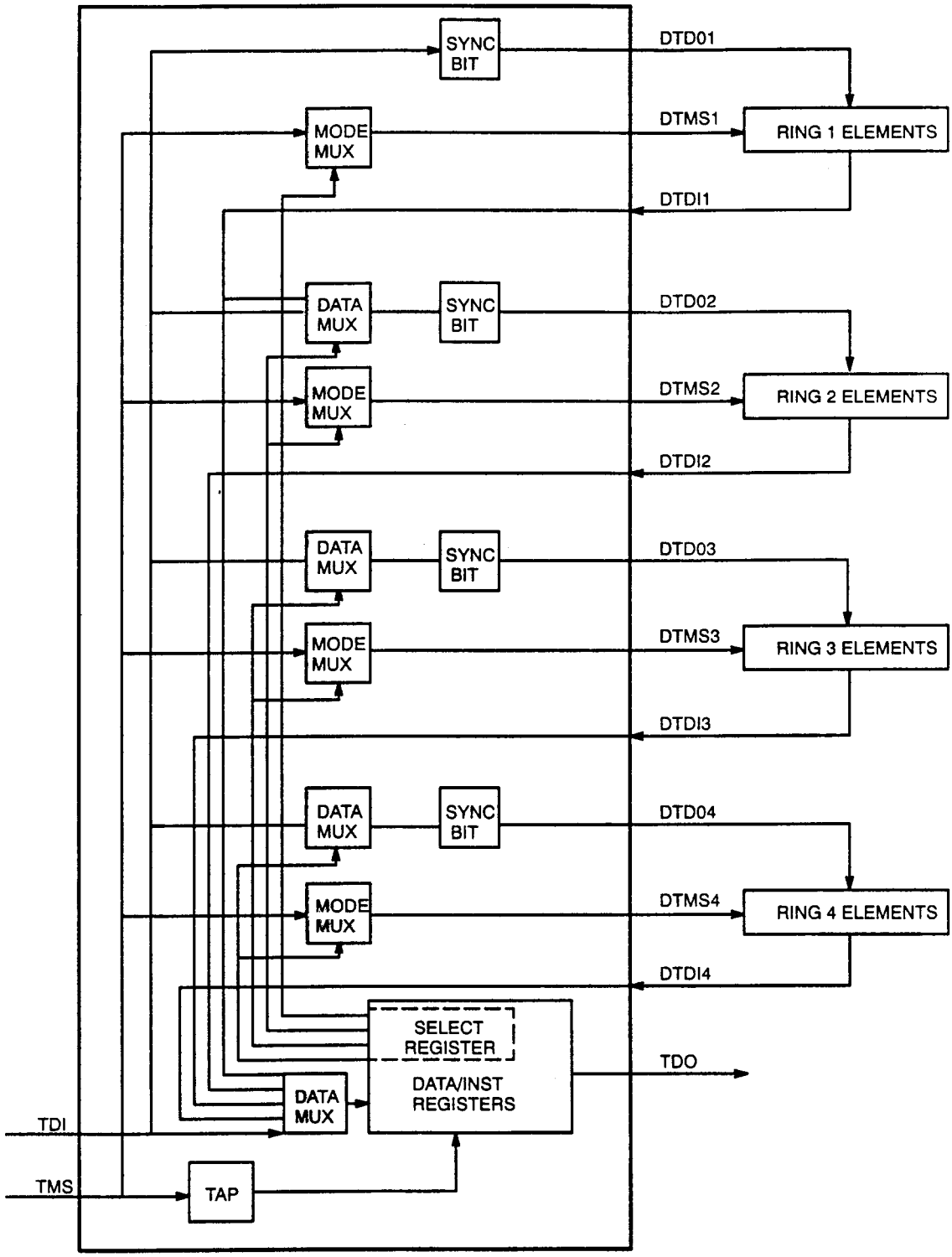
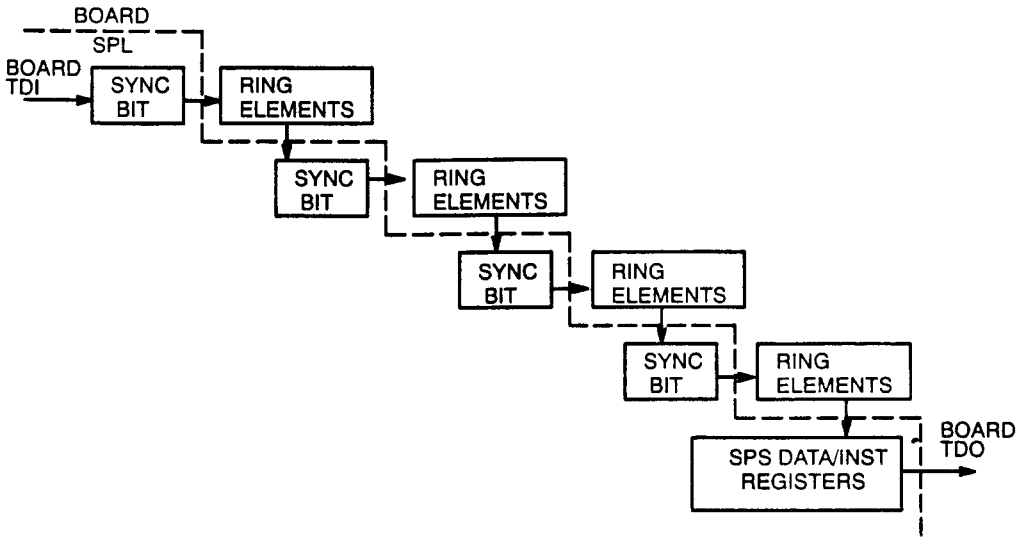
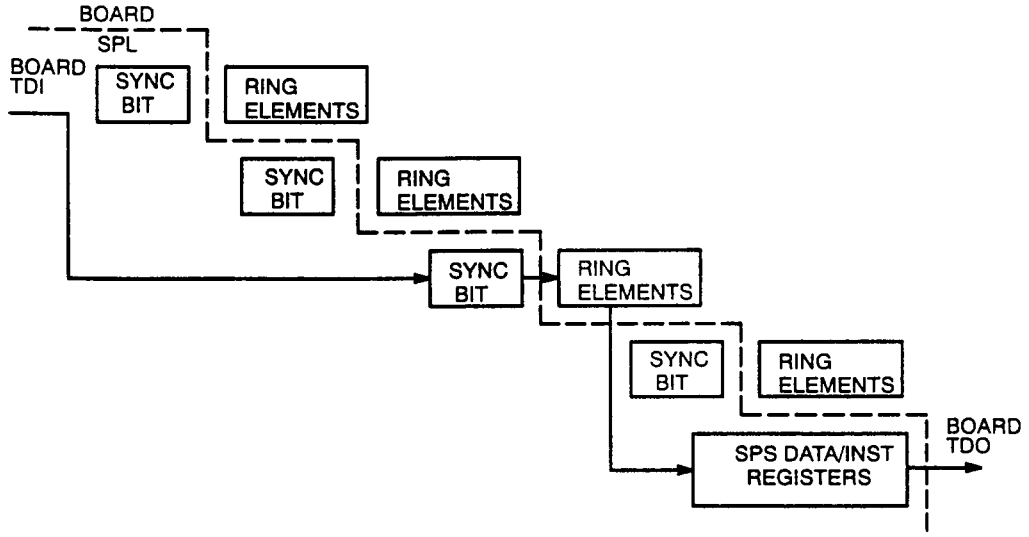


Figure 4. Scan-Path Linker (SN74ACT8997)



Scan-Path Linker (74ACT8997) with All Secondary Scan Paths Selected



Scan-Path Linker (74ACT8997) with One Secondary Scan Path Selected

Figure 5. Scan-Path Linker Data Path

Referring to Figure 4, the Scan-Path Linker again introduces an extra bit into the data path of each secondary scan path when opened. Figure 5 depicts the actual scan order when one or four secondary scan paths are opened in Scan-Path Linker.

Each of the sync bits are bypassed when a scan path is not selected and only the scan path or rings that are selected will introduce an extra bit into the path.

Remote Bus Controller Interfaces

When a Remote Bus Controller (RBC) is present with the Scan-Path Selector, certain interfaces to and from the SPS device need to be modified to ensure proper operation. The RBC inputs its TMS output to the OPTIONAL TMS (OTMS) pin of the SPS. When the SELECT register is loaded to output OTMS to the DTMS outputs, the CONTROL register must

also be loaded with the RBC Enable bit (RBCE) set TRUE to allow the RBC TMS direct control of the SELECT register. In this mode the Remote Test Access Port (RTAP) controls the shifting of data through the DTDI to the DTDO to the rings. When the RTAP is in control a dedicated instruction and bypass register become activated to emulate a true 1149.1 interface as seen by the RBC, as depicted in Figure 6.

The only valid instructions are 'scan the select register' or 'scan the bypass bit' during this mode of operation. The Primary Bus Controller (PBC) still has the ability to scan the other registers in the SPS that enables it to disable the RBC by setting the RBCE bit to FALSE should it become necessary. When connecting an RBC to the SPS the normal interfacing must be altered as shown in Figure 7.

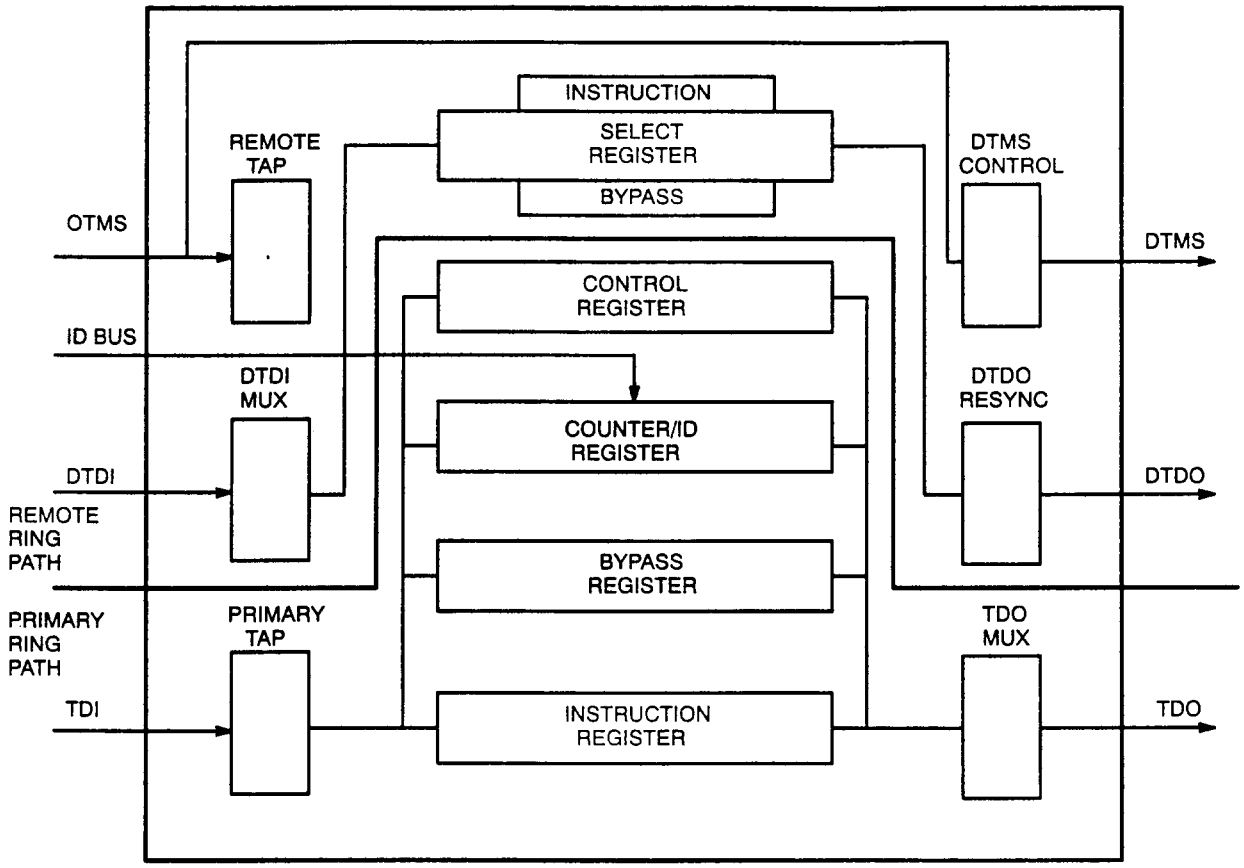


Figure 6. Scan-Path Selector (SN74ACT8999) with Optional (Remote) TMS Selected

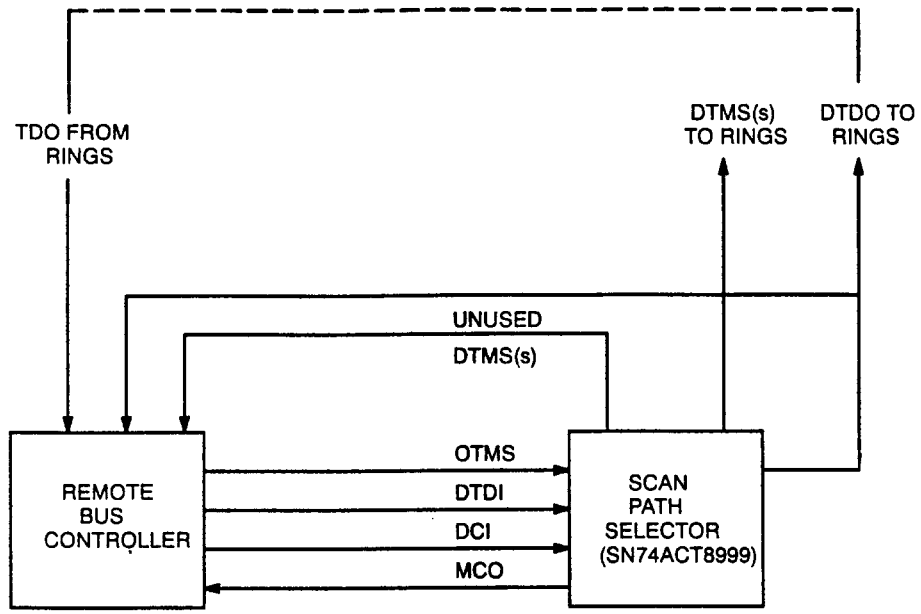


Figure 7. Remote Bus Controller Interface to Scan-Path Selector

The TDO signals of each of the rings must pass through the RBC in order for the RBC to receive data when active. In the same way each of the rings is resynchronized within the SPS, the RBC must clock the TDO data in and pass it out to the DTDI input of the scan-path device when inactive. For this reason, all of the DTMS signals must be fed to the RBC in order to determine when data is being shifted through a scan path so that the internal resync bit can be properly clocked or held. When activated, the RBC must also have the ability to bypass all of the rings, hence the requirement to feed the DTDO of the scan-path device directly to the RBC. Finally, to ensure proper handoff of control of the board rings, it is recommended that the RBC receive MCO from the SPS, to signal a grant from the PBC, and send DCI to the SPS, to indicate to the PBC that the RBC is currently using the board rings. This is also the handshake mechanism between the PBC and RBC for BiD bus transfers.

Partitioning 1149.1 Designs Using the Scan-Path Support Devices

System Level Partitioning and Considerations

Design Requirements

The ability to create a hybrid star/scan-path architecture using a scan-path device has many advantages over a single scan-path design. Scan designs can be partitioned in such a way as to completely isolate functions for testing while leaving others undisturbed. In scan-path architecture this is also possible. However, the devices not related to a particular test still must be placed in the BYPASS SCAN mode through an instruction scan, and the bypass bit in the data path must be recognized by software. In a design that requires time slice testing, that is, taking a function off-line to run a test and returning it back within a fixed amount of time, lends itself quite well to the scan-path device architecture. The controller can open a secondary scan path, test a function, and replace it to normal operation while not disturbing or scanning other functions in the system. In order to properly implement such a scheme, a careful design requirement must be developed in advance to account for any possible unexpected operations when exercising a function. For instance, an ASIC self test may inadvertently toggle its device outputs that in turn ripple to another function not under test. The inputs of the ASIC under test must be isolated so that the circuits feeding it do not effect the self-test. Avoiding inadvertent operation is probably the most common consideration but there are many others when implementing a time slice test scheme. Only through proper system definition and specification can all of the pitfalls be avoided. Another advantage of using a scan-path device is the ability to have a remote bus controller resident on the board to relieve the test burden of the primary bus controller. This creates a distributed test structure in which the PBC can command tests to be run autonomously on multiple boards and report status back. The relief realized at the system level is, of course, not

without cost. The development of board controller software will still be necessary as well as the handshaking and reporting structure between master and remote. This structure has a payoff throughout a product life cycle by exploiting tests during board and system integration, board production and depot testing as well as common module insertion. It can also reduce system test times by having all tests within a system running tests concurrently and reporting status instead of a single primary system executing tests in series.

Partitioning of Scan Paths

The proper partitioning of rings is the single most important factor in successfully reaping the benefits of scan-path device insertion into a scan design. Normally a board is functionally partitioned within a system by design. Within a board, functions also need to be partitioned for scan testing by placing test-related scan elements adjacent in the scan path. When using a scan-path device this is a requirement to enable efficient use of the device. If a test requires scanning of devices on separate rings of a scan-path device on a board, the controller must scan the devices to stimulate a test, scan the scan-path device SELECT register to place the stimulus secondary scan path in IDLE in order to hold the data, and open the response scan path, and then scan the results from the response scan path. This procedure becomes even more complex should the stimulus and response elements be mixed on separate rings. Should the test involve a dynamic stimulus and response, that is not static patterns, repeatability may not be possible. This fact arises due to the need to leave either the stimulus or response elements in IDLE (which implies running) while the other is being initialized. The time between scanning the first scan-path elements and the second could be variable or cause unknown data to be generated or sampled. Careful timing analyses can be performed to eliminate the problem but such an architecture is not recommended. Instead, the linkable scan-path device, SPL, should be used if scan elements for tests MUST reside on different rings for multiple uses, i.e., an element in RING1 is used for stimulus in a test with RING2, and response with elements on RING3. In most cases this is avoidable or optimization is possible to minimize the number of "inter-scan path" tests through proper partitioning.

How Much Scan

Another consideration for system-level designs is how much partitioning should be performed. Each scan-path device has four rings that can be used in a design, but not all of them have to be used. If the design does not lend itself to creating four separate rings, two or three can be used. This can create an open scan-path condition when an unused scan path is inadvertently selected. Great care must be taken during software development and design to avoid this possibility from occurring through constraint checking. If SPL is used, the DTDO and DTDI of unused rings can and should be tied together to at least create a path for data. Software must still detect the lack of any device(s) on the scan path that was opened, based upon instruction scan error checking or through examination of the scan-path device's SELECT register. This problem compounds itself when multiple scan-path devices exist within a system that have unused DTMS signals. Under such conditions the scan controller software will have to find the SELECT register contents of each scan-path device in the scan path to detect the error, determine the true state of the scan path, and correct the problem. The controller software becomes an issue in determining whether to use the scan-path device in a design. The obvious solution is to use all of the scan rings available on the scan-path device. Switching between multiple secondary scan paths for a test again becomes a problem and the SPL is recommended. If a remote controller is being used, all of the DTMS signals and the DTDO must be fed to it and can be used to detect the error condition, maintain the data-path integrity, and signal the PBC through the DCI-> DCO status signals of the condition.

Board Boundary Testing

When implementing scan-path devices into designs that contain board boundary scan elements to test backplanes or motherboards, two options exist for placing the boundary elements as depicted in Figure 8.

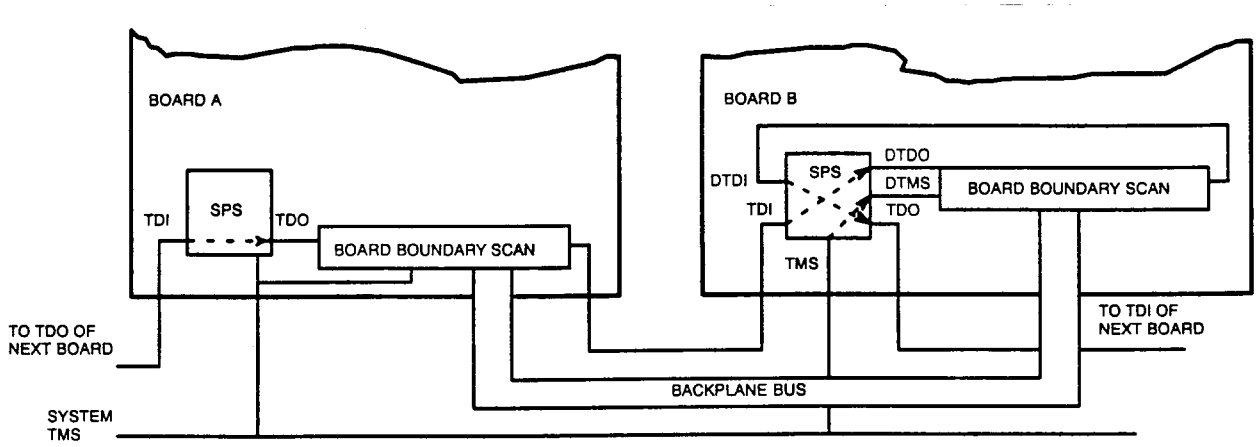


Figure 8. Board Boundary Element Scan-Path Options

Board A has the boundary elements placed on the primary scan path of the system. This would allow for two scenarios. First, if an RBC was also present on the board, the PBC could perform board boundary tests while the RBC performed board tests. Secondly, this implementation also allows selecting a scan path on the board and scanning the boundary elements to perform multiple tests concurrently. The disadvantage of this scheme is that the board is no longer isolated from the system by a single interface and some of the fault tolerance of the scan-path device architecture is lost. Board B places the boundary elements on a scan path of the scan-path device. This option retains all of the advantages of the scan-path device fault tolerance with the trade-off being the inability to run RBC concurrent tests if one is present in the design. In both cases board-to-board testing is still possible using the system scan-path architecture and the ability to open a scan path on each board.

Partitioning a Board Design – An Example Memory Board Description

The example given is a simple memory board. It consists of a bus interface controller that could be an ASIC or discrete circuitry. The bus controller decodes address and control activity on the backplane and creates the necessary address and control signals required locally for memory and I/O cycles. The board also includes further decoding to create specific device selects for the memory and I/O arrays and any further control signal generation not performed within the bus controller. Finally, the board contains a memory array and I/O register array. The memory array could contain both static- and PROM-type devices.

Partitioning for Test

The buffers for the board are chosen from the 'BCT8XXX family of 1149.1-compatible octal devices ('BCT8244,8245,8373,8374). Referring to Figure 9, the placement of these devices partition the board into its three functions; bus controller, decode circuitry, and the memory and I/O space.

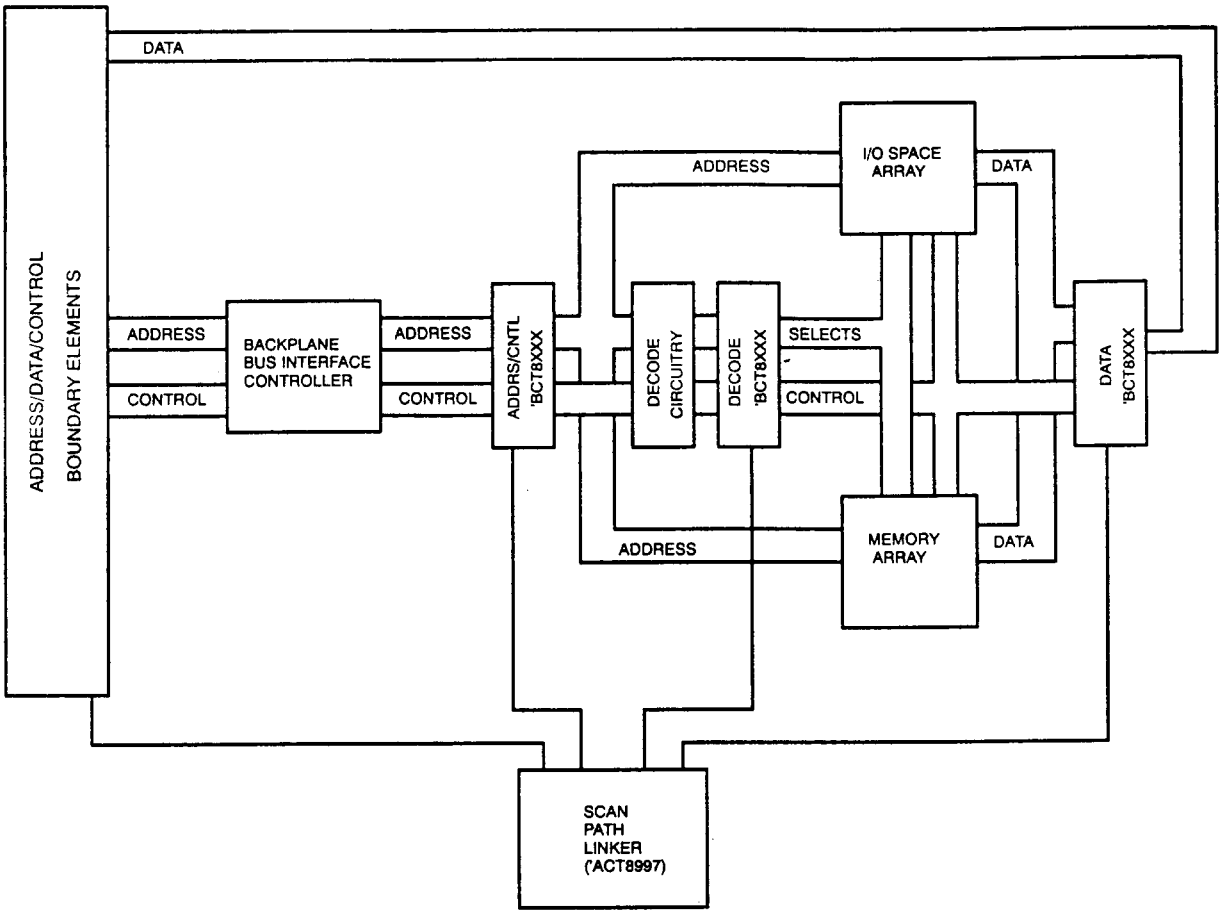


Figure 9. Memory Board Partition Example Using Scan-Path Linker

In addition, the backplane has been isolated by inserting the 1149.1-compatible octals for testing the interface to and from other boards using the test controller. These elements are on a scan path by themselves so that they can be scanned to perform the aforementioned tests without scanning the rest of the board. Next, 1149.1-compatible octals are placed between the bus controller and decode circuitry and between the decode circuitry and memory-I/O space arrays, each on its own scan path. Since tests of each of the functions relies on two of the scan-path device rings, the SPL is chosen. Thus, to test the memory array the control selects the address/control buffers and data buffers to be opened and links through the SPL; the boundary elements and address/control to test the bus interface controller; and so on. The address/control and decode octals could have been placed on the same scan path, but this would only serve to complicate the tests.

Remote Bus Controller Implementation

When Remote Bus Controller (RBC) is added and the rings slightly altered to best accommodate it, the SPS with an RBC input does not allow linking of the rings. Referring to Figure 10, in order to reduce the amount of switching between the rings, the address/control and data octals are placed on the same scan path .

This allows the RBC (and the PBC) to test the memory array most efficiently, since it would most likely be the longest test to be performed on the board. The boundary and decode circuitry are also placed on the same secondary scan path so that they can be tested quicker. Detection of a fault in the functions is possible, but isolation to the failing function still requires switching between secondary scan paths.

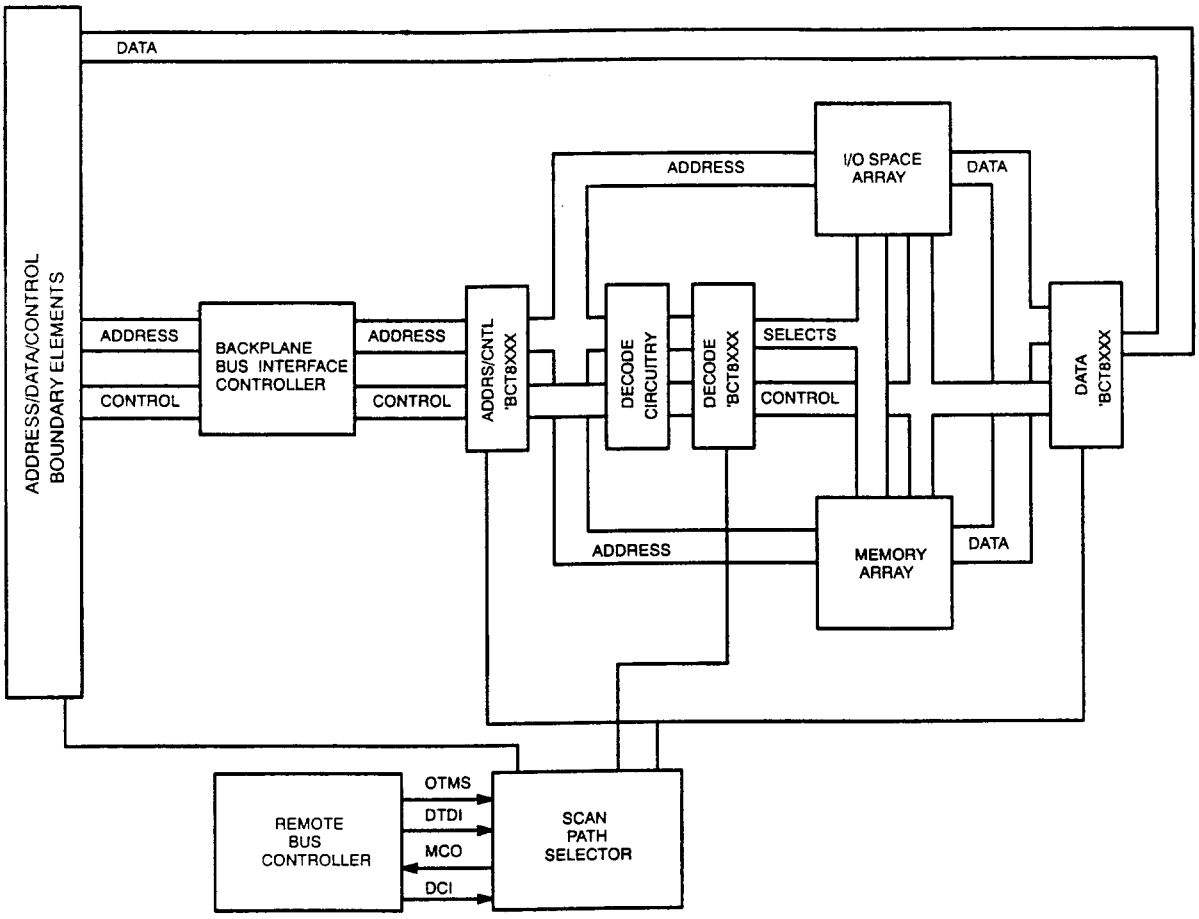


Figure 10. Memory Board Partition Example Using Scan-Path Selector

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