Recent Advancements in Bus-Interface Packaging and Processing

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Introduction

Over the past several years, the advancements in semiconductor processing have been combined with advanced surface-mount packages to offer solutions to board area concerns, as well as, providing for increased system performance. Figure 1 compares the reduction of the package's lead pitch to that of both CMOS and BiCMOS transistor geometries. This paper will explore the different types of fine pitch logic packages and the bus interface solutions provided when they are combined with sub-micron semiconductor processes.

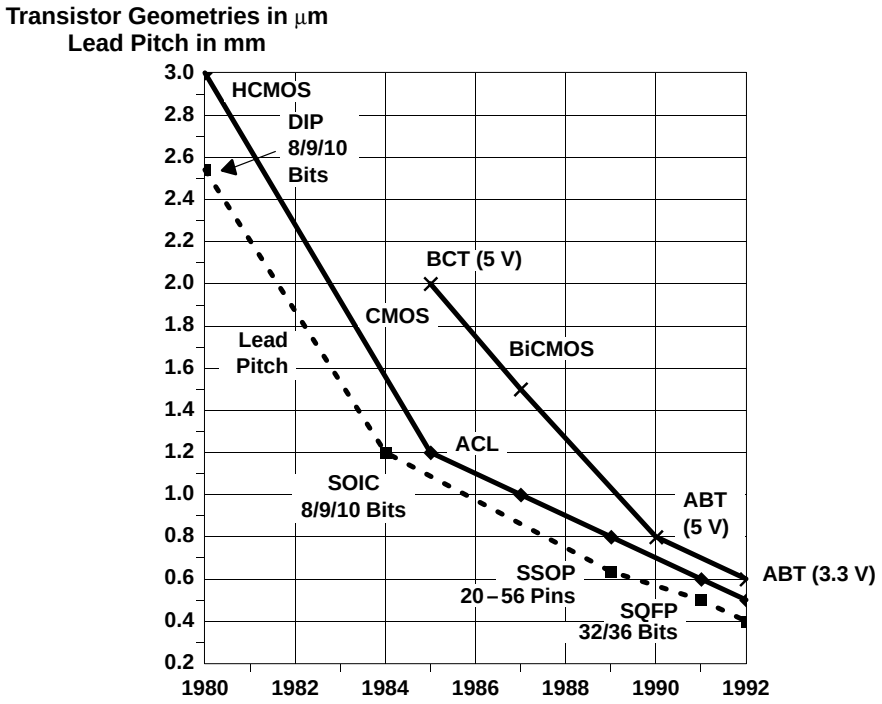

Figure 1. Packaging/Processing Evolution

Evolutions in Device Packaging

With the need for increased functionality in less board area has come the consolidation of much of the board's logic into higher complexity devices. In many cases the discrete logic parts that remain, primarily interface/bus drivers, must occupy the board area leftover after the higher level chips, i.e., microprocessor, ASICs, memory, etc., have been laid out. To meet this task the standard small-outline integrated circuit (SOIC) has evolved in two distinct paths. One path reduces the package's area and volume (see Figure 2), and the other increases the bit density of the device (see Figure 3).

One method to increase bit density is to keep the number of pins constant while reducing both the lead pitch and package area. The 20/24 pin SSOPs utilize a 0.65-mm lead pitch to achieve over a 50% reduction in area, compared to their standard SOIC counterparts. The package height is also reduced from 2.65 mm for the SOIC to 2 mm for the 20/24-pin SSOPs. This reduction in volume translates into tighter board to board spacing, allowing for denser memory arrays.

The advent of the Personal Computer Memory Card International Association (PCMCIA) standard has required that the package height be reduced even further, thus spawning the thin small-outline package (TSOP). This package utilizes 0.65-mm lead pitch and has a maximum device height of 1.1 mm. With an area of 59 mm^2, this package utilizes 86% less volume than the standard 24-pin SOIC, facilitating the use of logic functions on these cards.

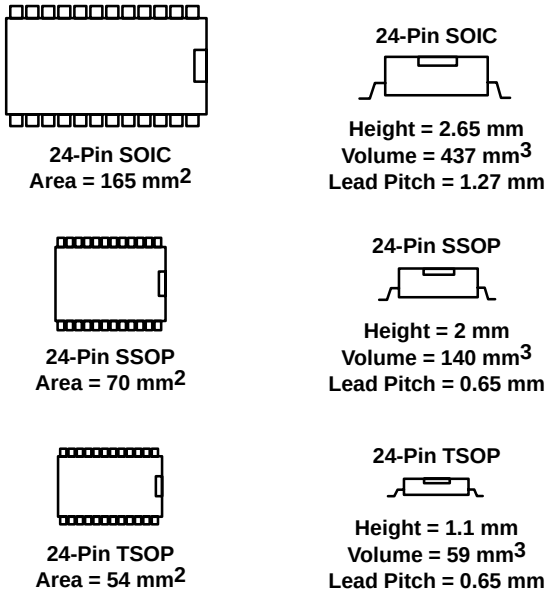

Figure 2. 24-Pin Surface-Mount Comparison

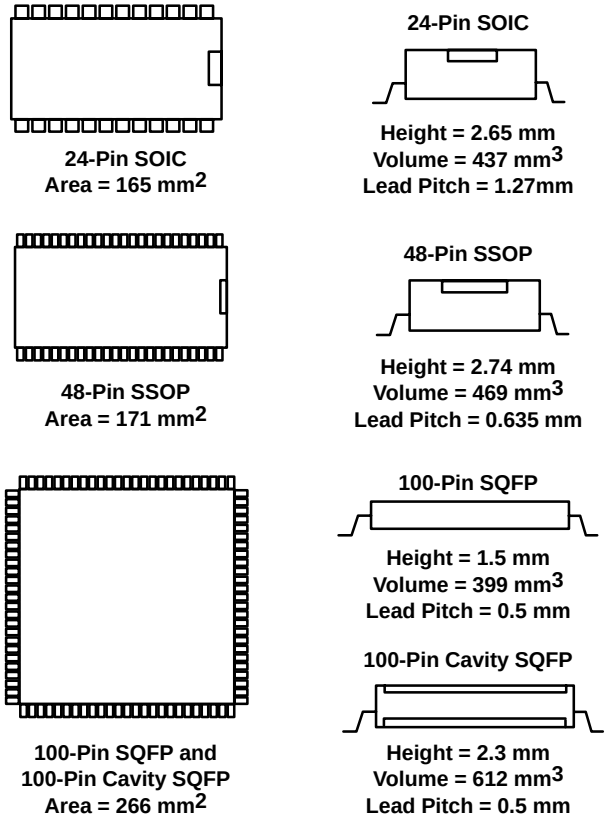

Figure 3. High Pin-Count Comparison

Another way to increase bit density is to reduce the lead pitch of the package. The 48/56-pin shrink small-outline package (SSOP) halves the lead pitch of the SOIC package from 1.27 mm to 0.635 mm, allowing for twice the number of I/O pins in the same board area. The 8-, 9-, and 10-bit functions now become 16-, 18-, and 20-bit parts. The 100-pin shrink quad flat package (SQFP), along with the high-power cavity-SQFP, further reduce the lead pitch to 0.5 mm. These packages double the bit density over the 48-pin SSOP with only a 50% increase in area. Both of these high pin-count packages allow for 32- and 36-bit logic functions, providing for efficient buffering of today's 32- and 64-bit bus widths.

Thermal Impedances of Fine-Pitch Packages

As package area decreases, which is the case for the 20- and 24-pin SSOP and TSOP, the thermal impedance of the package to the ambient environment (Θ_{JA}) increases. Figure 4 illustrates the fact that this relationship is almost linear, and for a 50% reduction in area, Θ_{JA} doubles for the 24-pin SSOP and TSOP. Because of the higher Θ_{JA}, additional attention must be given to the power dissipation of the device to insure proper operation.

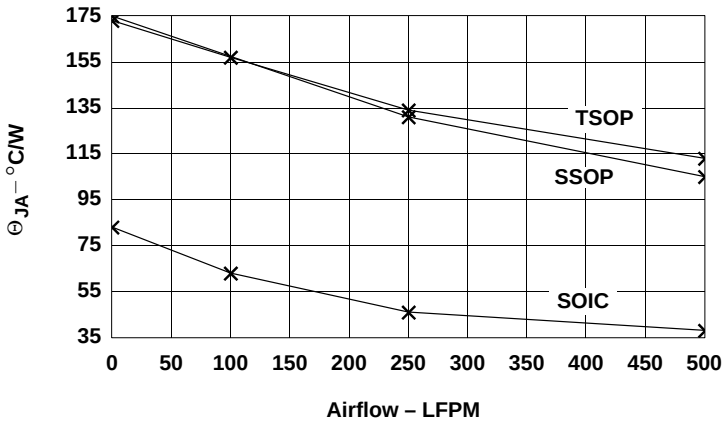

Figure 4. Θ_{JA} Versus Airflow for 24-Pin Packages

A similar power consideration occurs with the high-pin-count packages due to the increased number of bits causing higher power dissipation per package. Figure 5 compares Θ_{JA} for the 24-pin SOIC, 48-pin SSOP, 100-pin SQFP, and cavity SQFP. The cavity package mounts the lead frame directly to one of the metal lids of the package. This mounting provides a direct path for the heat to flow from the die to the ambient environment. This package accommodates both cavity up or down assembly allowing for both conduction, into the board, or convection, into the ambient, cooling.

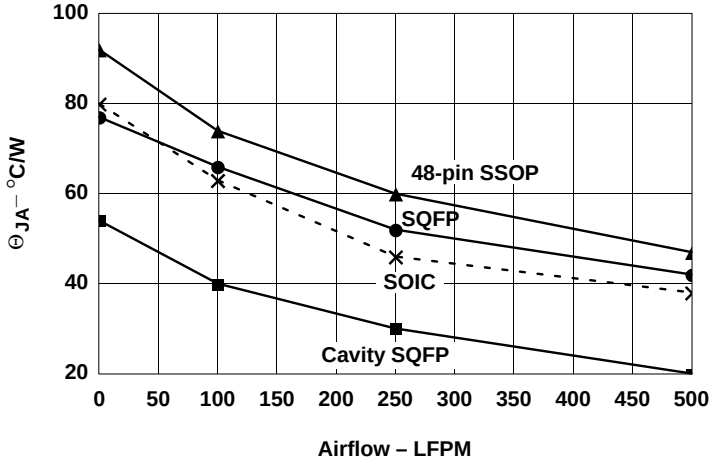

Figure 5. Θ_{JA} Versus Airflow

One factor influencing Θ_{JA} is the trace length that is connected to the package lead finger. This is because some of the heat is taken out of the package through the lead and dissipated into the board as well as through the package top and into the ambient air. Nonstandard trace length factors have been identified as a major contributing factor in differences between different manufacturer's published thermal values. Figure 6 shows the effect that trace length has on the 48-pin SSOP Θ_{JA}.

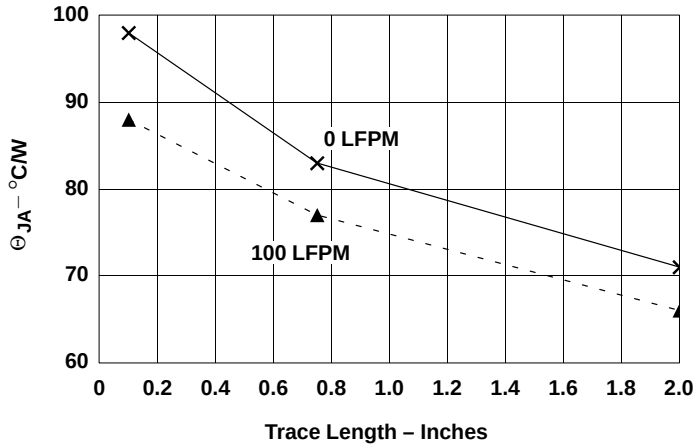

Figure 6. 48-Pin SSOP Θ_{JA} Versus Trace Length

Evolutions in Device Processing

With the improvements to microprocessor clock rates and memory access times, bus-interface devices have become a larger percentage of the total bus cycle time. To keep pace with the need for faster logic many semiconductor manufactures are utilizing sub-micron BiCMOS processes, utilizing shorter gate lengths and thinner gate oxide for device speed improvements. The reductions in transistor area result in less intrinsic capacitance allowing faster internal gate delays, as well as lowering the output capacitance (Ci/o). With a lower Ci/o, ABT devices minimize their impact to system loading.

In a transmission-line environment, when the driver's edge rate is less than twice the line's propagation delay, distributed output loading has the effect of reducing the characteristic impedance (Z_o) of the transmission line. The higher the distributed capacitive load, the lower the apparent impedance, making it harder for the driver to switch the line on the incident wave. This well-known transmission-line loading equation is:

$$Z'_o = \frac{Z_o}{\sqrt{1 + \frac{C_d}{C_o}}} \quad \textbf{(1)}$$

where Z_o is the line's unloaded characteristic impedance, C_o is its intrinsic capacitance per unit length, and C_d is the distributed capacitive load per unit length.

Figure 7 shows how the a device's output capacitance can lower a line's impedance, as in the case of a backplane. If the effects of the other board capacitance contributors – connectors, vias, and trace stubs, are assumed to be constant regardless of the device used, and thus ignored, a comparison of transmission-line loading between different technologies can be made.

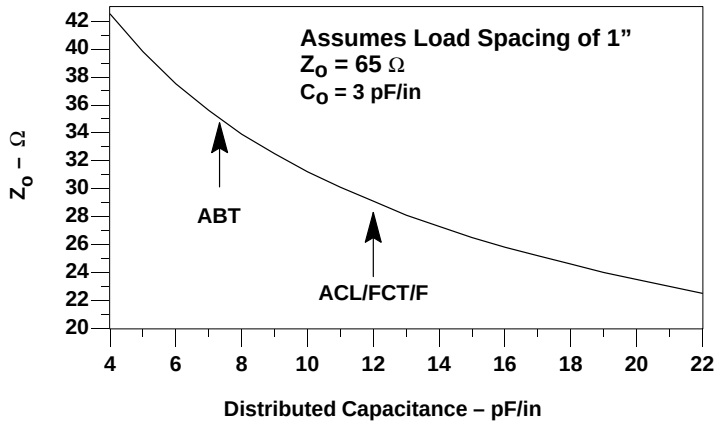

Figure 7. Loaded Z_O Versus Distributed Capacitance

3.3-V Operation

As process geometries move towards gate lengths of 0.5 μ and below, coupled with the desire for lower power consumption, 3.3-V operation becomes necessary. Because the migration to 3.3 V will be gradual, gated by the availability of semiconductor functions, the need for mixed signal-level operation will be critical for bus-interface devices. That is the input and I/O pins will be able to have input voltage levels up to 5.5 V without any conduction paths to V_{CC}. The outputs should also be capable of driving a standard 5-V backplane, which would translate into drive currents of at least –15 mA of I_{OH} and 64 mA of I_{OL}.

Advanced Bus-Interface Solutions

Memory-Driver Usages for the SSOP

As pointed out previously, any of the SSOPs can be utilized as buffers in high-density memory arrays. In many instances, series-dampening termination is chosen due to its ease of implementation and power savings. Numerous logic devices are available that incorporate the series-dampening resistor on chip, as in the BCT2XXX series of products, simplifying this type of termination. When these parts are packaged in the 20-pin SSOP, as in the ′BCT2240DB, a tremendous board real estate savings is realized over a discrete approach using external resisters and SOIC devices. For PCMCIA cards, the driver must also offer low-power consumption necessary for battery operation. The ′AC11244PW (TSOP package) can be used in these applications due to its low static-power CMOS characteristics.

Many times, when an output switches a large memory array, the capacitive load is localized in close proximity to the driver and can be treated as a simple lumped load. In these instances, it is useful to know how the propagation delay (t_{pd}) of the driver changes with the additional capacitive load. The change in the driver's t_{pd} is due to the interaction of its source impedance, R_{on}, with the capacitive load, C_L. Figures 8, 9, and 10 show this phenomena for the ′AC11244, ′BCT2240, ′ABT16244, and ′ABT32245 for both single and multiple-outputs switching.

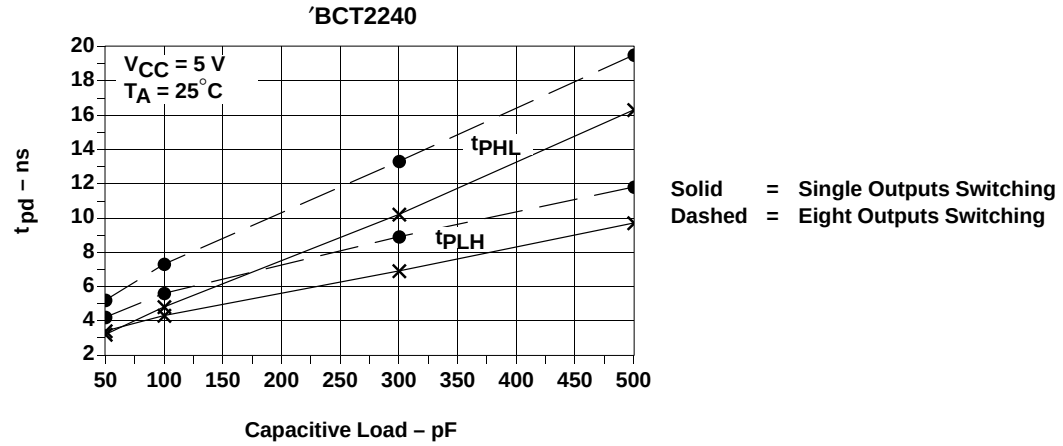

Figure 8. Typical t_{pd} Versus Capacitive Load

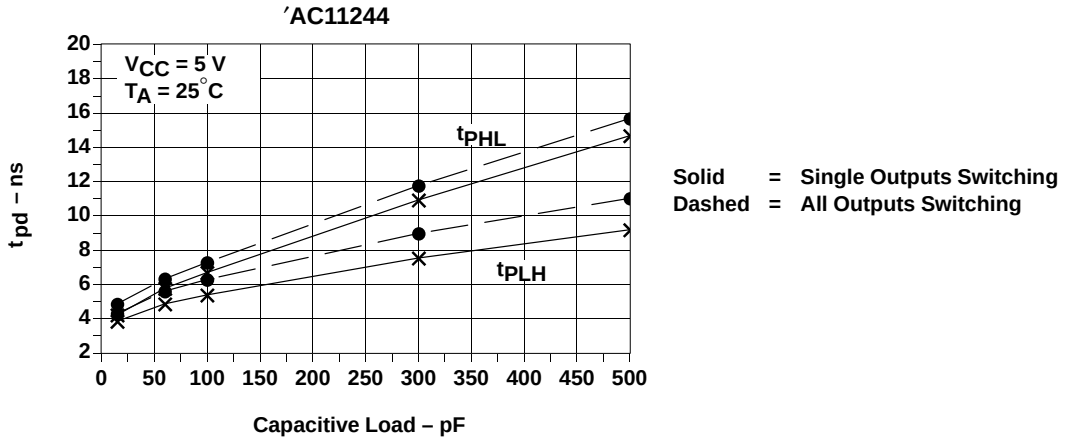

Figure 9. Typical t_{pd} Versus Capacitive Load

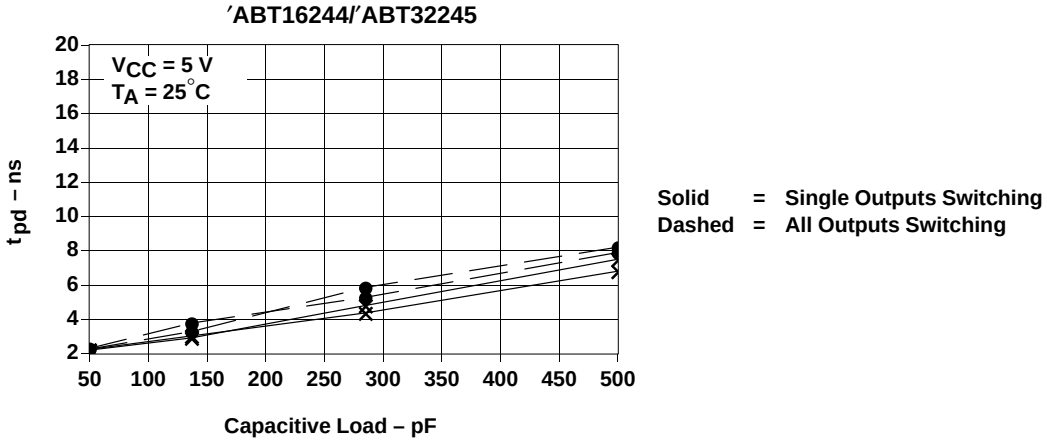

Figure 10. Typical t_{pd} Versus Capacitive Load

Figures 8 through 10 illustrate the effect that the output impedance of the driver has over t_{pd} degradation. Figure 8 shows that even though the ′AC11244 has symmetrical high and low output drive current ratings of 24 mA, t_{PHL} shows more degradation versus capacitive loading due to the graded turn-on of the output to minimize simultaneous switching noise [ground bounce]. Many advanced CMOS logic devices utilize this graded turn-on, but not without the penalty of slower propagation delays at higher capacitive loads. Figure 9 shows a similar asymmetrical t_{PHL} performance, but now it is due to the inclusion of a 33-Ω series output resistor. Contrasting the previous two graphs is Figure 10 that highlights the high-drive capability of the ABT16XXX and ABT32XXX devices, along with the symmetrical t_{pd} performance that the –32-mA/64-mA outputs deliver.

Bus-Interface Usages for the SSOP

The gains made by utilizing devices with faster propagation delays can be lost if the propagation delay degrades when multiple outputs on a package are switched simultaneously. This effect is greatly reduced when a device is packaged in the 48-/56-pin SSOP, because this package allows the signal-to-ground ratio of a standard 8-bit function to be improved from 8:1 to 2:1, and the signal-to-V_{CC} ratio to be improved from 8:1 to 4:1. This multiple power-pin system translates into a quieter on-chip power system when multiple outputs switch, resulting in less propagation-delay degradation compared to a standard 8-bit function. The same can be said of the 100-pin SQFP and cavity SQFP that utilizes a 3:1 signal-to-ground ratio. Figure 11 compares the change in t_{pd} versus the number of outputs switching (in phase) of a typical ′244, buffer-type function when packaged in a 48-pin SSOP and 100-pin SQFP to the performance in a 20-pin DIP and SOIC.

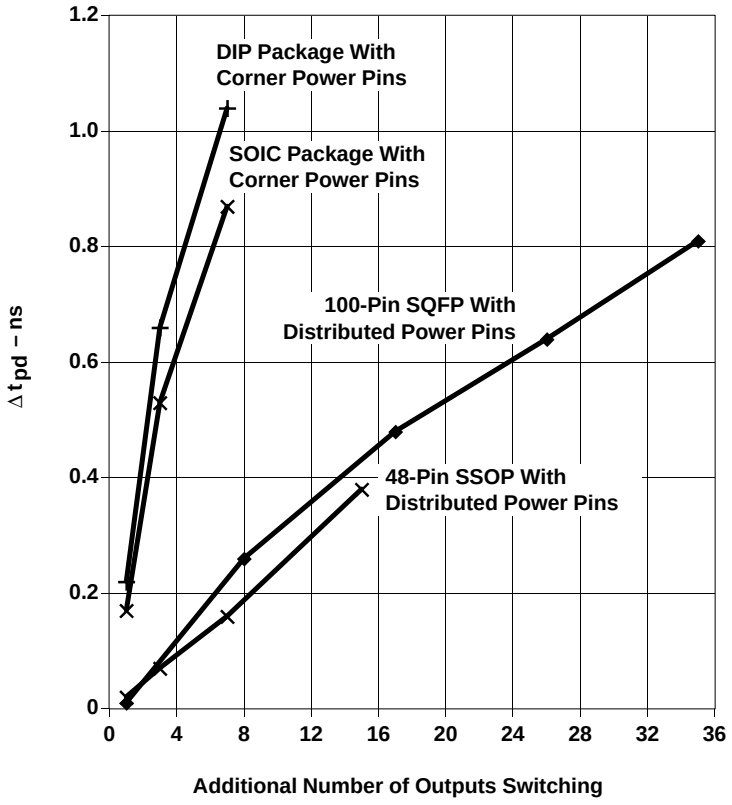

Figure 11. Typical Δt_{pd} Versus Outputs Switching

Summary

The various fine pitch surface-mount packages give the designer a wide range of solutions to today's system area and volume constraints. The high pin-count SSOP and SQFP packages allow bus-interface devices to track the trend of wider data bus widths, while providing superior electrical performance when compared to the standard end-pin product. The cavity SQFP allows for higher power-dissipation applications, allowing the interface device to operate at higher frequencies. The low pin-count SSOPs occupy less volume than other surface-mount devices, facilitating their use in height-critical applications.

References

Transmission Lines

Advanced Schottky Family Applications, Texas Instruments Incorporated Advanced Schottky Data Book, 1986
Advanced CMOS Logic Designer's Handbook, Texas Instruments Incorporated, 1988

Power Dissipation

SSOP Designer's Handbook, Texas Instruments Incorporated, 1991