Package Thermal Considerations

SCZA002C
June 1994 – Revised August 1996

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Contents

List of Illustrations

Abstract

Smaller packages with more functionality have greater power densities that increase junction temperatures, thereby adversely affecting device and system reliability. Good thermal-design practices, both package and application specific, can lower the junction temperature. Altering power consumption, trace length, heatsinks, air flow, and package design can mitigate effects of greater power density. Formulas for calculating power consumption must account for static and dynamic currents. Although no industry standard exists for calculating thermal resistance (Θ_{JA}), variations in values among manufacturers of identical packages can be attributed to physical aspects of board design rather than measurement methodology. Software has been developed that calculates realistic values for Θ_{JA}, taking into account significant conditions.

Introduction

To meet current and future system requirements of increasing speed and decreasing size, integrated-circuit manufacturers are pushing the edge on existing packaging technology. A component's performance is determined by process technology and the thermal limitations of its package. As a leader in package technology, Texas Instruments (TI) has introduced a number of fine-pitch packages and is acutely aware of the thermal considerations that must be examined by systems designers. This paper is intended to create awareness and understanding of thermal issues and to explore factors that influence thermal performance.

Thermal awareness became an industry concern when surface-mount (SMT) packages began replacing through-hole (DIP) packages in PCB designs. Circuits operating at the same V_{CC} enclosed in a smaller package meant higher power consumption. To add to the issue, systems required increased throughput, which resulted in higher frequencies, increasing the power density even further. Not only are designers faced by these same concerns today, they progressively are becoming more severe.

Figure 1 shows part of the reason for increased attention to thermal issues. As a baseline for comparison, the 24-pin small-outline integrated circuit (SOIC) is shown along with several fine-pitch packages supplied by TI, including the 24-pin SSOP (shrink small outline), 48-pin SSOP, and the 100-pin TQFP (thin quad flat pack). The 24-pin SSOP (8, 9, and 10 bits) allows for the same circuit functionality of the 24-pin SOIC to be packaged in less than half the area, while the 48-pin SSOP (16, 18, and 20 bits) occupies just slightly more area but has twice the functionality of the 24-pin SOIC. This same phenomenon is expanded even further with the 100-pin TQFP (32 and 36 bits), which is the functional equivalent of four 24-pin or two 48-pin devices, with additional board savings over that of the SSOP packages. As the trend toward smaller packages continues, attention must be focused on the thermal issues that are created.

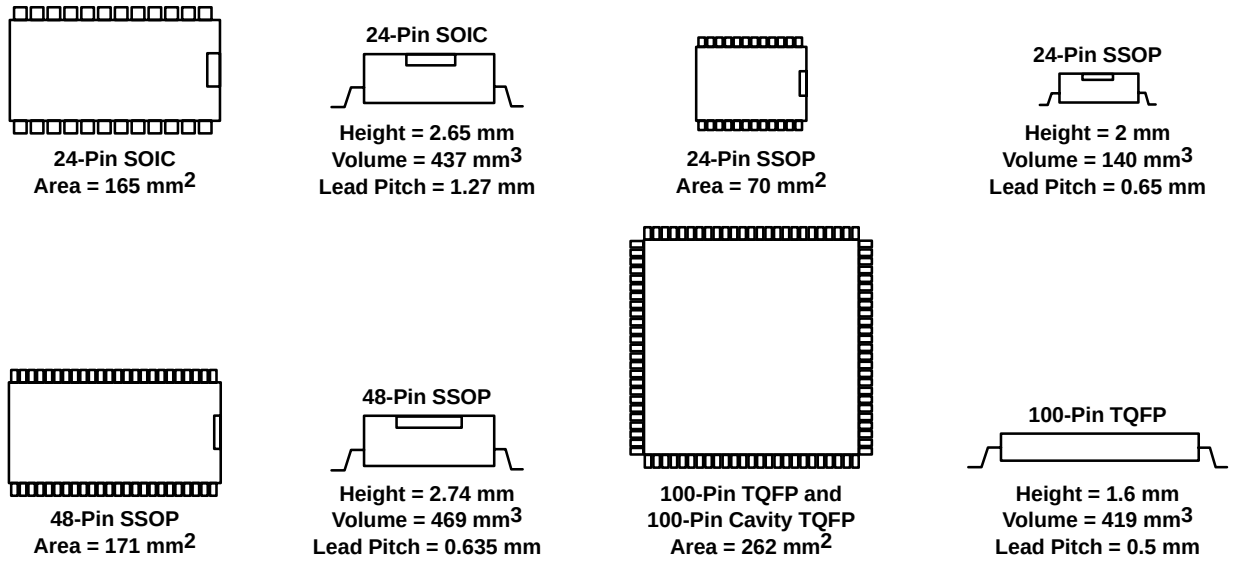


Figure 1. Advanced Packages

Reliability

The overriding effect of increased power densities in integrated circuits is a decrease in overall system reliability. A direct relationship exists between junction temperature and reliability.

Table 1 provides an example of a device with an initial junction temperature of 150°C and the calculated decrease in failure rate as the in-use junction temperature is lowered. The data in Table 1 indicates that lower junction temperature results in increased system reliability.

Table 1. Failure Rate Versus Junction Temperature

TEMPERATURE °C	% FR†
150	96
140	80
130	46
120	11
110	1
100	0.02

† Failure rate at 100,000 hours

A better understanding of the factors that contribute to junction temperature (T_J) provides a system designer with more flexibility when attempting to solve thermal issues. Device junction temperature is determined by equation 1:

$$T_J = T_A + (\Theta_{JA} \times P_T) \quad \textbf{(1)}$$

Where:

T_J = junction (die) temperature (°C)
T_A = ambient temperature (°C)
Θ_{JA} = thermal resistance of the package from the junction to the ambient (°C/W)
P_T = total power of the device (W)

Junction temperature can be altered by lower chip power consumption, longer trace length, heatsinks, forced air flow, package mold compound, lead-frame size and material, surface area, and die size. Some of these are mechanically inherent to a particular package while others are controlled by the designer and are application specific. Understanding which variables can be influenced by practicing good thermal-design techniques requires a more detailed investigation of power considerations as well as thermal-resistance measurements.

Power Consumption

One way to lower the junction temperature of a device, thus improving reliability, is to lower the power consumption. A variety of options are available to help achieve this, such as low-power process technologies, reduced output swing, and reduced power-supply voltage. A closer look at the power performance and advantages of several popular logic families can assist in choosing devices that best fit designers' needs.

The choices available from TI for high-speed bus interfaces range from standard bipolar (F) to advanced CMOS (ACL/ACT) to state-of-the-art BiCMOS (BCT) and advanced BiCMOS (ABT). Figures 2 through 4 show comparisons of current (I_{CC}) consumption of '244 functions for these technologies across frequency. As expected, the bipolar device consumes more current than the CMOS device at lower frequencies, but as frequency increases, this relationship no longer holds true. In fact, there is a region in the frequency range where the CMOS device consumes more current than the bipolar device. The point where they are equal is referred to as the crossover frequency.

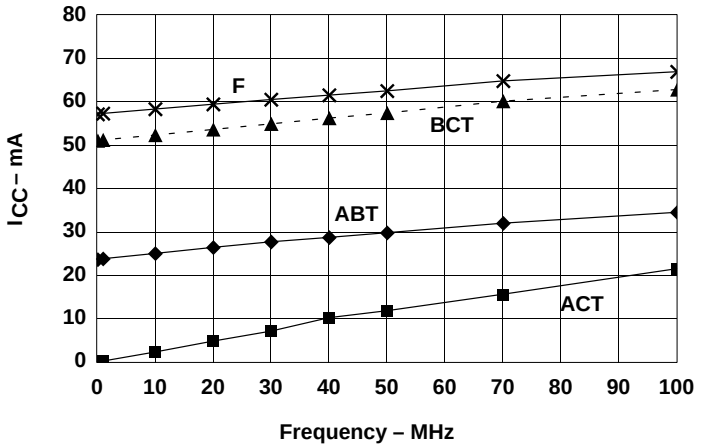


Figure 2. I_{CC} Versus Frequency (One Switching, Unused Outputs Low)

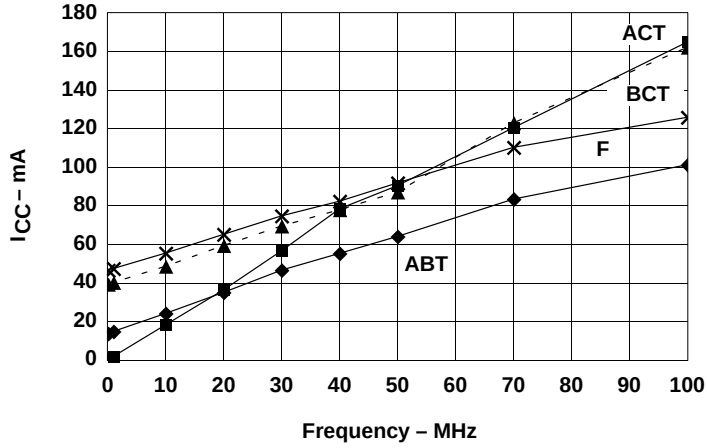


Figure 3. I_{CC} Versus Frequency (All Outputs Switching)

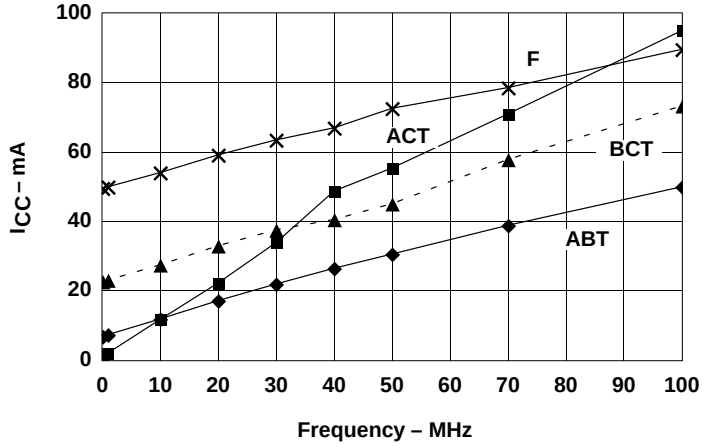


Figure 4. I_{CC} Versus Frequency (All Switching, 50% Duty Cycle Enabled)

Typical applications for bus-interface devices require them to be disabled or in the standby mode during certain periods of time, for instance, while other devices access the bus. This can result in a large decrease in current consumption for ABT, BCT, and ACT devices, which have low standby currents. These values are given in the data sheets as I_{CC} for ACT and I_{CCZ} for ABT (250 μA) and BCT (≅10 mA). Current consumption versus percent duty cycle enabled is shown in Figure 5. The frequency of the data is held constant at 25 MHz and all outputs are switching.

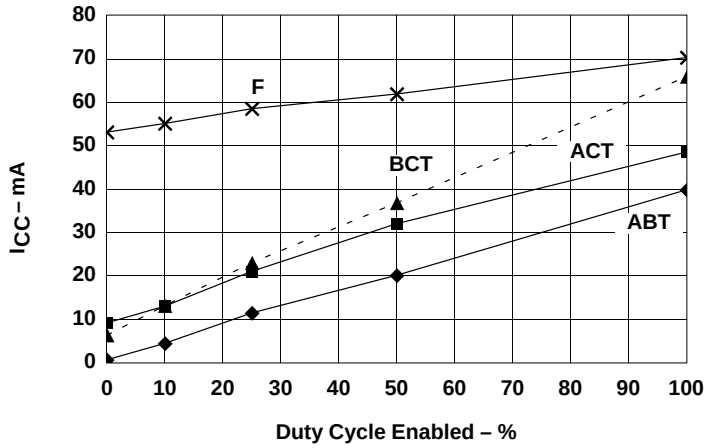


Figure 5. I_{CC} Versus Duty Cycle Enabled (25 MHz)

Using this data, along with standard formulas, power consumption can be calculated for specific applications.

Power Calculations

When calculating the total power consumption of a circuit, both the static and the dynamic currents must be taken into account. Both bipolar and BiCMOS devices have varying static-current levels, depending on the state of the output (I_{CCL}, I_{CCH}, or I_{CCZ}), while a CMOS device has a single value for I_{CC}. These values can be found in the individual data sheets. ACT and ABT inputs, when driven at TTL levels, also consume additional current because they may not be driven all the way to V_{CC} or GND; therefore, the input transistors are not completely turned off. This value is known as ΔI_{CC} and is provided in the data sheet.

Dynamic power consumption results from charging and discharging of both internal parasitic capacitances and external load capacitance. The parameter for ACT and AC devices that accounts for the parasitic capacitances is known as C_{pd}. It is obtained using equation 2 and is found in the data sheet.

$$C_{pd} = \left[\frac{I_{CC}\ (\text{dynamic})}{V_{CC} \times f_i}\right] - C_L \qquad \textbf{(2)}$$

Where:

f_i = input frequency (Hz)
V_{CC} = supply voltage (V)
C_L = load capacitance (F)
I_{CC} = measured value of current into the device

Although a C_{pd} value is not provided for ABT, BCT, or F devices, the I_{CC} versus frequency curves display essentially the same information. The slope of the curve provides a value in the form of mA/(MHz × bit), which when multiplied by the number of outputs switching and the desired frequency, provides the dynamic power dissipated by the device without the load current.

Equations 3 through 7 can be used to calculate total power for CMOS, bipolar, and BiCMOS devices:

$$P_T = P_{S(\text{static})} + P_{D(\text{dynamic})} \qquad \textbf{(3)}$$

CMOS

AC (CMOS-level inputs)

$$P_S = V_{CC} \times I_{CC}$$
$$P_D = \left[\left(C_{pd} \times f_i\right) + \left(C_L \times f_o\right)\right]{V_{CC}}^2 \times N_{SW} \quad (4)$$

ACT (TTL-level inputs)

$$P_S = V_{CC}[I_{CC} + (N_{TTL} \times \Delta I_{CC} \times DC_d)]$$
$$P_D = \left[\left(C_{pd} \times f_i\right) + \left(C_L \times f_o\right)\right]{V_{CC}}^2 \times N_{SW} \quad (5)$$

BiCMOS/Bipolar

$$P_S = V_{CC}\left[DC_{en}\left(N_H \times \frac{I_{CCH}}{N_T} + N_L \times \frac{I_{CCL}}{N_T}\right) + (1 - DC_{en})I_{CCZ} + (N_{TTL} \times \Delta I_{CC} \times DC_d)\right] \quad (6)$$

Note: $\Delta I_{CC} = 0$ for bipolar devices

$$P_D = [DC_{en} \times N_{sw} \times V_{CC} \times f_1 \times (V_{OH} - V_{OL}) \times C_L] + \left[DC_{en} \times N_{sw} \times V_{CC} \times f_2 \times \left(\frac{mA}{MHz \times bit}\right)\right] \times 10^{-3} \quad (7)$$

Where:

V_{CC}	=	Supply voltage (V)
I_{CC}	=	Power-supply current (A) (from the data sheet)
I_{CCL}	=	Power-supply current (A) when outputs are in low state (from the data sheet)
I_{CCH}	=	Power-supply current (A) when outputs are in high state (from the data sheet)
I_{CCZ}	=	Power-supply current (A) when outputs are in high-impedance state (from the data sheet)
ΔI_{CC}	=	Power-supply current (A) when inputs are at a TTL level (from the data sheet)
DC_{en}	=	% duty cycle enabled (50% = 0.5)
DC_d	=	% duty cycle of the data (50% = 0.5)
N_H	=	Number of outputs in high state
N_L	=	Number of outputs in low state
N_{sw}	=	Total number of outputs switching
N_T	=	Total number of outputs
f_i	=	Input frequency (Hz)
f_o	=	Output frequency (Hz)
f_1	=	Operating frequency (Hz)
f_2	=	Operating frequency (MHz)
V_{OH}	=	Output voltage (V) in high state
V_{OL}	=	Output voltage (V) in low state
C_L	=	External load capacitance (F)
mA/(MHz × bit)	=	Slope of the I_{CC} versus frequency curve

Thermal-Resistance Values

Design trends requiring board size reduction have made way for circuit manufacturers to produce fine-pitch packages that appear to threaten the reliability of systems due to further thermal constraints. As a leader in packaging technology, TI has done considerable research into the validity of traditional thermal measurements and data provided by circuit manufacturers.

Unlike data-sheet parameters, where the industry has adopted a standard load for measurement (50 pF, 500 Ω), the measurement of Θ_{JA} has no standard to which all manufacturers comply. The problem facing the designer wishing to make comparisons of thermal data from several manufacturers is that this could be an apples-to-oranges type comparison. As a result, a software package has been developed at TI to allow designers to obtain thermal data based on their specific application.

The validity and usefulness of the traditional approach to presenting Θ_{JA} values became a pressing issue when TI and another manufacturer measured an identical package and obtained results that varied by 40%. Extensive research led to the conclusion that the methodology used to measure Θ_{JA} did not cause the discrepancy but the physical aspects such as trace length, trace width, number of devices per board, and proximity of the other devices did.

To demonstrate the extreme impact of trace length alone, Figure 6 shows the Θ_{JA} values for TI's 48-pin SSOP at 0 LFMP and 250 LFMP with varying trace lengths. The 48-pin SSOP is shown in Figure 1 for a side-by-side comparison with the standard 24-pin SOIC, the 24-pin SSOP, and the 100-pin TQFP. The data in Figure 6 clearly shows the need for more complete thermal data, not simply a single data point.

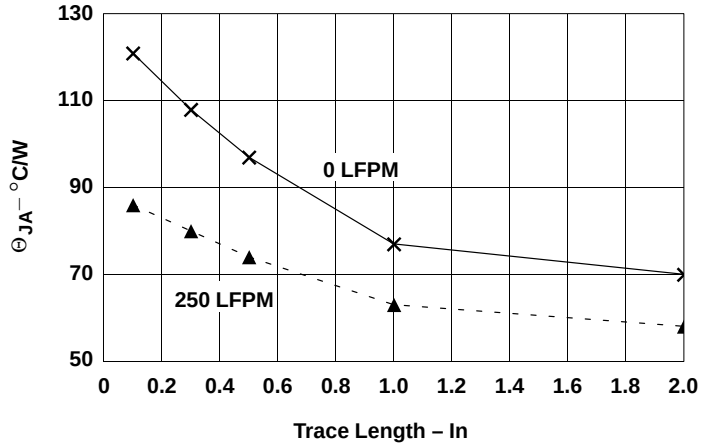


Figure 6. 48-Pin SSOP Θ_{JA} Versus Trace Length

There are other methods to lower the Θ_{JA} of a device. Using heatsinks or blowing air across a device certainly improves the ability to remove heat from its surface. Figure 7 provides Θ_{JA} data for the 48-pin SSOP with trace lengths of 200 mils and 1 inch while varying the amount of air flow. Although many applications tend to limit the amount of air flow, excellent benefits are possible with increased air flow.

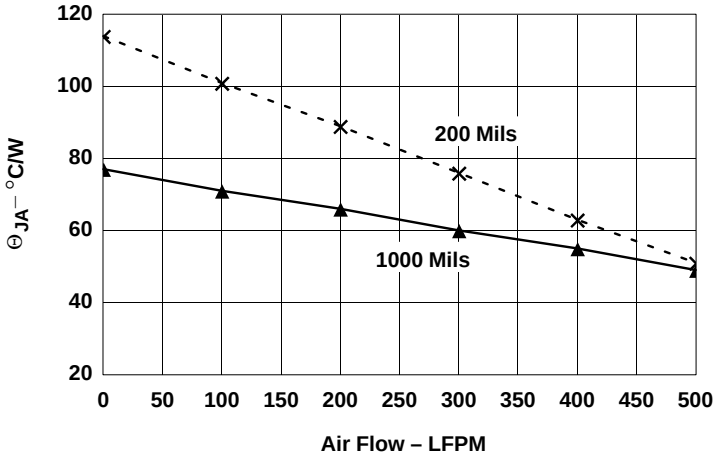
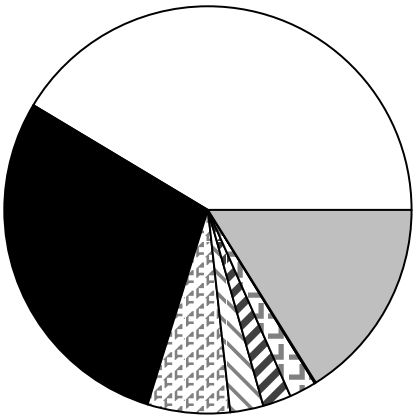


Figure 7. 48-Pin SSOP Θ_{JA} Versus Air Flow

Several variables that have a direct effect on Θ_{JA} values were compared and results are shown in Figure 8. Surprisingly, the major contributing factor is trace length, not air flow. Once again, this validates the need for improvement, not necessarily in the test methodology used to calculate Θ_{JA} values, but certainly in the way those values are provided.



VARIABLE	RANGE	% CONTRIBUTION
Trace Length	75 mils – 2000 mils	41.4
Air Flow	0 LFM – 500 LFM	28.8
Board Extension After Trace	0 mils – 400 mils	6.5
Board Extension After Package End	0 mils – 755 mils	2.6
Trace Thickness	1 oz – 2 oz	2.2
Trace Width	3 mils – 15 mils	2.1
Power	0.5 W – 1.5 W	0.1
Total Interactions Between Factors		16.3

Figure 8. 48-/56-Pin SSOP K-Factor Board Modeling

TI provides Θ_{JA} values for a variety of packages (including the SOIC, SSOP, and QSOP) in a user-friendly software package. The program allows designers to specify their conditions, such as trace length, air flow, proximity of other devices, and trace width in order to obtain realistic thermal solutions.

Summary

Adverse effects of increased power densities can be offset by decreasing the in-use junction temperatures of devices and by good thermal design practices.

Power consumption, which increases with greater functionality and higher operating frequencies, can be held to acceptable levels by careful selection of the logic family and duty cycle. When calculating power consumption, which varies among logic families, both static and dynamic currents must be taken into account.

Thermal resistance values vary widely among circuit manufacturers. Although there is no industry standard for measuring this parameter, variations in results are attributable to physical aspects of the circuit board rather than testing methodology. TI provides software to aid designers in obtaining realistic solutions for their applications.

References

Thermal Software

Contact the factory at (903) 868-7682.

Power Dissipation

*Advanced CMOS Logic Designer's Handboo*k, 1988, Texas Instruments Incorporated, literature number SCAA001B

SSOP Designer's Handbook, 1991, Texas Instruments Incorporated, literature number SCYA001