FIFO Memories: Fine-Pitch Surface-Mount Manufacturability

First-In, First-Out Technology

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Introduction

Recent advances in semiconductor processing and packaging have produced highly integrated, fine-pitch devices to satisfy the demand for smaller systems. With the trend towards higher chip complexity occupying less board space, device manufacturers must increase bit density while decreasing package size. To accommodate these requirements, manufacturers have two choices: increase bit density, keeping the number of pins constant while reducing pitch and area, or reduce the package lead pitch, keeping area constant while increasing pin count. Manufacturers of hand-held and laptop computers and data communications and telecommunications equipment require the use of fine-pitch packages to build and maintain a competitive advantage.

Improved Function Density

Texas Instruments (TI) provides five types of fine-pitch plastic surface-mount packages for its FIFO product line (see Table 1). Each of these surface-mount packages has lead-to-lead spacing less than or equal to 0.635 mm (0.025 in.). All of these packages offer designers critical board-space savings that is required for advanced systems. Compared to the commonly used 68-pin plastic leaded chip carrier (PLCC) for 18-bit FIFOs, TI's Widebus™ package, in either the 56-pin shrink small-outline package (SSOP) or the 80-pin thin quad flat package (TQFP), reduces board space by 70%. A 67% saving of board space is available with TI's 36-bit FIFO family in the 120-pin TQFP compared to the 132-pin plastic quad flat package (PQFP).

Table 1. Fine-Pitch Packages

	THIN QUAD FLAT PACKAGE (TQFP)				THIN SHRINK SMALL-OUTLINE PACKAGE (SSOP)
Pin count	64	80	120	132	56
Lead pitch (mm)	0.5	0.5	0.4	0.635	0.635
Footprint (mm)	12×12	14×14	16×16	28×28	10.35×18.42
Board area (mm^2)	144	196	256	784	190.6
Package suffix	PM	PN	PCB	PQ	DL

Manufacturing

Manufacturers are currently employing high-volume board-assembly techniques using standard lead pitches of 0.5 mm (20 mils) and greater. However, as lead pitch continues to decrease, questions must be asked of both the manufacturer and the supplier:

Are fine-pitch packaging capabilities available?

Does production equipment have sufficient accuracy to produce high-volume, high-quality parts?

Do the manufacturing personnel have experience in high-volume, high-quality production using fine-pitch packaging?

Have the testability issues of fine-pitch packaging been considered?

Standard processing techniques such as those used with surface-mount rigid-lead packages become difficult with fine-pitch packaging. Manufacturing issues may arise from compromises in screen-printing techniques, solder board/lead coplanarity, placement-accuracy requirements of components, and solder deposition methods (e.g., mass reflowing). All of these factors can result in shorts or opens due to poor placement, too much solder, or not enough solder. These issues influence the overall yield and reliability of the product.

Equipment for the placement of fine-pitch packaging must feature a highly accurate positioning system. Placement accuracy for fine-pitch packages must increase as lead pitch decreases. Misaligned packages and boards greatly reduce production yields as well as throughput. Systems that feature state-of-the-art machine vision, align and inspect leads, and calculate registration with an extremely high degree of accuracy and repeatability, ensure high production yields. There must also be careful control over the Z-axis pressure when placing these fine-pitch packages to protect the lead coplanarity. Currently, there are systems available with accurate placement as fine as 0.1-mm pitch.

One of the most critical issues facing the manufacturer is the reliability of the footprint design. Constraints include the length and width of the footprint and the amount of solder paste used to produce a good joint. If too much solder is used, the footprint can bridge, causing a short (see Table 2). The minute dimensions associated with fine-pitch packages require that the footprint be drawn to the highest level of accuracy in order to ensure consistent reliability. Board assemblers must be able to match the footprint with the same level of accuracy and repeatability.

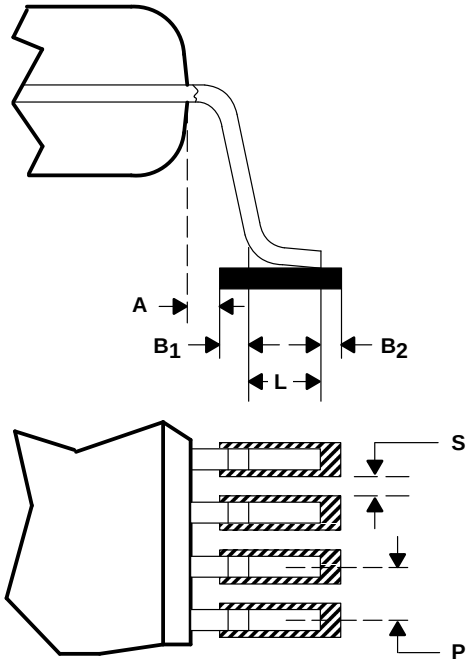
Table 2. Defect Causes and Effects

DEFECT	CONTROL
Solder bridging	Control the solder-paste quantity
Open circuits	Control solder-paste thickness and maintain lead coplanarity
Shorts and opens	Control equipment accuracy in the placement of parts

As previously discussed, the key to ensuring high yield is an accurate footprint pattern. Many manufacturers request footprint patterns and dimensions to assist in their board assembly. There are several factors to consider when designing a footprint pattern to ensure reliability:

- Device design – JEDEC or EIAJ Standard
- PWB – foil thickness, number of layers, supplier's capabilities
- Solder paste – type, solder mesh
- Printer – manufacturer, standoff control, squeegee pressure
- Print mask – type (stencil/mesh), tension, bias
- Reflow process – preheat, temperature, dwell, etc.

The key dimensions for designing an accurate footprint layout are shown in Figure 1.



A = Distance Package Edge to End of Pad
B_1 = Pad Extension Beyond Heel of Foot
B_2 = Pad Extension Beyond Toe of Foot
L = Lead Foot Length
P = Lead Pitch
S = Distance From Center of Pin to Center of Pin

Figure 1. Footprint Diagram

Palladium-Plated Lead Frames

Another area for manufacturers to investigate is metallization, or bonding of the leads to the circuit board with solder. There are several widely used localized reflow techniques including hand soldering, hot bar, focused infrared (IR), and laser. With each technique, heat is applied to the leads until the solder melts. When the heat source is removed, the solder cools forming the joint. Each manufacturer must make the choice between precision point-to-point systems (one chip at a time) and the speed of gang bonding (multiple chip bonding). Another area of metallization to consider is preplating of the leads by the device manufacturer. TI has begun to implement palladium (Pd) lead plating on many fine-pitch packages. These efforts began with joint testing of palladium-plated leads with several large computer and telecom customers in 1987. Since then, TI has begun high-volume manufacturing with over five billion palladium-plated devices in the field.

Palladium preplating is essentially a nickel- (Ni) plated lead frame that has a minimum of 3 micro inches (0.076 micron) of Pd. The Pd finish protects the Ni from oxidation and eliminates the need for silver spotting. Silver (Ag) spots are used to attach the fine wires from the die to the lead frames. However, the silver can migrate over time to form extraneous electrical contacts that greatly impact reliability. Many problems associated with fine-pitch manufacturing can be eliminated with palladium preplating:

- Reduces excess solder
- Excellent Pd wetting characteristics
- Reduced handling
- Improved package integrity
- Reduced mechanical damage
- Tarnish resistant
- Compatible with existing assembly processes
- Excellent adhesion to mold compounds

Table 3 shows the results of a solder-joint strength test comparing Pd solder joints to traditional solder joints. The results demonstrate an equal performance between the two techniques. Palladium preplating also exhibits adhesion to most mold compounds, which reduces moisture ingress and plastic-to-lead-frame delimitation.

Table 3. Results of Soldered Joint Strength

SAMPLE	HOURS OF HEAT AGING			
	0 HR	8 HR	16 HR	24 HR
3 microinches Pd	5.17 lbf	5.95 lbf	5.85 lbf	4.71 lbf
Solder dip	5.07 lbf	4.51 lbf	5.55 lbf	5.50 lbf

In many cases, the cause for shorts and opens can be attributed to lead coplanarity, or the extent to which all leads lie in a single plane. This holds especially true for fine-pitch packaging due to the smaller geometries and delicate leads. Traditional solder-dipped leads tend to have more pin-to-pin alignment problems than the Pd-plated leads. The Pd-preplated leads have a more conformal and uniform coating than those that are solder dipped since the plating is performed prior to the packaging process (see Figure 4). An increase in coplanarity improves overall circuit reliability. The excellent wetting characteristics of Pd improve the wicking effects of solder and form a better solder joint/fillet. The thin Pd coating and minimal handling reduce the chance of coplanarity problems (i.e., shorts and opens) and also produce uniform solder joints with a minimum amount of solder. Table 4 lists TI's fine-pitch packages that implement Pd plating.

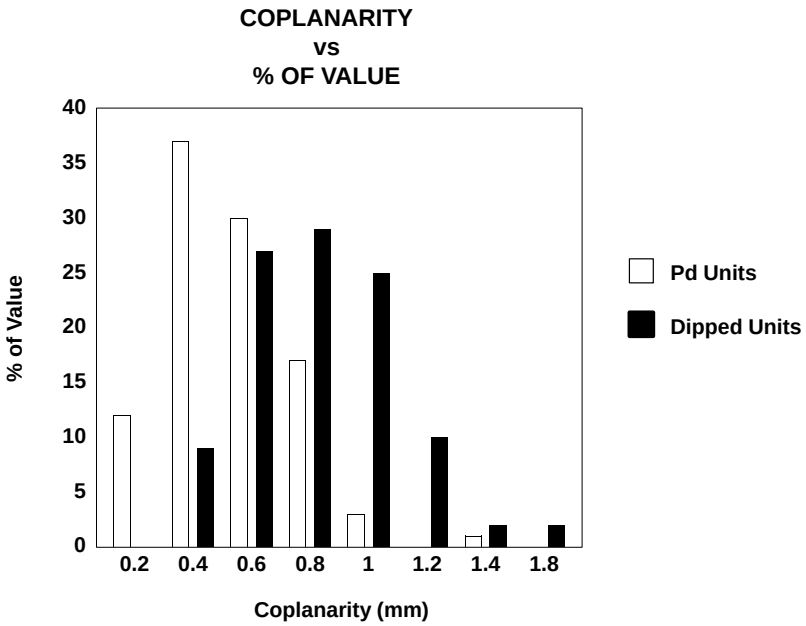


Figure 2. Coplanarity Results

Table 4. Lead-Frame Platings by Package Type

PACKAGE	SUFFIX	LEAD FRAME
132-pin PQFP	PQ	Palladium
120-pin TQFP	PCB	Palladium
80-pin TQFP	PN	Solder
64-pin TQFP	PM	Solder
56-pin SSOP	DL	Palladium

Testability

Another issue introduced by the onset of fine-pitch surface-mount packages involves testing circuit boards. With denser printed-circuit boards heavily populated with fine-pitch surface-mount packages, the issues involved with functional testing should be addressed. One of the most cost-effective solutions is the implementation of boundary-scan methodology defined by the joint test action group (JTAG) and adopted by the IEEE 1149.1 committee. JTAG devices incorporate on-chip test points called boundary-scan cells and utilize a serial-scan protocol through the device. Devices with JTAG can be designed into the datapath and provide the controllability and observability needed to troubleshoot manufacturing defects.

Design/Preproduction Considerations

For designers who wish to implement fine-pitch packaging, TI provides an easy alternative for the development of prototypes and breadboarding. TI has worked with several test-socket manufacturers who provide accurate and easy-to-use through-hole test sockets for all of their surface-mount packaging. In addition to test sockets, TI also offers mechanical packages. These are packages that include lead frames without the silicon and meet all mechanical specifications. Mechanical packages provide an inexpensive means for manufacturing capability studies, machine setup, personnel training, and process-development work (see Table 5).

Table 5. Available Fine-Pitch Test Sockets and Mechanical Packages

SOCKET TYPE	MANUFACTURER	PART NUMBER	DESCRIPTION
64-pin TQFP	Yamaichi	IC51-0644-807	Through hole
56-pin SSOP	Yamaichi	IC51-0562-1514	Through hole
80-pin TQFP	Yamaichi	IC51-0804-808	Through hole
120-pin TQFP	Yamaichi	IC51-1204-1596	Through hole
132-pin PQFP	Yamaichi	IC51-828-KS12338	Through hole

PACKAGE	TI PART NUMBER
64-pin TQFP	SN700870PM
56-pin SSOP	SN250011DLR
80-pin TQFP	SN700871PN
120-pin TQFP	SN700782PCB

Conclusion

Designs that incorporate fine-pitch packages have the advantage of critical board-space reduction. As designers continue to implement higher levels of integration, board space remains at a premium. With the implementation of concurrent engineering practices from design to test to manufacturing, many packaging difficulties can be overcome. Fine-pitch packaging is the designers' easiest option to reduce critical board space without the loss of higher chip integration.

References

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