FIFO Surface-Mount Package Information

First-In, First-Out Technology

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SSPA001A

TEXAS INSTRUMENTS

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Introduction

Texas Instruments provides seven types of plastic surface-mount packages for CMOS FIFO memory devices. These packages and the data bus width that each package can provide are listed in Table 1.

Table 1. Plastic Surface-Mount FIFO Packages

PACKAGE	NO. OF DATA BITS
44-pin PLCC	9
64-pin TQFP	9
56-pin SSOP	18
68-pin PLCC	18
80-pin TQFP	18
80-pin QFP	18
120-pin TQFP	32 or 36

SSOP = shrink small-outline package
PLCC = plastic leaded chip carrier
TQFP = thin quad flat package
QFP = quad flat package

This application report discusses several topics concerning the FIFO packages listed in Table 1:

- The thermal resistance, $R_{\Theta JA}$, and the chip junction temperature of the device
- The need for dry packing to maintain safe moisture levels inside the package
- The three methods used by Texas Instruments for shipping FIFOs to customers
- The package dimensions, including two-dimensional drawings that show areas, heights, and lead pitches
- The area comparison of surface-mount packages used for commercial FIFO memories
- The test sockets available for surface-mount FIFO packages

Thermal Resistance

Thermal resistance is defined as the ability of a package to dissipate heat generated by an electronic device and is characterized by $R_{\Theta JA}$. $R_{\Theta JA}$ is the thermal resistance from the integrated circuit chip junction to the free air (ambient). Units for this parameter are in degrees Celsius per watt. Table 2 lists $R_{\Theta JA}$ for SSOP, PLCC, TQFP, and QFP packages under five different air-flow environments: 0, 100, 200, 250, and 500 linear feet/minute. The chip junction temperature (T_J) can be determined using equation 1.

$$T_J = R_{\Theta JA} \times P_T + T_A \quad \textbf{(1)}$$

Where:

T_J = chip junction temperature (°C)
$R_{\Theta JA}$ = thermal resistance, junction to free-air (°C/watt)
P_T = total power dissipation of the device (watts)
T_A = free-air (ambient) temperature in the particular environment in which the device is operating (°C)

Table 2. Thermal Resistance, $R_{\Theta JA}$, for FIFO Packages

PACKAGE	LEAD FRAME	$R_{\Theta JA}$ (°C/W)				
		0 LFPM	100 LFPM	200 LFPM	250 LFPM	500 LFPM
56-pin SSOP	Copper	94.2	82.2	N/A	70	57.8
44-pin PLCC	Copper	65	N/A	N/A	N/A	N/A
68-pin PLCC	Copper	47.2	43.4	N/A	32.7	27.8
64-pin TQFP	Copper	92.5	87.8	N/A	72.9	57.8
80-pin TQFP	Copper	87.8	79.1	N/A	67.3	54.2
120-pin TQFP†	Copper	49.6	44.3	N/A	38.3	28.6
80-pin QFP	Alloy 42	80	67	61	N/A	N/A

† Heat slug molded inside the package
N/A = not available

The $R_{\Theta JA}$ generally increases with decreasing package size; however, this is not true with the 120-pin SQFP package. A heat slug molded inside the package absorbs a large amount of heat dissipated by the device. As a result, this package provides a relatively low $R_{\Theta JA}$.

Package Moisture Sensitivity

When a plastic surface-mount package is exposed to temperatures typical of furnace reflow, infrared (IR) soldering, or wave soldering (215°C or higher), the moisture absorbed by the package turns to steam and expands rapidly. The stress caused by this expanding moisture results in internal and external cracking of the package that leads to reliability failures. Possible damage includes the delamination of the plastic from the chip surface and lead frame, damaged bonds, cratering beneath the bonds, and external package cracks.

To prevent potential damage, packages that are susceptible to the effects of moisture expansion undergo a process called dry pack. This dry pack process helps to reduce moisture levels inside the package. The process consists of a 24-hour bake at 125°C followed by sealing of the packages in moisture-barrier bags with desiccant to prevent reabsorption of moisture during the shipping and storage processes. These moisture-barrier bags allow a shelf storage of 12 months from the date of seal. Once the moisture-barrier bag is opened, the devices in it must be handled by one of the following four methods, listed in order of preference:

The devices may be mounted within 48 hours in an atmospheric environment of less than 60% relative humidity and less than 30°C.

The devices may be stored outside the moisture-barrier bag in a dry-atmospheric environment of less than 20% relative humidity until future use.

The devices may be resealed in the moisture-barrier bag adding new fresh desiccant to the bag. When the bag is opened again, the devices should be used within the 48-hour time limit or resealed again with fresh desiccant.

The devices may be resealed in the moisture-barrier bag using the original desiccant. This method does not allow the floor life of the devices to be extended. The cumulative exposure time before reflow must not exceed a total of 48 hours.

All plastic surface-mount FIFO devices are tested for moisture sensitivity in accordance with Texas Instruments JESD A112 procedure.

Shipping Methods/Quantities/Dry Pack

Three methods are used by Texas Instruments for shipping FIFOs to customers. These methods are tubes, tape/reel, and trays. The quantities for each of the shipping methods are listed in Table 3. The shipping quantity is defined as the maximum number of packages that can be packed in a single shipping unit (e.g., the maximum number of 56-pin SSOP packages that can be packed in a tube is 20). Whether or not the packages require dry pack before shipping is noted in the dry-pack column.

Table 3. Shipping Methods and Quantities

PACKAGE	SHIPPING METHOD			DRY PACK
	TUBE†	TAPE/REEL†	TRAYS†	
56-pin SSOP	20	500	N/A	No
44-pin PLCC	27	500	N/A	No
68-pin PLCC	18/19‡	250	N/A	Yes
64-pin TQFP	N/A	N/A	160	Yes
80-pin TQFP	N/A	N/A	119	Yes
120-pin TQFP	N/A	N/A	90	Yes
80-pin TQFP	N/A	N/A	50	Yes

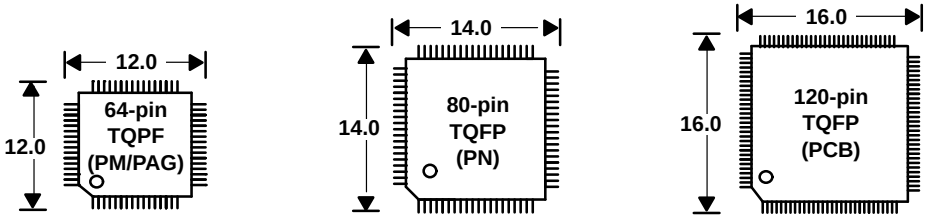
† Texas Instruments reserves the right to change any of the shipping quantities at any time without notice.

‡ Eighteen packages can be packed in a single tube when pin is used as a tap or nineteen packages can be packed in a tube when plug is used as a tap.

N/A = not applicable

Package Dimensions and Area Comparison

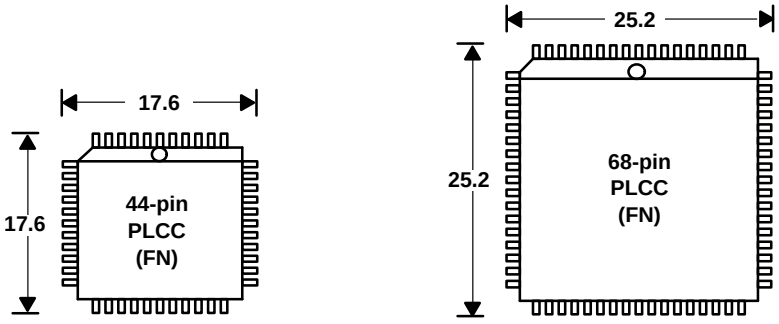
Figure 1 contains two-dimensional drawings of the seven available surface-mount FIFO packages. For detailed mechanical drawings of these packages, please refer to the mechanical drawing section of the 1994 *High-Performance FIFO Memories Data Book*, literature #SCAD003B.



Area: 144.00 mm^2
Height: 1.50 mm (PM)
Height: 1.0 mm (PAG)
Lead Pitch: 0.5 mm

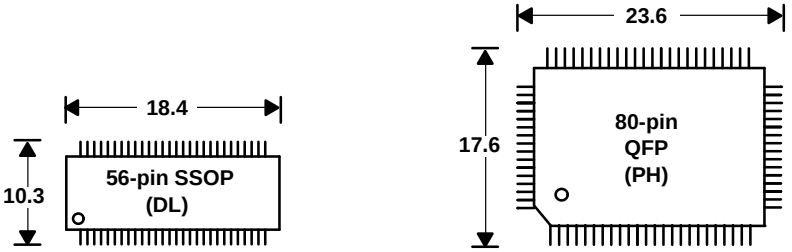
Area: 196.00 mm^2
Height: 1.50 mm
Lead Pitch: 0.5 mm

Area: 256.00 mm^2
Height: 1.6 mm
Lead Pitch: 0.4 mm



Area: 309.80 mm^2
Height: 4.37 mm
Lead Pitch: 1.27 mm

Area: 635.04 mm^2
Height: 4.37 mm
Lead Pitch: 1.27 mm



Area: 189.50 mm^2
Height: 2.59 mm
Lead Pitch: 0.635 mm

Area: 415.40 mm^2
Height: 2.95 mm
Lead Pitch: 0.8 mm

Figure 1. Package Dimensions

Figure 2 shows the area comparison of surface-mount packages for FIFOs from Texas Instruments and other FIFO vendors.

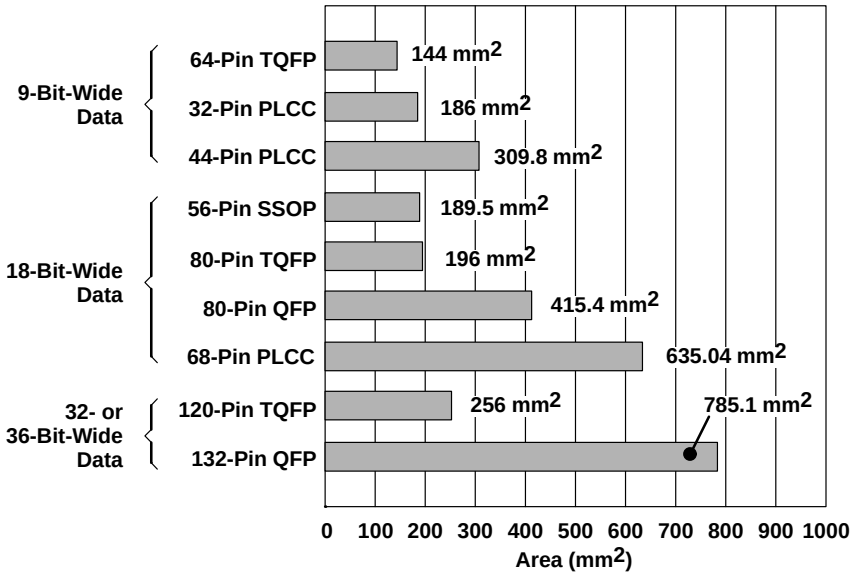


Figure 2. Surface-Mount Package Area Comparison

Test Sockets

For prototype development of a system, it is often an advantage to have sockets for surface-mount products. Test sockets available for use with Texas Instruments FIFO packages are listed in Table 4. Only one manufacturer is listed for each socket type, although other vendors may offer comparable sockets.

Table 4. Test Sockets for FIFO Packages

PACKAGE	MANUFACTURER	NUMBER	DESCRIPTION
56-pin SSOP	Yamaichi	IC51-0562-1387	Solder through hole
44-pin PLCC	NEY	6044	Solder through hole
68-pin PLCC	NEY	6068	Solder through hole
64-pin TQFP	Yamaichi	IC51-0644-807	Solder through hole
80-pin TQFP	Yamaichi	IC51-0804-808	Solder through hole
120-pin TQFP	Yamaichi	IC51–1204–1596	Solder through hole
80-pin QFP	Yamaichi	IC51-0804-394	Solder through hole

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