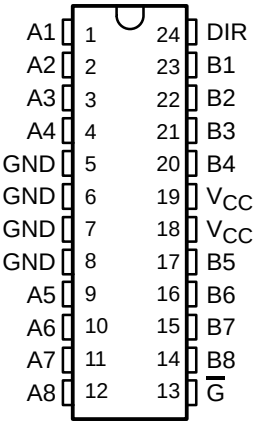
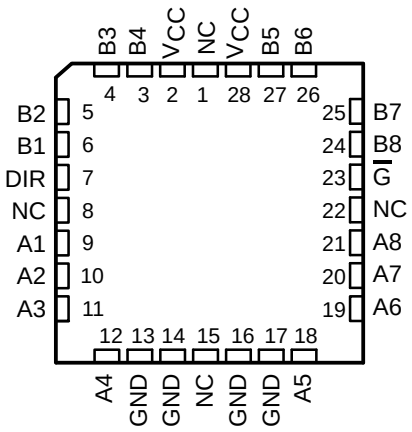
- **Bidirectional Bus Transceivers in High-Density 24-Pin Packages**
- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin $V_{CC}$ and GND Configurations to Minimize High-Speed Switching Noise**
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

**54ACT11640 . . . JT PACKAGE**
**74ACT11640 . . . DW OR NT PACKAGE**
**(TOP VIEW)**




**54ACT11640 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input $\overline{G}$ is used to disable the device so the buses are effectively isolated.

The 54ACT11640 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT11640 is characterized for operation from – 40°C to 85°C.

**FUNCTION TABLE**

| CONTROL INPUTS | | OPERATION |
|---|---|---|
| $\overline{G}$ | DIR | |
| L | L | $\overline{B}$ data to A bus |
| L | H | $\overline{A}$ data to B bus |
| H | X | Isolation |

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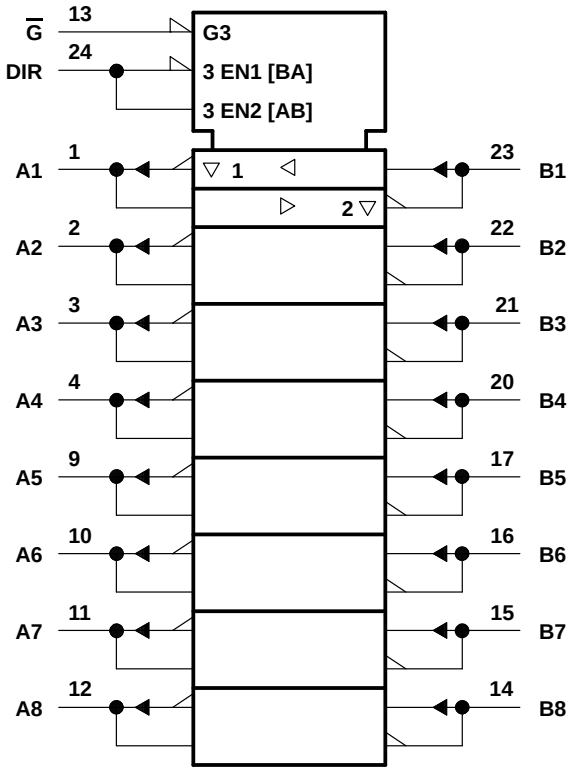
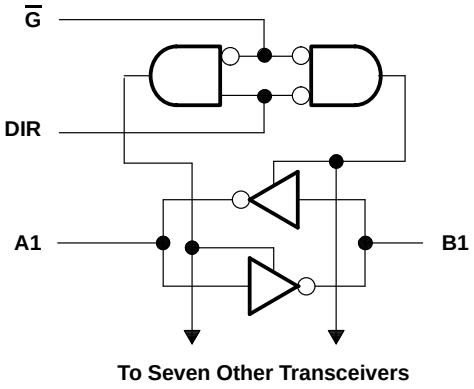
## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 6 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{CC}$) . . . . . ± 20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ± 50 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ± 50 mA
Continuous current through $V_{CC}$ or GND . . . . . ± 200 mA
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## recommended operating conditions

| | | 54ACT11640 | | | 74ACT11640 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input voltage | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | | –24 | | | –24 | mA |
| $I_{OL}$ | Low-level output current | | | 24 | | | 24 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 0 | | 10 | 0 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | | 125 | – 40 | | 85 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | 54ACT11640 | | 74ACT11640 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = – 50 μA | 4.5 V | 4.4 | | | 4.4 | | 4.4 | | V |
| | | | 5.5 V | 5.4 | | | 5.4 | | 5.4 | | |
| | | $I_{OH}$ = – 24 mA | 4.5 V | 3.94 | | | 3.7 | | 3.8 | | |
| | | | 5.5 V | 4.94 | | | 4.7 | | 4.8 | | |
| | | $I_{OH}$ = – 50 mA† | 5.5 V | | | | 3.85 | | | | |
| | | $I_{OH}$ = – 75 mA† | 5.5 V | | | | | | 3.85 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 5.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 24 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | | 5.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 50 mA† | 5.5 V | | | | | 1.65 | | | |
| | | $I_{OL}$ = 75 mA† | 5.5 V | | | | | | | 1.65 | |
| $I_{OZ}$ | A or B ports‡ | $V_O = V_{CC}$ or GND | 5.5 V | | | ± 0.5 | | ± 10 | | ± 5 | μA |
| $I_I$ | $\overline{G}$ or DIR | $V_I = V_{CC}$ or GND | 5.5 V | | | ± 0.1 | | ± 1 | | ± 1 | μA |
| $I_{CC}$ | | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 8 | | 160 | | 80 | μA |
| $\Delta I_{CC}$§ | | One input at 3.4 V, Other inputs at GND or $V_{CC}$ | 5.5 V | | | 0.9 | | 1 | | 1 | mA |
| $C_i$ | $\overline{G}$ or DIR | $V_I = V_{CC}$ or GND | 5 V | | 4 | | | | | | pF |
| $C_{io}$ | A or B ports | $V_O = V_{CC}$ or GND | 5 V | | 12 | | | | | | pF |

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter $I_{OZ}$ includes the input leakage.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

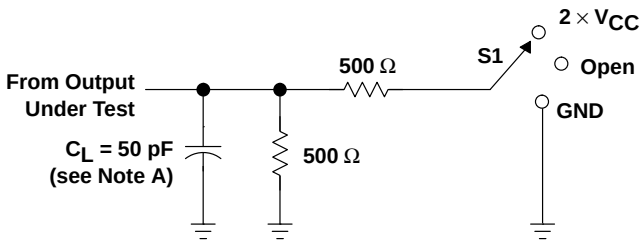
### switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ = 25°C | | | 54ACT11640 | | 74ACT11640 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 1.5 | 6.3 | 9.6 | 1.5 | 11 | 1.5 | 10.5 | ns |
| $t_{PHL}$ | | | 1.5 | 5.7 | 8.6 | 1.5 | 10 | 1.5 | 9.5 | |
| $t_{PZH}$ | $\overline{G}$ | A or B | 1.5 | 8.8 | 12.2 | 1.5 | 14.2 | 1.5 | 13.4 | ns |
| $t_{PZL}$ | | | 1.5 | 8.4 | 12.3 | 1.5 | 14.5 | 1.5 | 13.6 | |
| $t_{PHZ}$ | $\overline{G}$ | A or B | 1.5 | 9.1 | 12.9 | 1.5 | 14.5 | 1.5 | 13.9 | ns |
| $t_{PLZ}$ | | | 1.5 | 9.6 | 13.1 | 1.5 | 15 | 1.5 | 14.2 | |

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

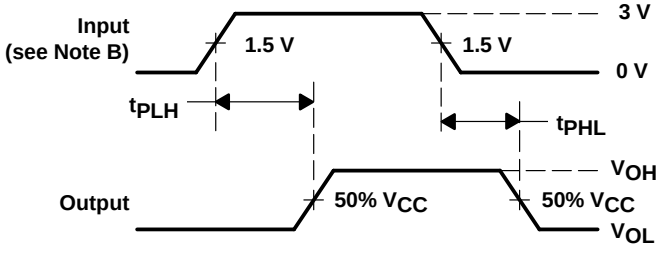
| PARAMETER | | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per transceiver | Outputs enabled | $C_L$ = 50 pF, | f = 1 MHz | 45 | pF |
| | | Outputs disabled | | | 12 | |

## PARAMETER MEASUREMENT INFORMATION

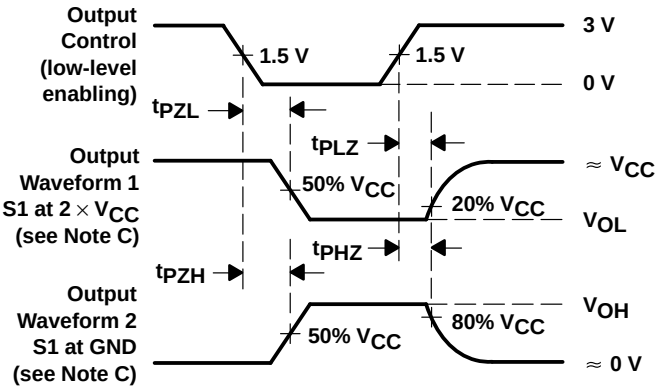



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

LOAD CIRCUIT




VOLTAGE WAVEFORMS




VOLTAGE WAVEFORMS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

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