

# 74AC11648 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS114 – MARCH 1990 – REVISED APRIL 1993

- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Inverting Data Paths
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin  $V_{CC}$  and GND Configurations Minimize High-Speed Switching Noise
- **EPIC™** (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

## description

The 74AC11648 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 74AC11648.

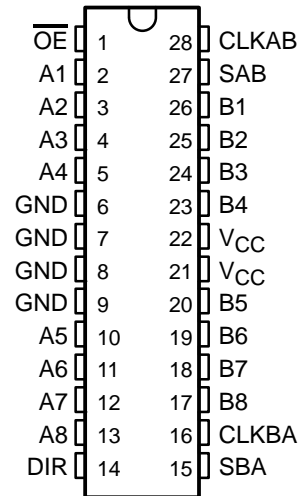
Output-enable ( $\overline{OE}$ ) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus will receive data when  $\overline{OE}$  is low. In the isolation mode ( $\overline{OE}$  high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The 74AC11648 is characterized for operation from -40°C to 85°C.

DW OR NT PACKAGE  
(TOP VIEW)



EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1993, Texas Instruments Incorporated

# 74AC11648

## OCTAL BUS TRANSCEIVER AND REGISTER

### WITH 3-STATE OUTPUTS

SCAS114 – MARCH 1990 – REVISED APRIL 1993

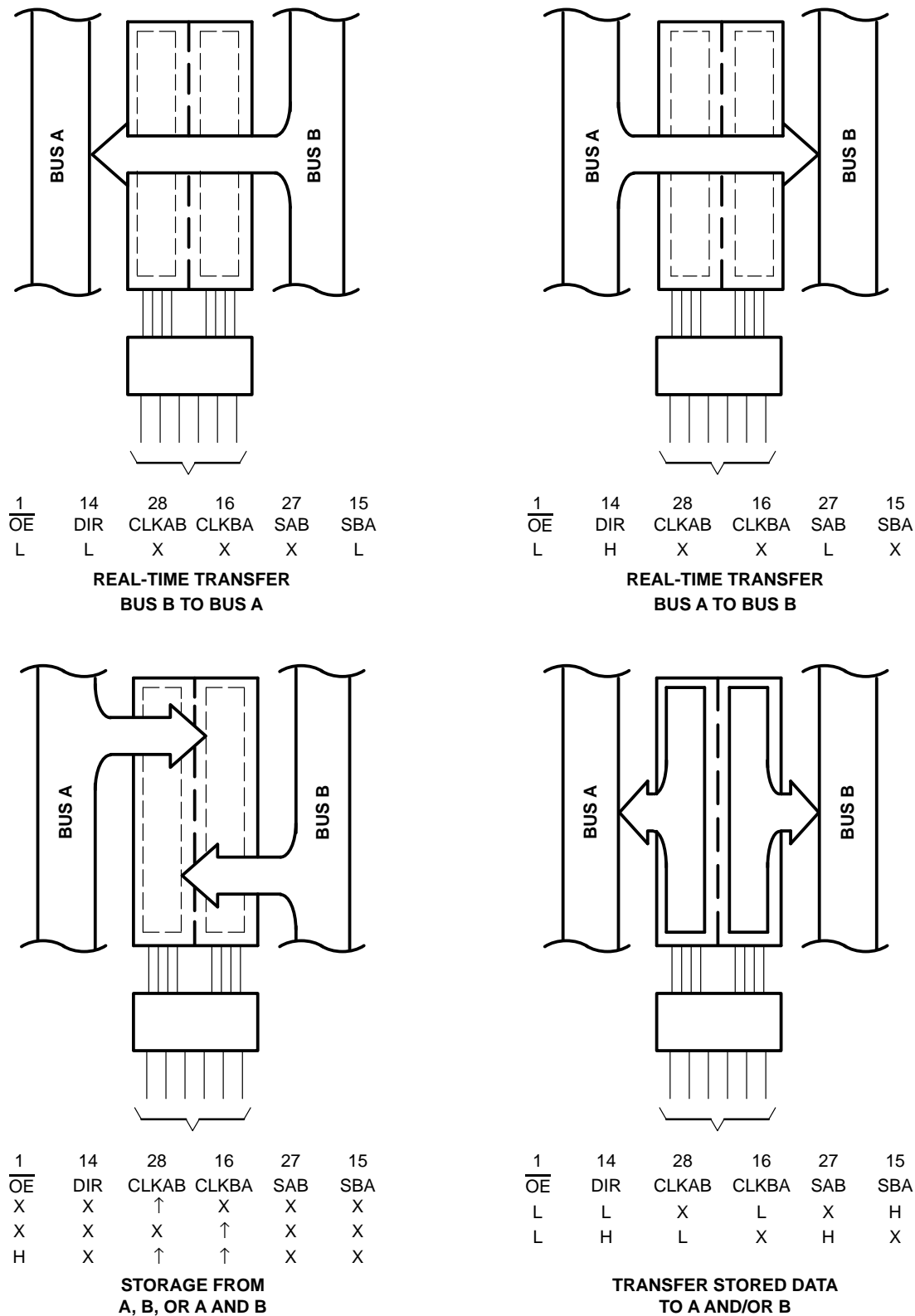


Figure 1. Bus-Management Functions

**74AC11648**  
**OCTAL BUS TRANSCEIVER AND REGISTER**  
**WITH 3-STATE OUTPUTS**

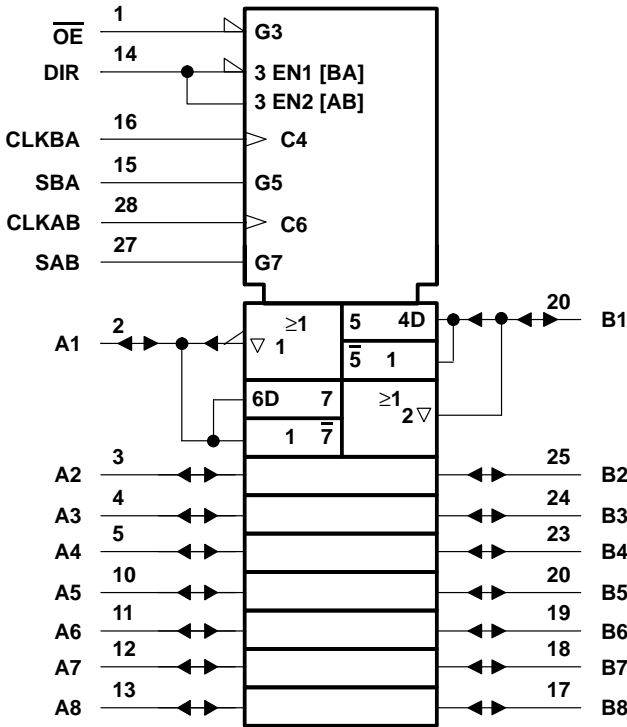
SCAS114 – MARCH 1990 – REVISED APRIL 1993

**FUNCTION TABLE**

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	$\uparrow$	X	X	X	Input	Unspecified <sup>†</sup>	Store A, B unspecified <sup>†</sup>
X	X	X	$\uparrow$	X	X	Unspecified <sup>†</sup>	Input	Store B, A unspecified <sup>†</sup>
H	X	$\uparrow$	$\uparrow$	X	X	Input	Input	Store A and B data
H	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time $\overline{B}$ data to A bus
L	L	X	L	X	H	Output	Input	Stored $\overline{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real-time $\overline{A}$ data to B bus
L	H	L	X	H	X	Input	Output	Stored $\overline{A}$ data to B bus

<sup>†</sup> The data output functions may be enabled or disabled by various signals at the  $\overline{OE}$  and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

**logic symbol<sup>‡</sup>**



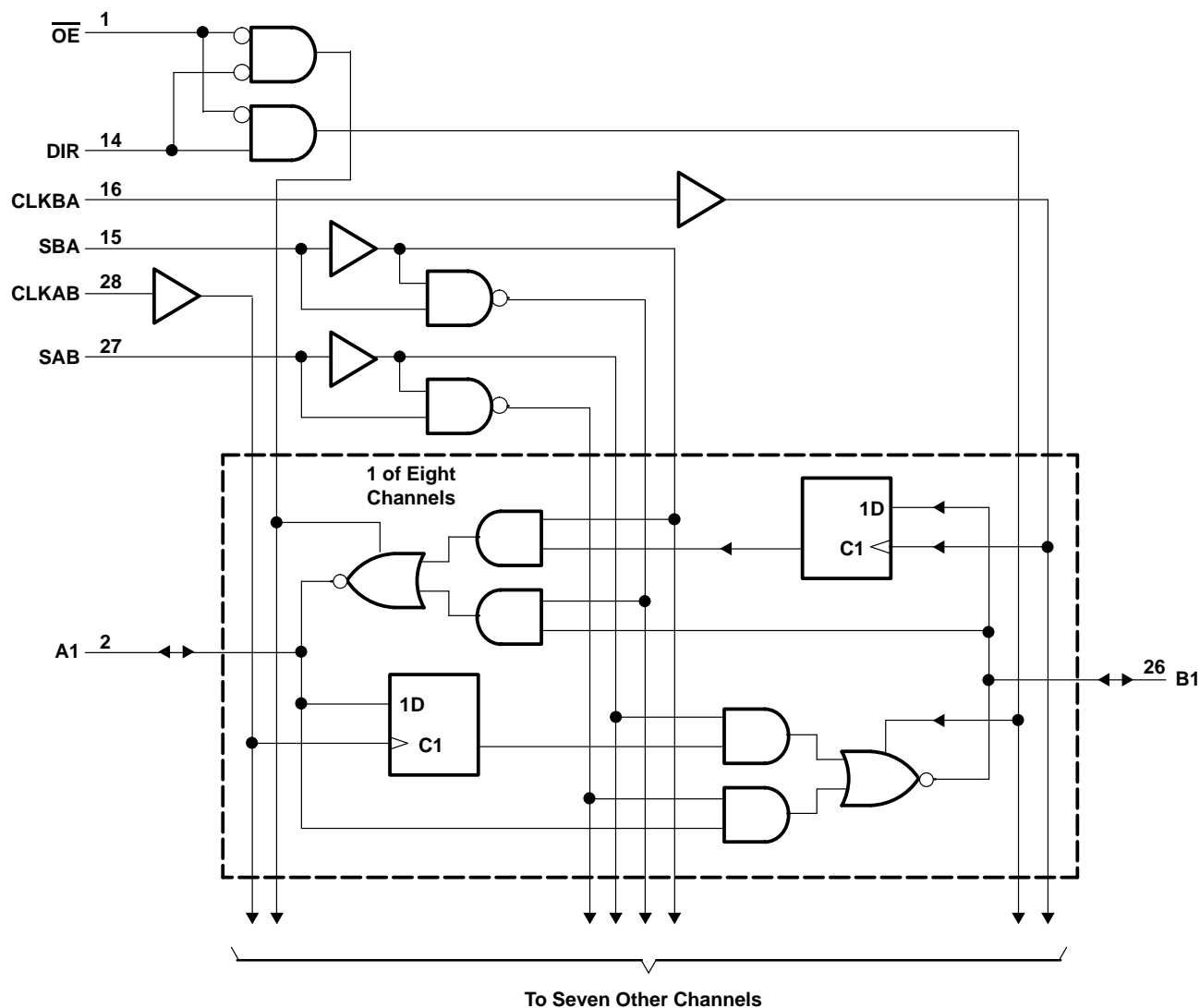
<sup>‡</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# 74AC11648

## OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS114 – MARCH 1990 – REVISED APRIL 1993

### logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through $V_{CC}$ or GND	±200 mA
Storage temperature range	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

**74AC11648**  
**OCTAL BUS TRANSCEIVER AND REGISTER**  
**WITH 3-STATE OUTPUTS**

SCAS114 – MARCH 1990 – REVISED APRIL 1993

**recommended operating conditions**

			MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage		3	5	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 3\text{ V}$	2.1			V
		$V_{CC} = 4.5\text{ V}$	3.15			
		$V_{CC} = 5.5\text{ V}$	3.85			
$V_{IL}$	Low-level input voltage	$V_{CC} = 3\text{ V}$			0.9	V
		$V_{CC} = 4.5\text{ V}$			1.35	
		$V_{CC} = 5.5\text{ V}$			1.65	
$V_I$	Input voltage		0		$V_{CC}$	V
$V_O$	Output voltage		0		$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 3\text{ V}$			-4	mA
		$V_{CC} = 4.5\text{ V}$			-24	
		$V_{CC} = 5.5\text{ V}$			-24	
$I_{OL}$	Low-level output current	$V_{CC} = 3\text{ V}$			12	mA
		$V_{CC} = 4.5\text{ V}$			24	
		$V_{CC} = 5.5\text{ V}$			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
$T_A$	Operating free-air temperature		-40		85	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$V_{OH}$		$I_{OH} = -50\text{ }\mu\text{A}$	3 V	2.9			2.9		V
			4.5 V	4.4			4.4		
			5.5 V	5.4			5.4		
		$I_{OH} = -4\text{ mA}$	3 V	2.58			2.48		
			4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
$V_{OL}$		$I_{OL} = 50\text{ }\mu\text{A}$	3 V			0.1		0.1	V
			4.5 V			0.1		0.1	
			5.5 V			0.1		0.1	
		$I_{OL} = 12\text{ mA}$	3 V			0.36		0.44	
			4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
$I_I$	Control inputs	$V_I = V_{CC}$ or GND	5.5 V				$\pm 0.1$	$\pm 1$	$\mu\text{A}$
$I_{OZ}^\dagger$	A or B ports	$V_O = V_{CC}$ or GND	5.5 V				$\pm 0.5$	$\pm 5$	$\mu\text{A}$
$I_{CC}$		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V				8	80	$\mu\text{A}$
$C_i$	Control inputs	$V_I = V_{CC}$ or GND	5 V				4.5		pF
$C_{io}$	A or B ports	$V_O = V_{CC}$ or GND	5 V				12		pF

$^\dagger$  Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

$^\ddagger$  For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

# 74AC11648

## OCTAL BUS TRANSCEIVER AND REGISTER

### WITH 3-STATE OUTPUTS

SCAS114 – MARCH 1990 – REVISED APRIL 1993

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 2)**

		$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
$f_{\text{clock}}$	Clock frequency	0	40	0	40	MHz
$t_w$	Pulse duration, CLK high or low	12.5		12.5		ns
$t_{\text{su}}$	Setup time, A or B before CLKAB $\uparrow$ or CLKBA $\uparrow$	6.5		6.5		ns
$t_h$	Hold time, A or B after CLKAB $\uparrow$ or CLKBA $\uparrow$	0		0		ns

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 2)**

		$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
$f_{\text{clock}}$	Clock frequency	0	90	0	90	MHz
$t_w$	Pulse duration, CLK high or low	5.6		5.6		ns
$t_{\text{su}}$	Setup time, A or B before CLKAB $\uparrow$ or CLKBA $\uparrow$	4.5		4.5		ns
$t_h$	Hold time, A or B after CLKAB $\uparrow$ or CLKBA $\uparrow$	1		1		ns

**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$f_{\text{max}}$			40			40		MHz
$t_{\text{PLH}}$	A or B	B or A	3	8.7	12.6	3	14.3	ns
$t_{\text{PHL}}$			3.8	9.3	14.4	3.8	15.9	
$t_{\text{PZH}}$	$\overline{\text{OE}}$	A or B	5	11.1	17.2	5	19.4	ns
$t_{\text{PZL}}$			5.2	12.8	20.5	5.2	23	
$t_{\text{PHZ}}$	$\overline{\text{OE}}$	A or B	4.1	7.2	9.9	4.1	10.6	ns
$t_{\text{PLZ}}$			3.7	6.5	9.1	3.7	9.7	
$t_{\text{PLH}}$	CLKBA or CLKAB	A or B	4.3	10.1	15.6	4.3	17.6	ns
$t_{\text{PHL}}$			5.2	11.5	17.6	5.2	19.4	
$t_{\text{PLH}}$	SBA or SAB $\uparrow$ (A or B high)	A or B	3.7	9.1	14.1	3.7	15.8	ns
$t_{\text{PHL}}$			4.5	10.3	15.9	4.5	17.4	
$t_{\text{PLH}}$	SBA or SAB $\uparrow$ (A or B low)	A or B	3.2	8.6	13.6	3.2	15.3	ns
$t_{\text{PHL}}$			4.6	10.3	15.6	4.6	17.1	
$t_{\text{PZH}}$	DIR	A or B	4.9	11.6	18.2	4.9	20.6	ns
$t_{\text{PZL}}$			5.2	14.2	21.6	5.2	24.3	
$t_{\text{PHZ}}$	DIR	A or B	3.8	7.1	10.1	3.8	10.9	ns

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

**74AC11648**  
**OCTAL BUS TRANSCEIVER AND REGISTER**  
**WITH 3-STATE OUTPUTS**

SCAS114 – MARCH 1990 – REVISED APRIL 1993

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$f_{\text{max}}$			90			90		MHz
$t_{\text{PLH}}$	A or B	B or A	2.6	5.6	8.3	2.6	9.5	ns
$t_{\text{PHL}}$			3.2	6.4	9.4	3.2	10.6	
$t_{\text{PZH}}$	$\overline{\text{OE}}$	A or B	4.2	7.8	11.3	4.2	12.8	ns
$t_{\text{PZL}}$			4.1	8.1	12	4.1	13.6	
$t_{\text{PHZ}}$	$\overline{\text{OE}}$	A or B	3.8	6.3	8.6	3.8	9.2	ns
$t_{\text{PLZ}}$			3.5	5.7	7.8	3.5	8.4	
$t_{\text{PLH}}$	CLKBA or CLKAB	A or B	3.6	6.9	10	3.6	11.4	ns
$t_{\text{PHL}}$			4.3	8	11.4	4.3	12.8	
$t_{\text{PLH}}$	SBA or SAB $\dagger$ (A or B high)	A or B	3.1	6.2	9.2	3.1	10.4	ns
$t_{\text{PHL}}$			3.8	7.6	10.4	3.8	11.6	
$t_{\text{PLH}}$	SBA or SAB $\dagger$ (A or B low)	A or B	2.8	6.1	8.9	2.8	10.1	ns
$t_{\text{PHL}}$			3.8	7.3	10.4	3.8	11.6	
$t_{\text{PZH}}$	DIR	A or B	4	8	11.9	4	13.4	ns
$t_{\text{PZL}}$			4.1	8.4	12.7	4.1	14.4	
$t_{\text{PHZ}}$	DIR	A or B	3.5	6.1	8.5	3.5	9.1	ns
$t_{\text{PLZ}}$			3.4	5.9	7.8	3.4	8.4	

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{\text{pd}}$	Power dissipation capacitance per transceiver	Outputs enabled	66	pF
		Outputs disabled	17	

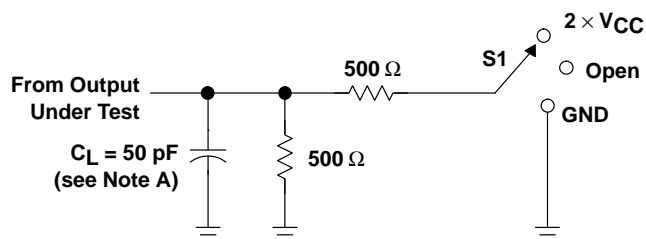
# 74AC11648

## OCTAL BUS TRANSCEIVER AND REGISTER

### WITH 3-STATE OUTPUTS

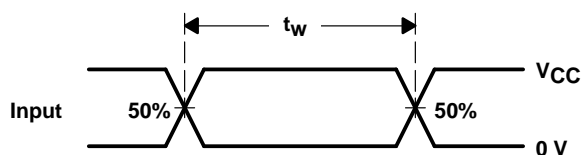
SCAS114 – MARCH 1990 – REVISED APRIL 1993

#### PARAMETER MEASUREMENT INFORMATION

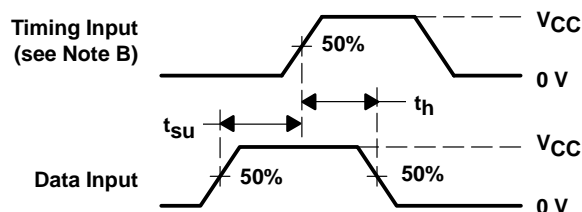


LOAD CIRCUIT

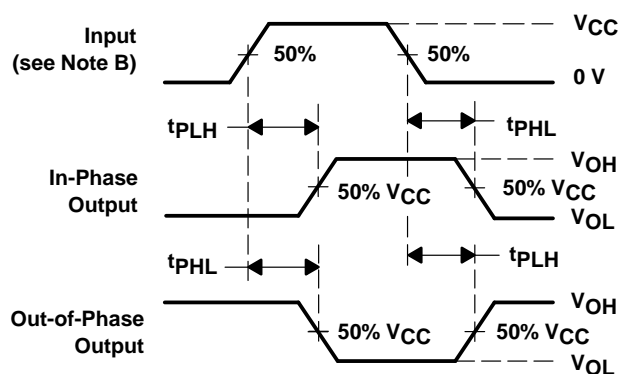
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



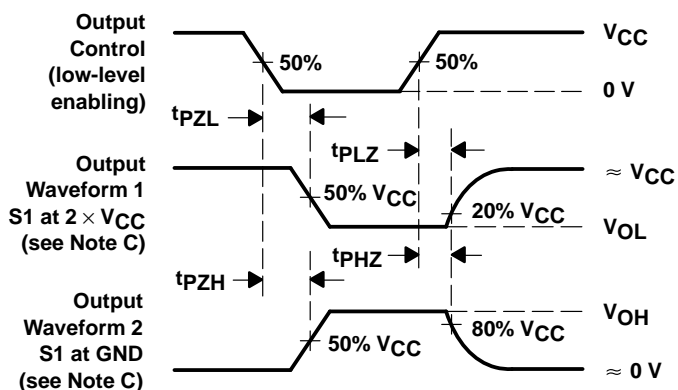
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A.  $C_L$  includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms



## **IMPORTANT NOTICE**

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

**TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.**

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.