

# 74AC16623 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS172 – D3680, JANUARY 1991 – REVISED APRIL 1993

- Member of the Texas Instruments *Widebus™* Family
- Packaged in Plastic 300-mil Shrink Small-Outline Package Using 25-mil Center-to-Center Pin Spacings
- Flow-Through Architecture Optimizes PCB Layout
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- *EPIC™* (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C

## description

The 74AC16623 is a 16-bit transceiver designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing.

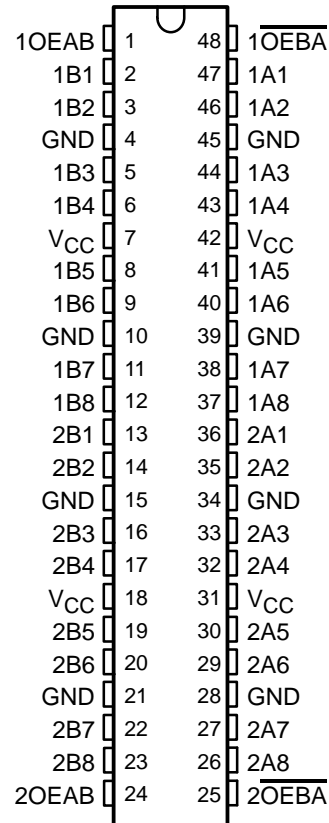
This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the output-enable ( $\overline{OEBA}$  and OEAB) inputs. The output-enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the bus transceiver the capability to store data by simultaneous enabling of  $\overline{OEBA}$  and OEAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, the bus lines will remain at their last states.

The 74AC16623 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 74AC16623 is characterized for operation from –40°C to 85°C.

DL PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each 8-bit section)

INPUTS		OPERATION
$\overline{OEBA}$	OEAB	
L	L	B data to A bus
H	H	A data to B bus
H	L	Isolation
L	H	B data to A bus, A data to B bus

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1993, Texas Instruments Incorporated



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

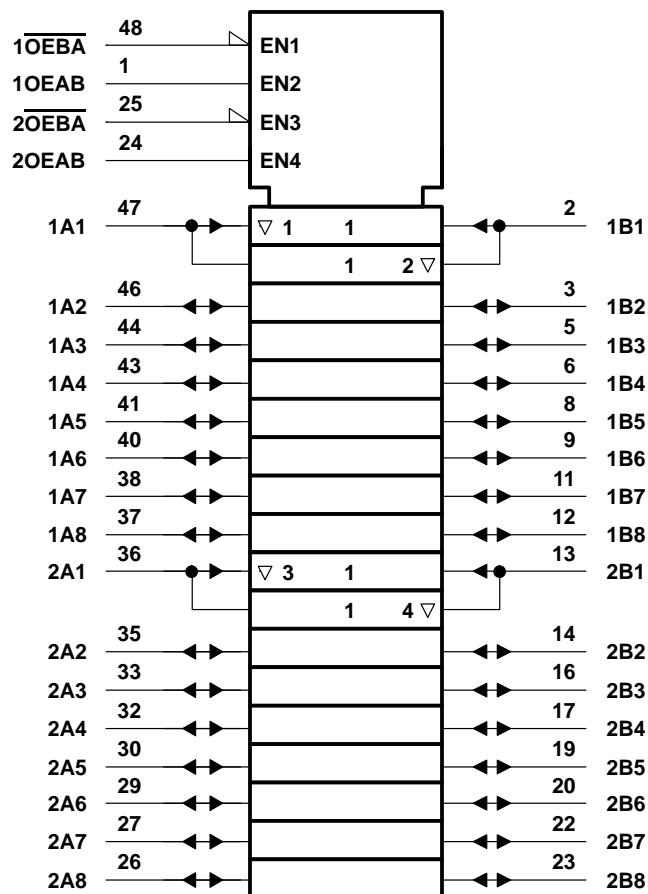
# 74AC16623

## 16-BIT BUS TRANSCEIVER

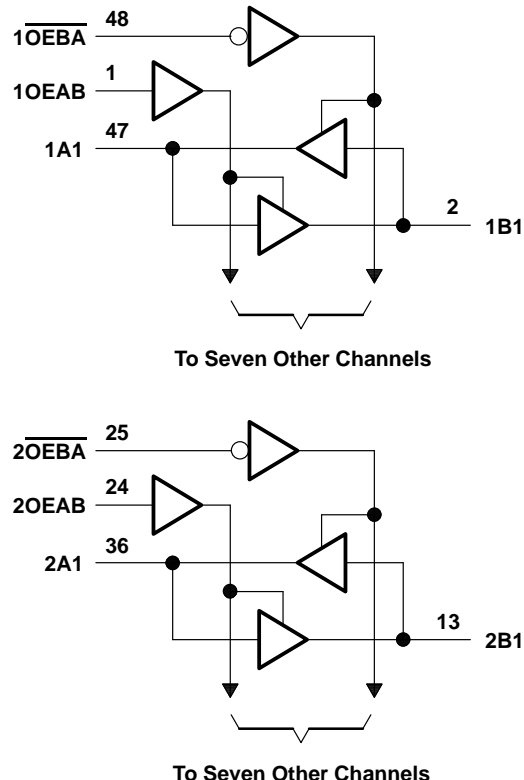
### WITH 3-STATE OUTPUTS

SCAS172 – D3680, JANUARY 1991 – REVISED APRIL 1993

#### logic symbol†



#### logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through $V_{CC}$ or GND	±400 mA
Maximum power package dissipation at $T_A = 55^\circ\text{C}$ (in still air)	0.85 W
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

**74AC16623**  
**16-BIT BUS TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

SCAS172 – D3680, JANUARY 1991 – REVISED APRIL 1993

**recommended operating conditions (see Note 2)**

			MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage		3	5	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 3\text{ V}$	2.1			V
		$V_{CC} = 4.5\text{ V}$	3.15			
		$V_{CC} = 5.5\text{ V}$	3.85			
$V_{IL}$	Low-level input voltage	$V_{CC} = 3\text{ V}$			0.9	V
		$V_{CC} = 4.5\text{ V}$			1.35	
		$V_{CC} = 5.5\text{ V}$			1.65	
$V_I$	Input voltage		0		$V_{CC}$	V
$V_O$	Output voltage		0		$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 3\text{ V}$			-4	mA
		$V_{CC} = 4.5\text{ V}$			-24	
		$V_{CC} = 5.5\text{ V}$			-24	
$I_{OL}$	Low-level output current	$V_{CC} = 3\text{ V}$			12	mA
		$V_{CC} = 4.5\text{ V}$			24	
		$V_{CC} = 5.5\text{ V}$			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
$T_A$	Operating free-air temperature		-40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	$V_{CC}$	TA = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
$V_{OH}$		$I_{OH} = -50\text{ }\mu\text{A}$	3 V	2.9			2.9		V
			4.5 V	4.4			4.4		
			5.5 V	5.4			5.4		
		$I_{OH} = -4\text{ mA}$	3 V	2.58			2.48		
			4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
$V_{OL}$		$I_{OL} = 50\text{ }\mu\text{A}$	3 V			0.1		0.1	V
			4.5 V			0.1		0.1	
			5.5 V			0.1		0.1	
		$I_{OL} = 12\text{ mA}$	3 V			0.36		0.44	
			4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
$I_L$	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			$\pm 0.1$		$\pm 1$	$\mu\text{A}$
$I_{OZ}^\ddagger$	A or B ports	$V_O = V_{CC}$ or GND	5.5 V			$\pm 0.5$		$\pm 5$	$\mu\text{A}$
$I_{CC}$		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		80	$\mu\text{A}$
$C_i$	Control inputs	$V_I = V_{CC}$ or GND	5 V		4.5				pF
$C_{io}$	A or B ports	$V_O = V_{CC}$ or GND	5 V		16				pF

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

<sup>‡</sup> For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.



# 74AC16623

## 16-BIT BUS TRANSCEIVER

### WITH 3-STATE OUTPUTS

SCAS172 – D3680, JANUARY 1991 – REVISED APRIL 1993

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$t_{PLH}$	A or B	B or A	2.7	8.1	10	2.7	11.2	ns
$t_{PHL}$			3.1	9.3	11.4	3.1	12.5	
$t_{PZH}$	$\overline{\text{OEBA}}$	A	2.7	8.3	10.3	2.7	11.5	ns
$t_{PZL}$			3.5	11.8	14.2	3.5	15.6	
$t_{PHZ}$	$\overline{\text{OEBA}}$	A	4.8	7.7	9.3	4.8	9.9	ns
$t_{PLZ}$			4.1	7.5	9.2	4.1	9.8	
$t_{PZH}$	OEAB	B	2.8	8.1	9.9	2.8	11.1	ns
$t_{PZL}$			3.8	10.7	14.1	3.8	15.1	
$t_{PHZ}$	OEAB	B	4.7	7.5	9.1	4.7	9.5	ns
$t_{PLZ}$			4.3	7.3	8.9	4.3	9.3	

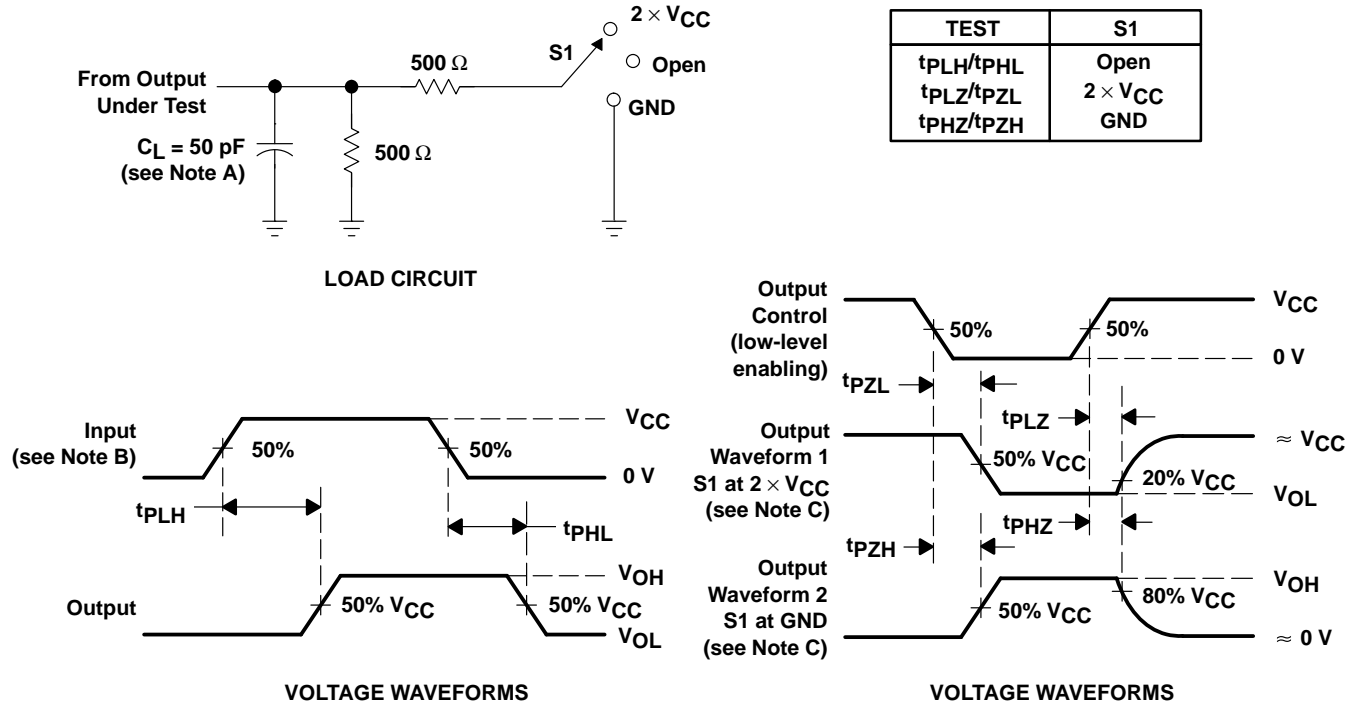
switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$t_{PLH}$	A or B	B or A	2.3	5.1	6.9	2.3	7.7	ns
$t_{PHL}$			2.6	6	7.8	2.6	8.6	
$t_{PZH}$	$\overline{\text{OEBA}}$	A	2.1	5.3	6.8	2.1	7.6	ns
$t_{PZL}$			2.8	6.9	8.5	2.8	9.4	
$t_{PHZ}$	$\overline{\text{OEBA}}$	A	4.7	6.9	8.4	4.7	8.9	ns
$t_{PLZ}$			4	6.3	7.7	4	8.2	
$t_{PZH}$	OEAB	B	2.3	5.2	6.7	2.3	7.5	ns
$t_{PZL}$			3	6.7	8.4	3	9.3	
$t_{PHZ}$	OEAB	B	4.5	6.9	8.4	4.5	8.9	ns
$t_{PLZ}$			4	6.2	7.6	4	7.9	

operating characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance per transceiver	Outputs enabled	47	pF
		Outputs disabled	8	

## PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



## **IMPORTANT NOTICE**

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

**TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.**

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.