

- Free-Running Read and Write Clocks Can Be Asynchronous or Coincident
- Read and Write Operations Synchronized to Independent System Clocks
- Input-Ready Flag Synchronized to Write Clock
- Output-Ready Flag Synchronized to Read Clock
- 2048 Words by 9 Bits
- Low-Power Advanced CMOS Technology
- Programmable Almost-Full/Almost-Empty Flag
- Input-Ready, Output-Ready, and Half-Full Flags
- Cascadable in Word Width and/or Word Depth
- Fast Access Times of 12 ns With a 50-pF Load
- Data Rates From 0 to 67 MHz
- 3-State Outputs
- Available in 44-Pin PLCC (FN), Space-Saving 64-Pin Thin Quad Flat (PM), and Reduced-Height 64-Pin Thin Quad Flat (PAG) Packages

## description

The SN74ACT7807 is a 2048-word by 9-bit FIFO with high speed and fast access times. It processes data at rates up to 67 MHz and access times of 12 ns in a bit-parallel format. Data outputs are noninverting with respect to the data inputs. Expansion is easily accomplished in both word width and word depth.

The write-clock (WRTCLK) and read-clock (RDCLK) inputs should be free running and can be asynchronous or coincident. Data is written to memory on the rising edge of WRTCLK when the write-enable (WRTEN1/DP9, WRTEN2) inputs are high and the input-ready (IR) flag output is high. Data is read from memory on the rising edge of RDCLK when the read-enable (RDEN1, RDEN2) and output-enable (OE) inputs are high and the output-ready (OR) flag output is high. The first word written to memory is clocked through to the output buffer regardless of the levels on RDEN1, RDEN2, and OE. The OR flag indicates that valid data is present on the output buffer.

The FIFO can be reset asynchronous to WRTCLK and RDCLK.  $\overline{\text{RESET}}$  must be asserted while at least four WRTCLK and four RDCLK cycles occur to clear the synchronizing registers. Resetting the FIFO initializes the IR, OR, and HF flags low and the AF/AE flag high. The FIFO must be reset upon power up.

The SN74ACT7807 is characterized for operation from 0°C to 70°C.



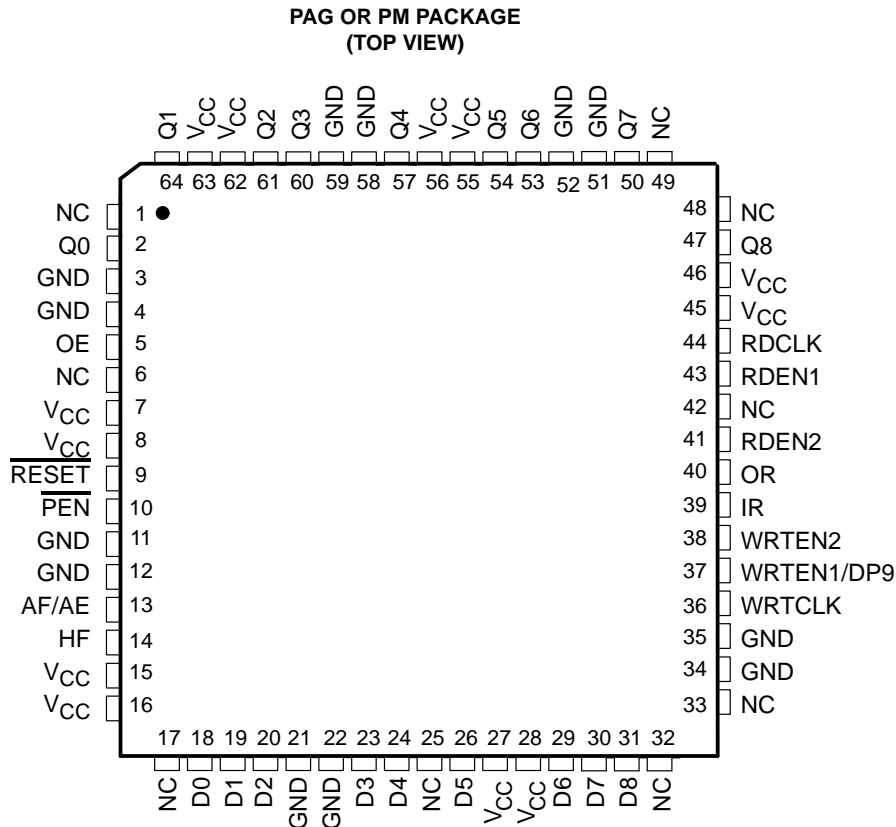
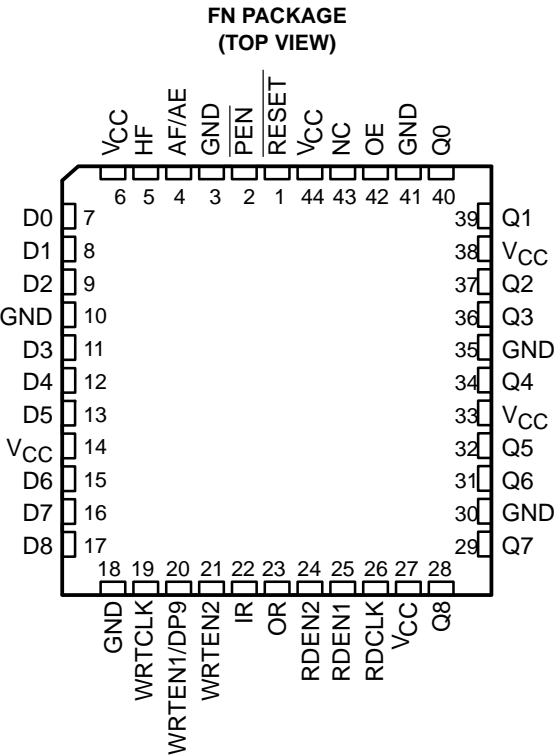
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

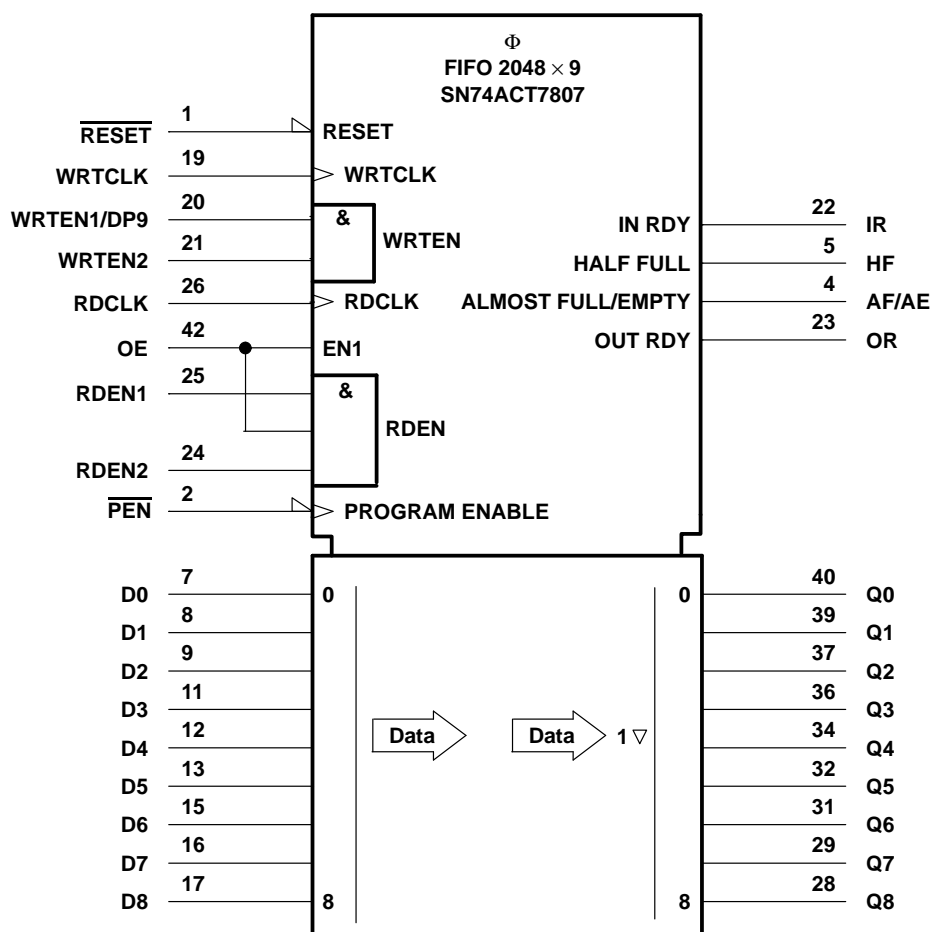
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1995, Texas Instruments Incorporated



NC – No internal connection

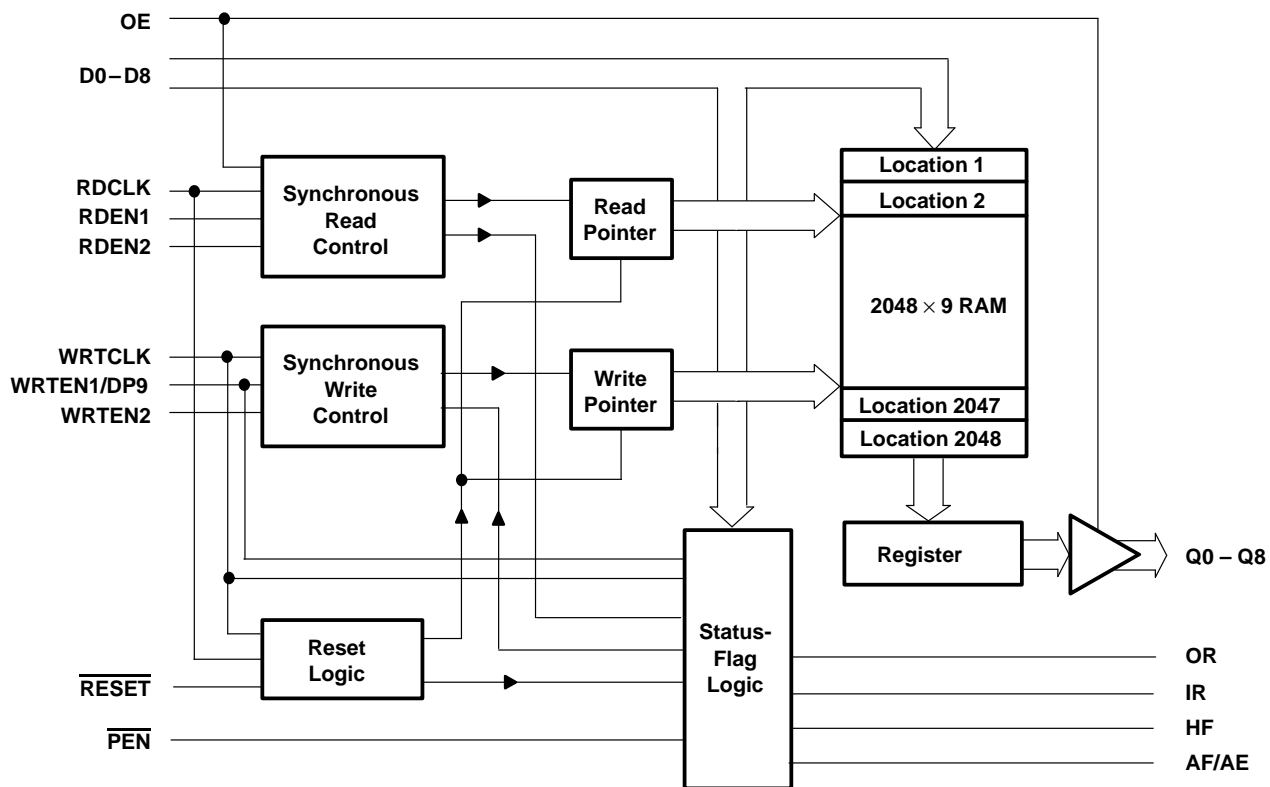
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the FN package.

**SN74ACT7807**  
**2048 × 9**  
**CLOCKED FIRST-IN, FIRST-OUT MEMORY**  
 SCAS200B – JANUARY 1991 – REVISED JULY 1995

**functional block diagram**



## CLOCKED FIRST-IN, FIRST-OUT MEMORY

SCAS200B – JANUARY 1991 – REVISED JULY 1995

## Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
AF/AE	O	Almost-full/almost-empty flag. Depth offset values can be programmed for AF/AE or the default value of 256 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or less words or (2048 – Y) or more words. AF/AE is high after reset.
D0–D8	I	Nine-bit data input port
HF	O	Half-full flag. HF is high when the FIFO memory contains 1024 or more words. HF is low after reset.
IR	O	Input-ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is low during reset and goes high on the second low-to-high transition of WRTCLK after reset.
OE	I	Output enable. When OE, RDEN1, RDEN2 and OR are high, data is read from the FIFO on a low-to-high transition of RDCLK. When OE is low, reads are disabled and the data outputs are in the high-impedance state.
OR	O	Output-ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on Q0–Q8 when OR is high. OR is low during reset and goes high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory.
$\overline{\text{PEN}}$	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D8 and DP9 is latched as an AF/AE offset value when $\overline{\text{PEN}}$ is low and WRTCLK is high.
Q0–Q8	O	Nine-bit data output port. After the first valid write to empty memory, the first word is output on Q0–Q8 on the third rising edge of RDCLK. OR is also asserted high at this time to indicate ready data. When OR is low, the last word read from the FIFO is present on Q0–Q8.
RDCLK	I	Read clock. RDCLK is a continuous clock and can be asynchronous or coincident to WRTCLK. A low-to-high transition of RDCLK reads data from memory when RDEN1, RDEN2, OE, and OR are high. OR is synchronous to the low-to-high transition of RDCLK.
RDEN1, RDEN2	I	Read enables. When RDEN1, RDEN2, OE, and OR are high, data is read from the FIFO on the low-to-high transition of RDCLK.
$\overline{\text{RESET}}$	I	Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while $\overline{\text{RESET}}$ is low. This sets HF, IR, and OR low and AF/AE high.
WRTCLK	I	Write clock. WRTCLK is a continuous clock and can be asynchronous or coincident to RDCLK. A low-to-high transition of WRTCLK writes data to memory when WRTEN1/DP9, WRTEN2, and IR are high. IR is synchronous to the low-to-high transition of WRTCLK.
WRTEN1/DP9	I	Write enable/data pin 9. When WRTEN1/DP9, WRTEN2, and IR are high, data is written to the FIFO on a low-to-high transition of WRTCLK. When programming an AF/AE offset value, WRTEN1/DP9 is used as the most significant data bit.
WRTEN2	I	Write enable. When WRTEN1/DP9, WRTEN2, and IR are high, data is written to the FIFO on a low-to-high transition of WRTCLK.

## offset values for AF/AE

The almost-full/almost-empty flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. If the offsets are not programmed, the default values of  $X = Y = 256$  are used. The AF/AE flag is high when the FIFO contains X or less words or  $(2048 - Y)$  or more words.

Program enable ( $\overline{PEN}$ ) should be held high throughout the reset cycle.  $\overline{PEN}$  can be brought low only when IR is high and WRTCLK is low. On the following low-to-high transition of WRTCLK, the binary value on D0–D8 and WRTEN1/DP9 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding  $\overline{PEN}$  low for another low-to-high transition of WRTCLK reprograms Y to the binary value on D0–D8 and WRTEN1/DP9 at the time of the second WRTCLK low-to-high transition. While the offsets are programmed, data is not written to the FIFO memory regardless of the state of the write enables (WRTEN1/DP9, WRTEN2). A maximum value of 1023 can be programmed for either X or Y (see Figure 1). To use the default values of  $X = Y = 256$ ,  $\overline{PEN}$  must be held high.

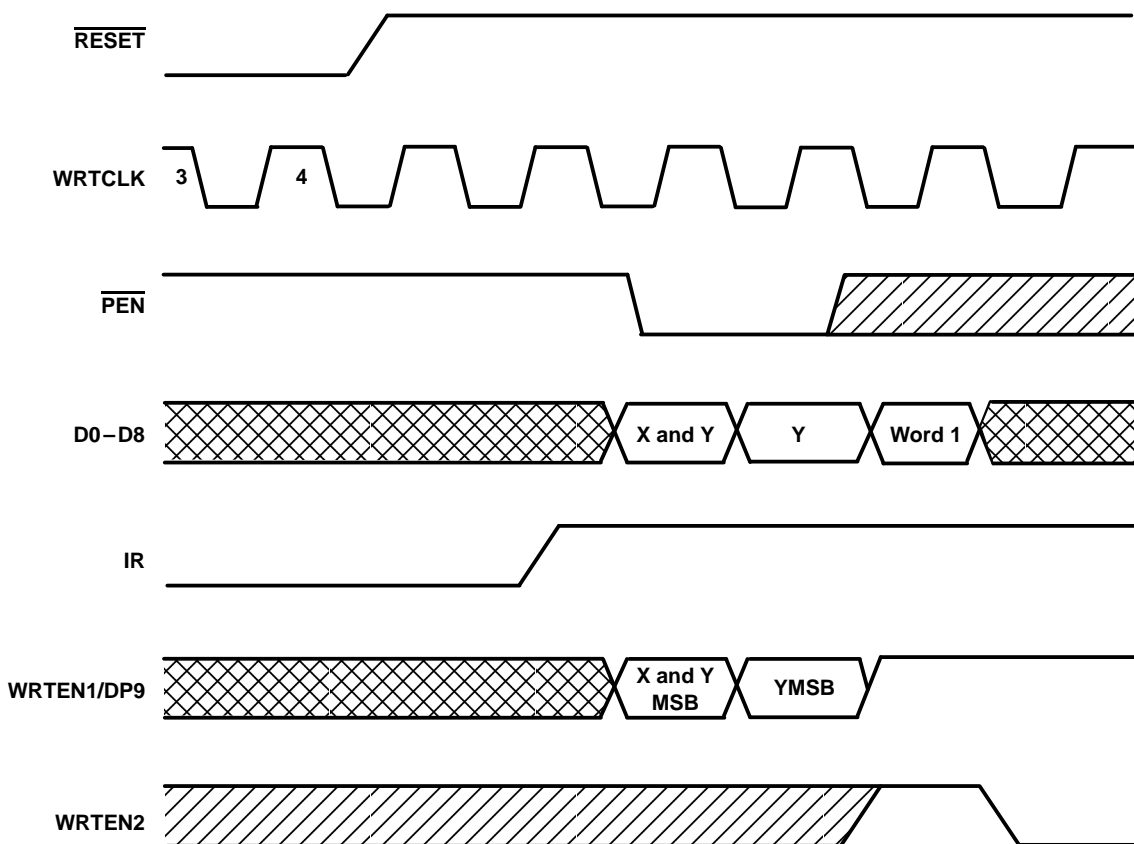
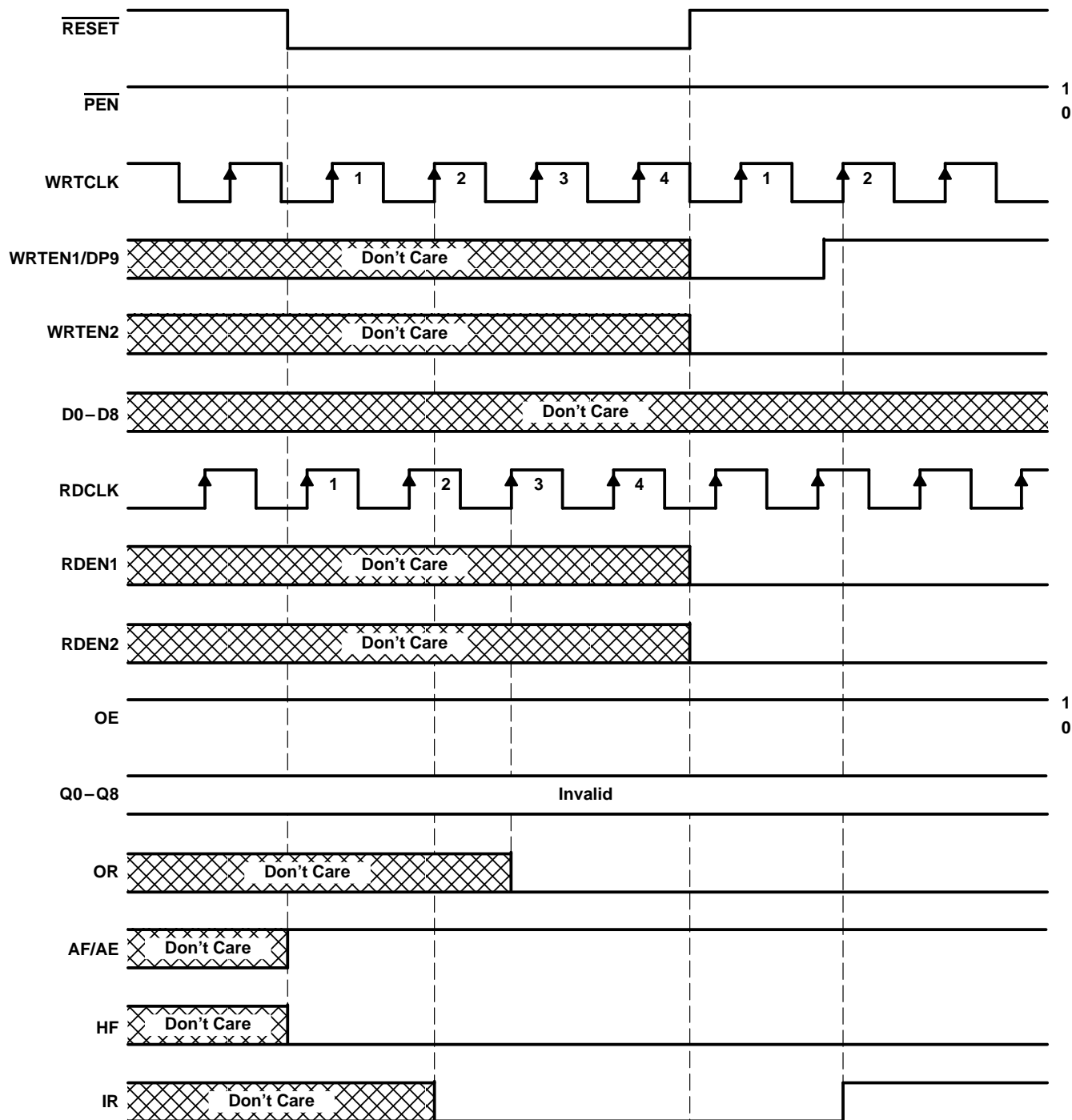


Figure 1. Programming X and Y Separately

## CLOCKED FIRST-IN, FIRST-OUT MEMORY

SCAS200B – JANUARY 1991 – REVISED JULY 1995



Define the AF/AE Flag Using the  
Default Value of  $X = Y = 256$

Figure 2. Reset Cycle

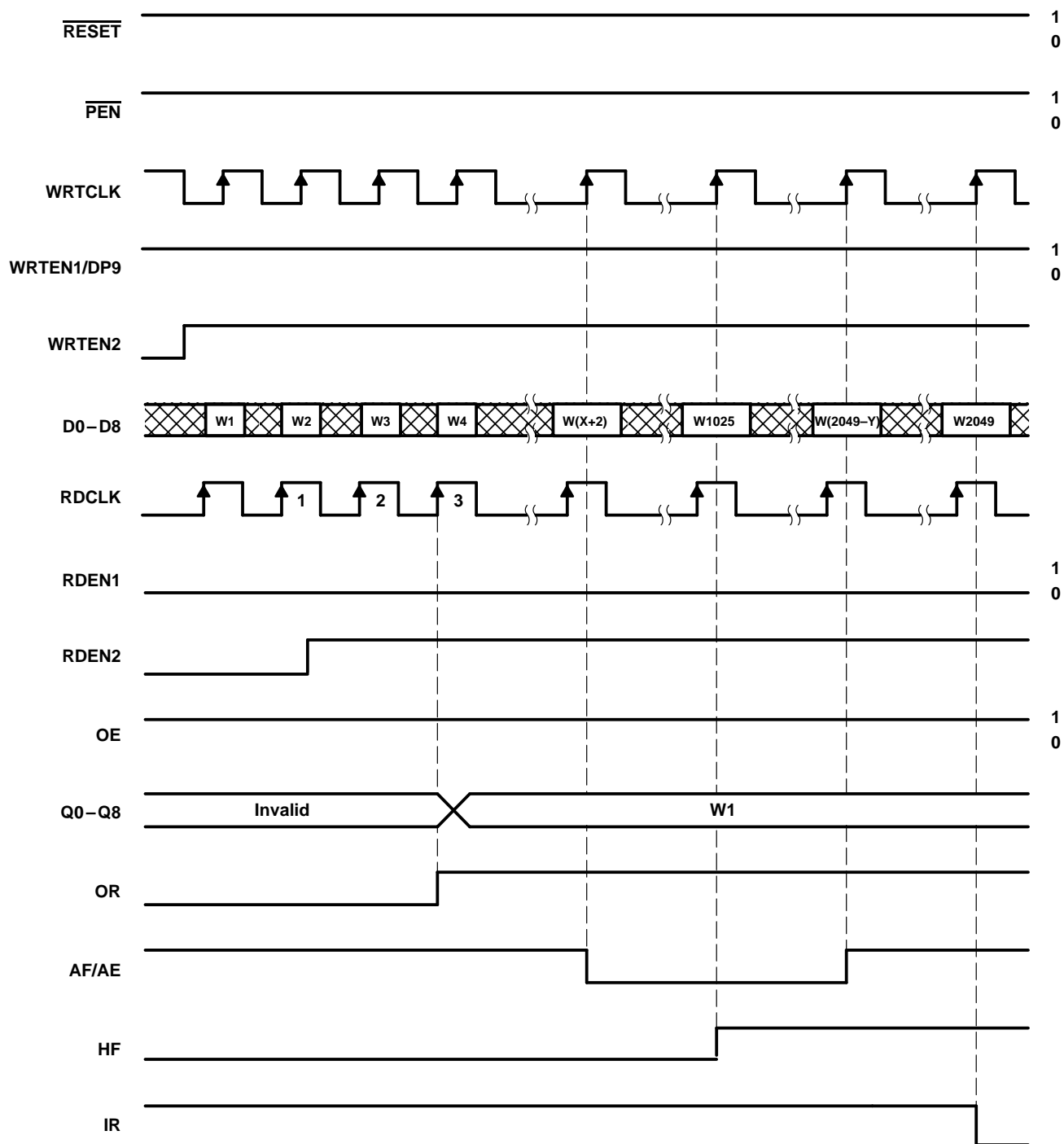


Figure 3. Write Cycle



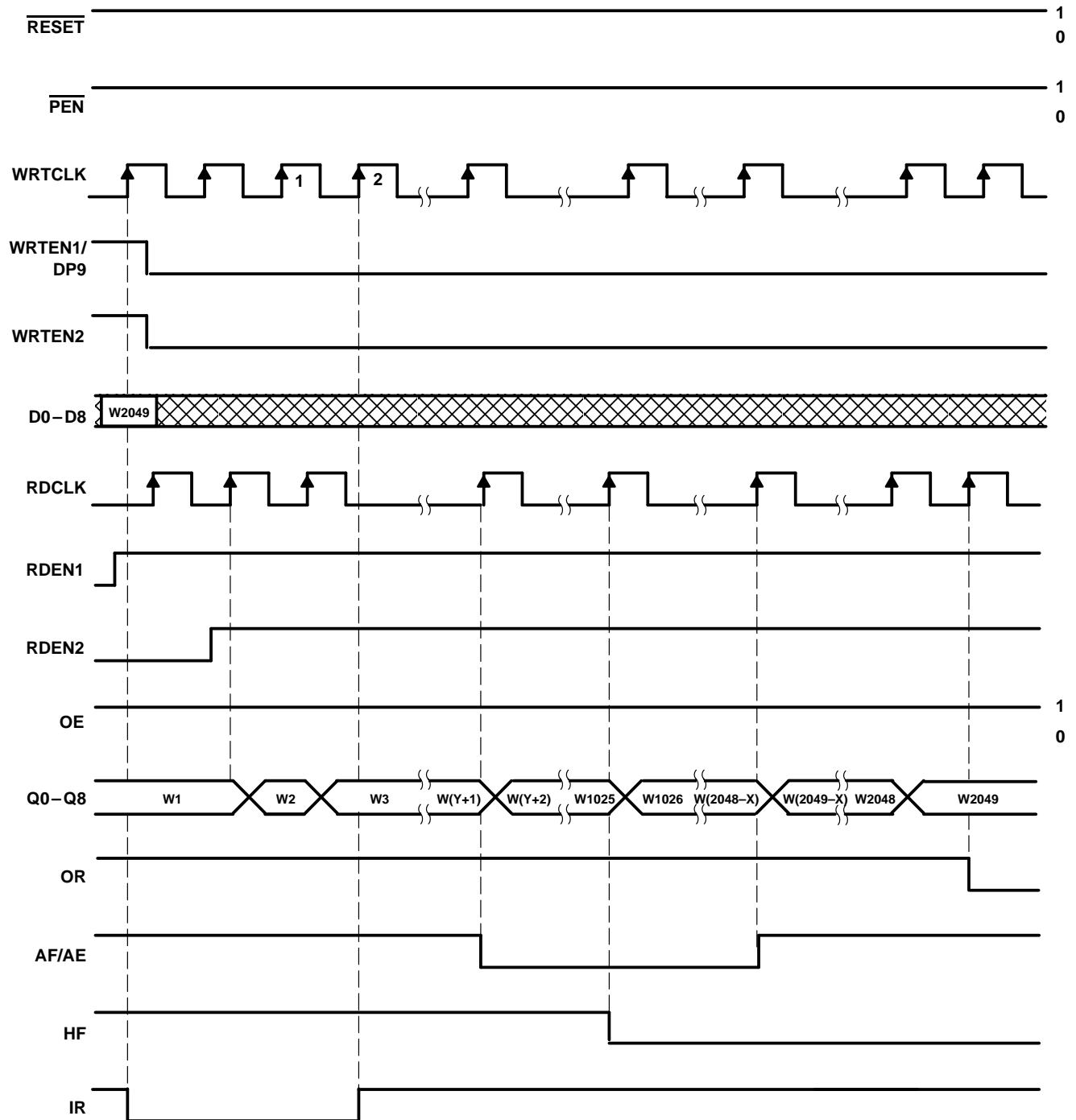


Figure 4. Read Cycle

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage, $V_I$	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

			'ACT7807-15		'ACT7807-20		'ACT7807-25		'ACT7807-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8		0.8		0.8	V
I <sub>OH</sub>	High-level output current	Q outputs, flags	−8		−8		−8		−8		mA
I <sub>OL</sub>	Low-level output current	Q outputs	16		16		16		16		mA
		Flags	8		8		8		8		
f <sub>clock</sub>	Clock frequency		67		50		40		25		MHz
t <sub>w</sub>	Pulse duration	WRTCLK high or low	6		8		9		13		ns
		RDCLK high or low	6		8		9		13		
		PEN low	6		9		9		13		
t <sub>su</sub>	Setup time	D0–D8 before WRTCLK↑	4		5		5		5		ns
		WRTEN1, WRTEN2 before WRTCLK↑	4		5		5		5		
		OE, RDEN1, RDEN2 before RDCLK↑	5		6		6		6.5		
		Reset: RESET low before first WRTCLK↑ and RDCLK↑‡	7		8		8		8		
		PEN before WRTCLK↑	4		5		5		5		
t <sub>h</sub>	Hold time	D0–D8 after WRTCLK↑	0		0		0		0		ns
		WRTEN1, WRTEN2 after WRTCLK↑	0		0		0		0		
		OE, RDEN1, RDEN2 after RDCLK↑	0		0		0		0		
		Reset: RESET low after fourth WRTCLK↑ and RDCLK↑‡	5		5		5		5		
		PEN high after WRTCLK↓	0		0		0		0		
		PEN low after WRTCLK↑	3		3		3		3		
T <sub>A</sub>	Operating free-air temperature		0	70	0	70	0	70	0	70	°C

<sup>‡</sup> To permit the clock pulse to be utilized for reset purposes

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{OH}$		$V_{CC} = 4.5\text{ V}$ ,	$I_{OH} = -8\text{ mA}$	2.4			V
$V_{OL}$	Flags	$V_{CC} = 4.5\text{ V}$ ,	$I_{OL} = 8\text{ mA}$			0.5	V
	Q outputs	$V_{CC} = 4.5\text{ V}$ ,	$I_{OL} = 16\text{ mA}$			0.5	
$I_I$		$V_{CC} = 5.5\text{ V}$ ,	$V_I = V_{CC}$ or 0			±5	μA
$I_{OZ}$		$V_{CC} = 5.5\text{ V}$ ,	$V_O = V_{CC}$ or 0			±5	μA
$I_{CC}$		$V_{CC} = 5.5\text{ V}$ ,	$V_I = V_{CC} - 0.2\text{ V}$ or 0			400	μA
$\Delta I_{CC}^\ddagger$	WRTEN1/DP9	$V_{CC} = 5.5\text{ V}$ ,	One input at 3.4 V, Other inputs at $V_{CC}$ or GND			2	mA
	Other inputs					1	
$C_i$		$V_I = 0$ ,	$f = 1\text{ MHz}$			4	pF
$C_o$		$V_O = 0$ ,	$f = 1\text{ MHz}$			8	pF

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ This is the supply current for each input that is at one of the specified TTL voltage levels rather 0 V or  $V_{CC}$ .

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figures 9 and 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7807-15			'ACT7807-20		'ACT7807-25		'ACT7807-40		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$	WRTCLK or RDCLK		67			50		40		25		MHz
$t_{pd}$	RDCLK↑	Any Q	3	9	12	3	13	3	18	3	25	ns
$t_{pd}^\S$				8								
$t_{pd}$	WRTCLK↑	IR	1		9	1	12	1	14	1	16	ns
$t_{pd}$	RDCLK↑	OR	1		9	2	12	2	14	2	16	ns
$t_{pd}$	WRTCLK↑	AF/AE	2		16	2	20	2	25	2	30	ns
	RDCLK↑		2		17	2	20	2	25	2	30	
$t_{PLH}$	WRTCLK↑	HF	2		19	2	21	2	23	2	25	ns
$t_{PHL}$	RDCLK↑		2		16	2	18	2	20	2	22	
$t_{PLH}$	$\overline{\text{RESET}}$ low	AF/AE	1		12	1	18	1	22	1	24	ns
$t_{PHL}$		HF	2		12	2	18	2	22	2	24	
$t_{en}$	OE	Any Q	2		10	2	13	2	15	2	18	ns
$t_{dis}$			1		11	1	13	1	15	1	18	

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§ This parameter is measured with  $C_L = 30\text{ pF}$  (see Figure 5).

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance per FIFO channel	Outputs enabled	$C_L = 50\text{ pF}$ , $f = 5\text{ MHz}$	91	pF

TYPICAL CHARACTERISTICS

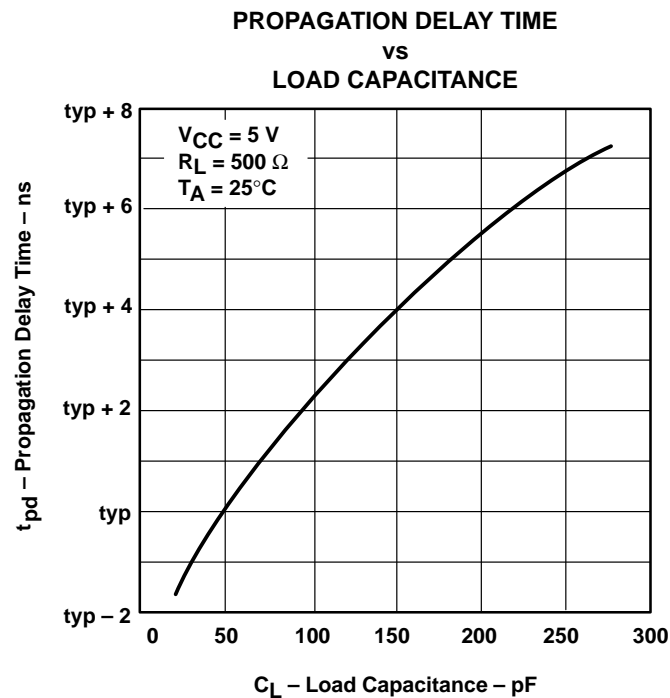


Figure 5

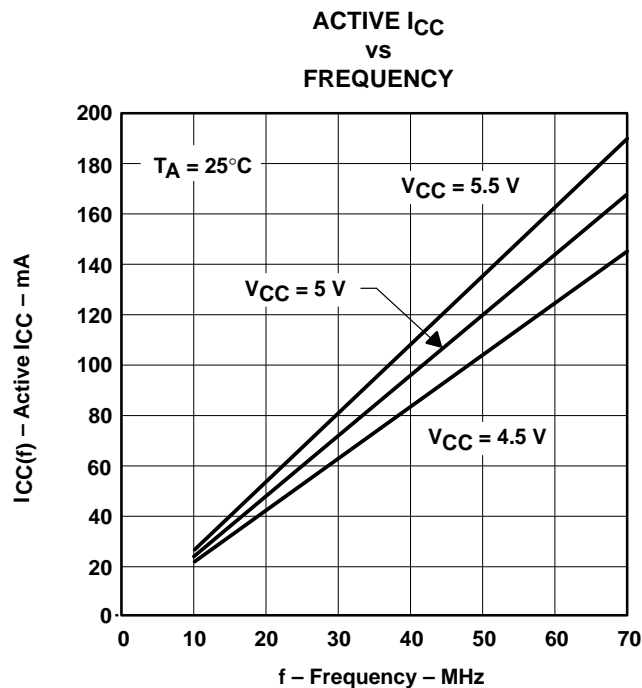


Figure 6

## TYPICAL CHARACTERISTICS

## calculating power dissipation

With  $I_{CC(f)}$  taken from Figure 6, the maximum power dissipation ( $P_T$ ) of the SN74ACT7807 can be calculated by:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_L \times V_{CC}^2 \times f_o)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found by:

$$P_T = V_{CC} \times [I_{CC(I)} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma (C_L \times V_{CC}^2 \times f_o)$$

where:

$I_{CC(I)}$  = idle  $I_{CC}$  maximum (see Figure 7)

$N$  = number of inputs driven by a TTL device

$\Delta I_{CC}$  = increase in supply current

$dc$  = duty cycle of inputs at a TTL high level of 3.4 V

$C_{pd}$  = power dissipation capacitance

$C_L$  = output capacitive load

$f_i$  = data input frequency

$f_o$  = data output frequency

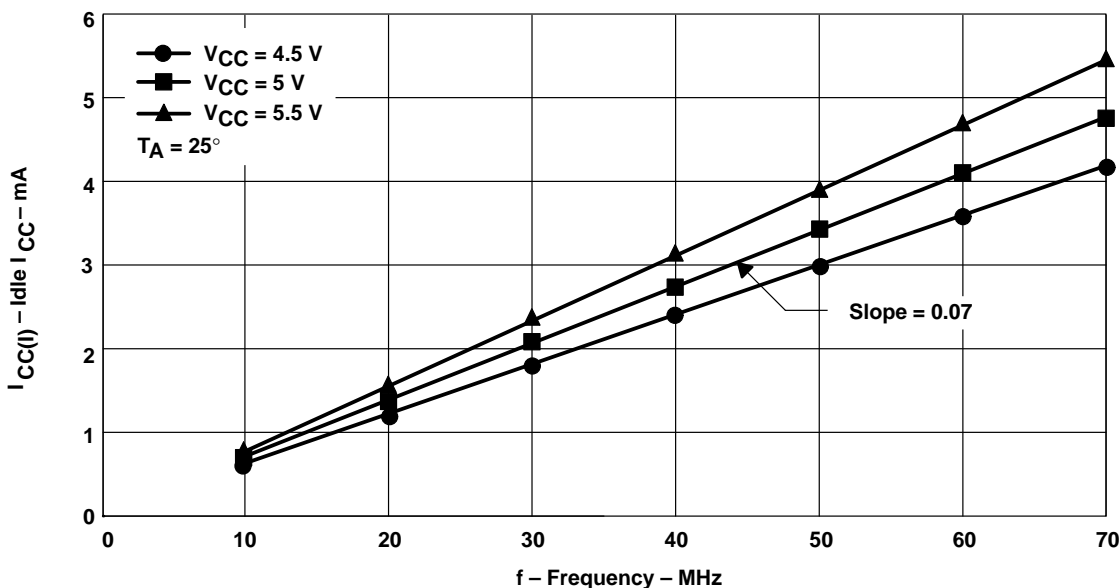


Figure 7. SN74ACT7807 Idle  $I_{CC}$  With WRTCLK Switching, Other Inputs at 0 or  $V_{CC} - 0.2$  V and Outputs Disconnected

## APPLICATION INFORMATION

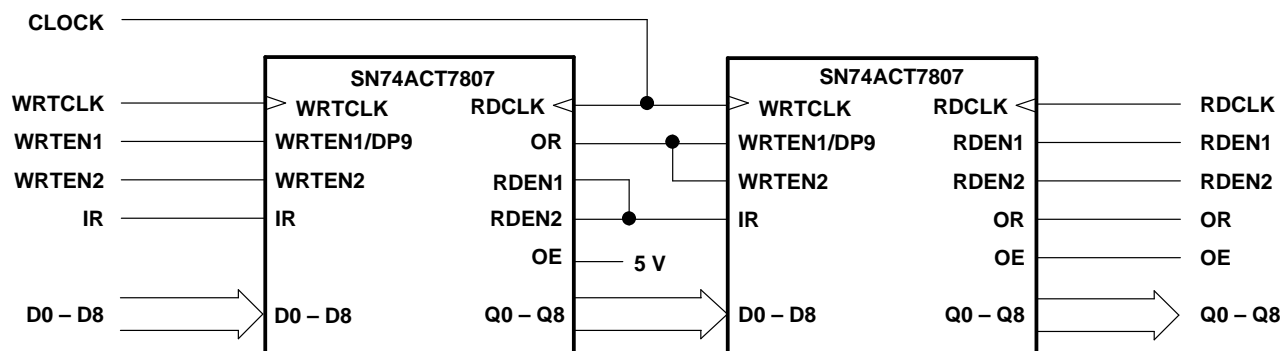


Figure 8. Word-Depth Expansion: 4096 Words by 9 Bits

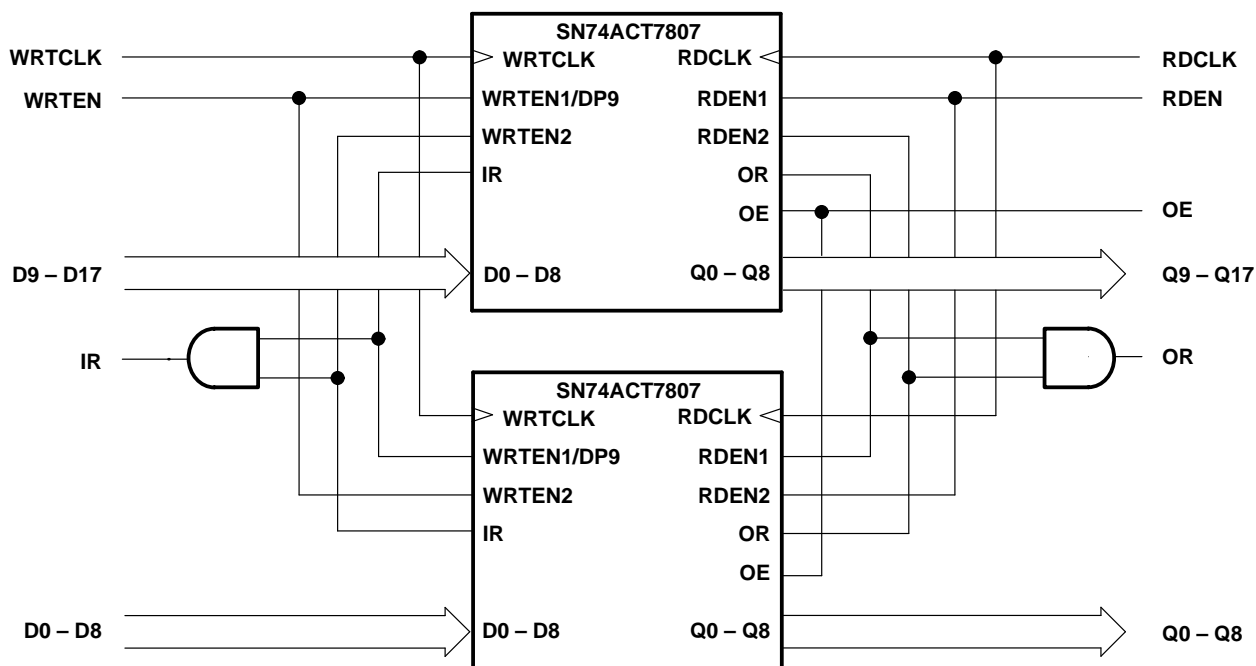


Figure 9. Word-Width Expansion: 2048 Words by 18 Bits

## PARAMETER MEASUREMENT INFORMATION

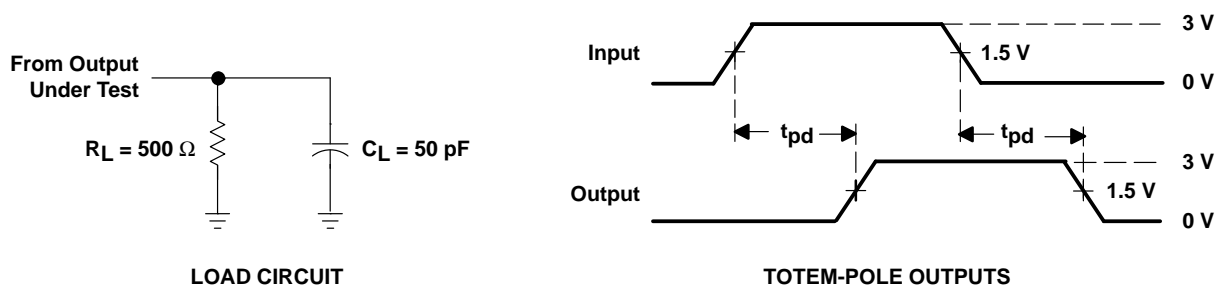
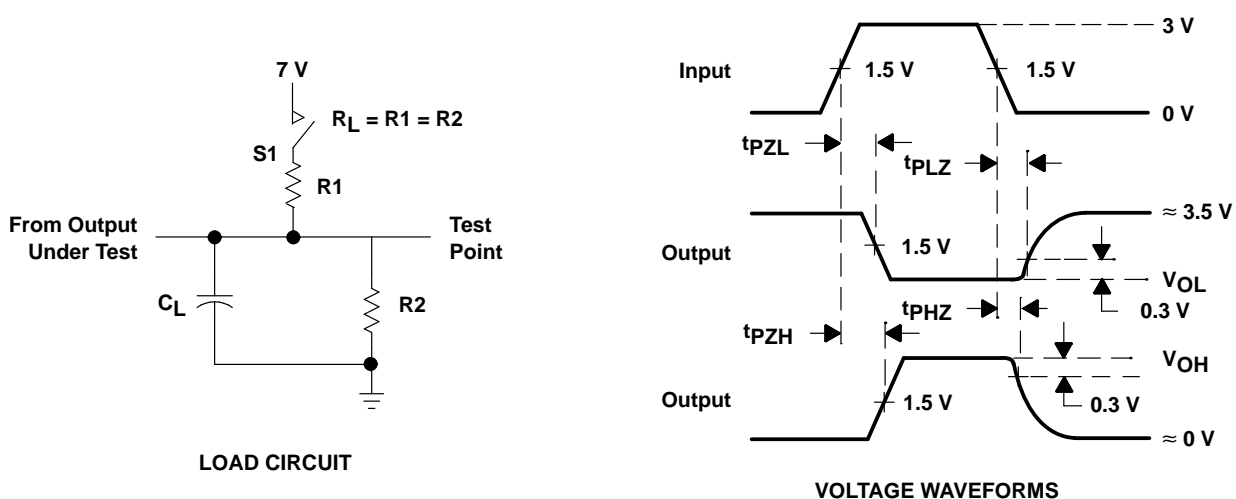


Figure 10. Standard CMOS Outputs (IR, OR, HF, AF/AE)



PARAMETER		R1, R2	$C_L^\dagger$	S1
$t_{en}$	$t_{PZH}$	500 $\Omega$	50 pF	Open
	$t_{PZL}$			Closed
$t_{dis}$	$t_{PHZ}$	500 $\Omega$	50 pF	Open
	$t_{PLZ}$			Closed
$t_{pd}$		500 $\Omega$	50 pF	Open

<sup>†</sup> Includes probe and test fixture capacitance

Figure 11. 3-State Outputs (Any Q)

## **IMPORTANT NOTICE**

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

**TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.**

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.