

# SN74ALS232B

## 16 × 4 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

SCAS251 – FEBRUARY 1989 – REVISED SEPTEMBER 1993

- Independent Asynchronous Inputs and Outputs
- 16 Words by 4 Bits
- Data Rates From 0 to 40 MHz
- Fall-Through Time . . . 14 ns Typ
- 3-State Outputs
- Package Options Include Plastic Small-Outline Packages (DW), Plastic Chip Carriers (FN), and Standard Plastic 300-mil DIPs (N)

### description

This 64-bit memory use advanced low-power Schottky technology and features high speed and fast fall-through times. It is organized as 16 words by 4 bits each.

A first-in, first-out (FIFO) memory is a storage device that allows data to be written into and read from its array at independent data rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

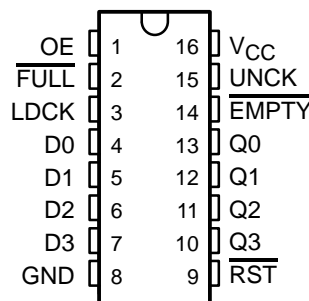
Data is written into memory on a low-to-high transition at the load-clock (LDCK) input and is read out on a low-to-high transition at the unload-clock (UNCK) input. The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the  $\overline{\text{FULL}}$  and  $\overline{\text{EMPTY}}$  output flags. The  $\overline{\text{FULL}}$  output is low when the memory is full and high when it is not full. The  $\overline{\text{EMPTY}}$  output is low when the memory is empty and high when it is not empty.

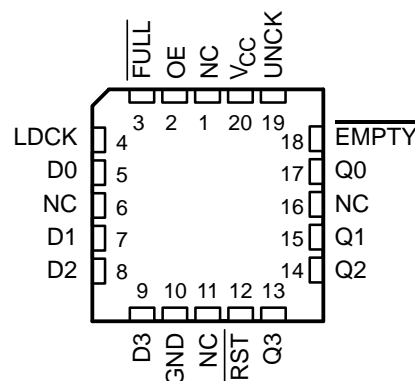
A low level on the reset ( $\overline{\text{RST}}$ ) input resets the internal stack-control pointers and also sets  $\overline{\text{EMPTY}}$  low and sets  $\overline{\text{FULL}}$  high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK, after either a  $\overline{\text{RST}}$  pulse or from an empty condition, causes  $\overline{\text{EMPTY}}$  to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable (OE) input is low. OE does not affect the  $\overline{\text{FULL}}$  or  $\overline{\text{EMPTY}}$  output flags. Cascading is easily accomplished in the word-width direction but is not possible in the word-depth direction.

The SN74ALS232B is characterized for operation from 0°C to 70°C.

DW OR N PACKAGE  
(TOP VIEW)



FN PACKAGE  
(TOP VIEW)



NC – No internal connection



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**TEXAS  
INSTRUMENTS**

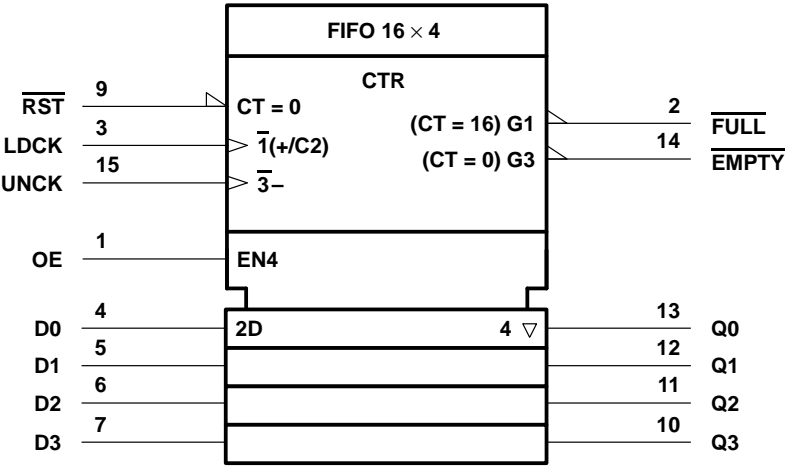
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logic symbol†



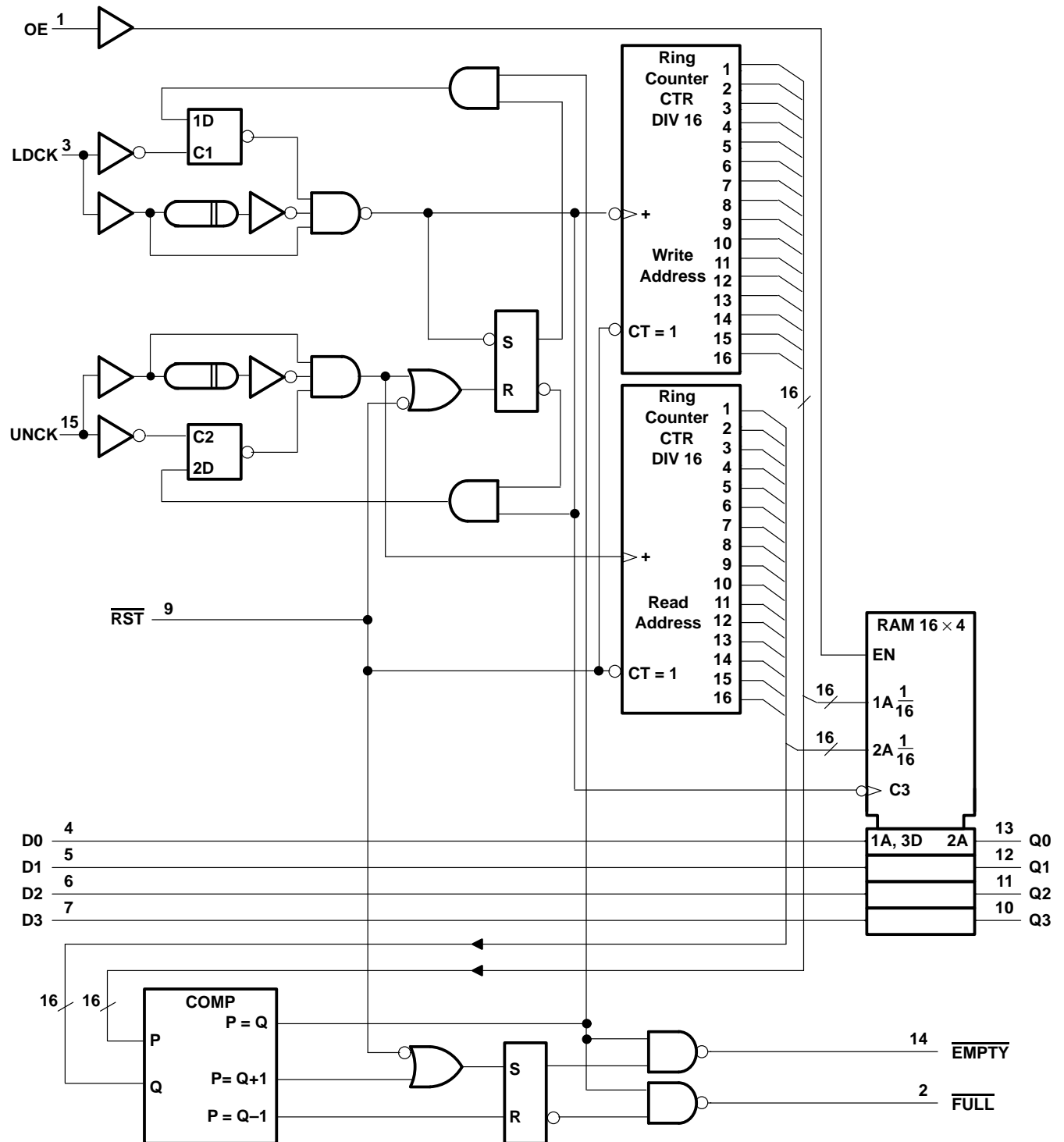
† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0. Pin numbers shown are for the DW and N packages.

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### logic diagram (positive logic)

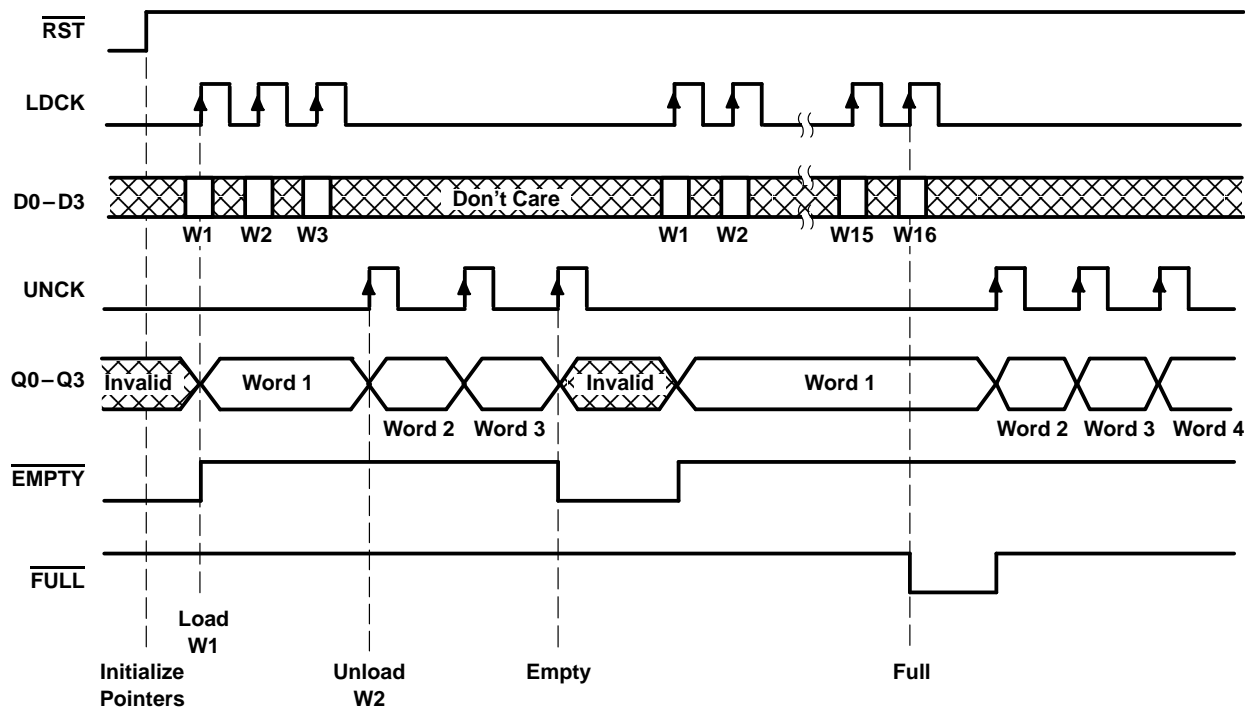


Pin numbers shown are for the DW and N packages.

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timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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### recommended operating conditions (see Note 1)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	2			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>OH</sub>	High-level output current	Q outputs		–2.6	mA
		FULL, EMPTY		–0.4	
I <sub>OL</sub>	Low-level output current	Q outputs		24	mA
		FULL, EMPTY		8	
f <sub>clock</sub> †	Clock frequency	LDCK	0	40	MHz
		UNCK	0	40	
t <sub>w</sub>	Pulse duration	RST low	18		ns
		LDCK low	15		
		LDCK high	10		
		UNCK low	15		
		UNCK high	10		
t <sub>su</sub>	Setup time	Data before LDCK↑	8		ns
		LDCK inactive before RST↑	5		
t <sub>h</sub>	Hold time	Data after LDCK↑	5		ns
		LDCK inactive after RST↑	5		
T <sub>A</sub>	Operating free-air temperature	0		70	°C

† The maximum possible clock frequency is 40 MHz. The maximum clock frequency when using a 50% duty cycle is 33.3 MHz.

NOTE 1: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates limits for maximum V<sub>IL</sub>, minimum V<sub>IH</sub>, or minimum pulse duration can cause a false clock or improper operation of the internal read and write pointers.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = –18 mA			–1.2	V
V <sub>OH</sub>	Q outputs	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = –2.6 mA	2.4	3.2	V
	FULL, EMPTY	V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = –0.4 mA	V <sub>CC</sub> – 2		
V <sub>OL</sub>	Q outputs	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 12 mA	0.25	V
			I <sub>OL</sub> = 24 mA	0.35	
	FULL, EMPTY	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 4 mA	0.25	
			I <sub>OL</sub> = 8 mA	0.35	
I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V			20	μA
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.4 V			–20	μA
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V			0.1	mA
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V			20	μA
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V			–0.2	mA
I <sub>O§</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V	–30		–112	mA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V		80	125	mA

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>.



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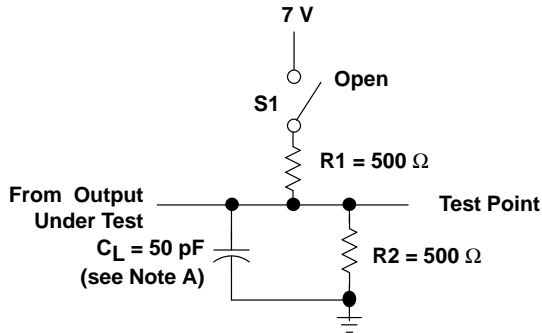
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### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, C <sub>L</sub> = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T <sub>A</sub> = 25°C			V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T <sub>A</sub> = MIN to MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
f <sub>max</sub>	LDCK, UNCK			50		40		MHz
t <sub>pd</sub>	LDCK↑	Any Q		14	23	6	30	ns
	UNCK↑			15	23	6	30	
t <sub>PLH</sub>	LDCK↑	<u>EMPTY</u>		13	20	5	25	ns
t <sub>PHL</sub>	UNCK↑			15	22	6	27	
t <sub>PHL</sub>	<u>RST</u> ↓	<u>EMPTY</u>		15	21	5	26	ns
t <sub>PHL</sub>	LDCK↑	<u>FULL</u>		15	22	6	27	ns
t <sub>PLH</sub>	UNCK↑	<u>FULL</u>		13	20	5	25	ns
	<u>RST</u> ↓			16	23	7	28	
t <sub>en</sub>	OE↑	Q		5	12	1	14	ns
t <sub>dis</sub>	OE↓	Q		5	12	1	16	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

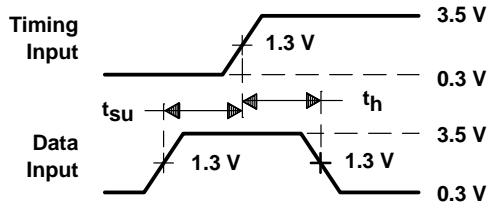
## PARAMETER MEASUREMENT INFORMATION



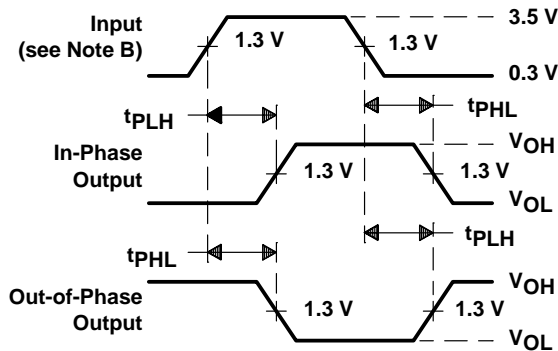
**LOAD CIRCUIT FOR 3-STATE OUTPUTS**

**SWITCH POSITION TABLE**

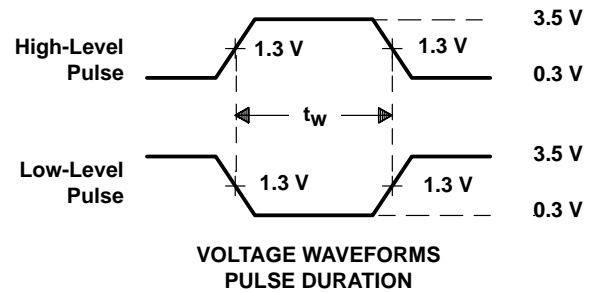
TEST	S1
$t_{PLH}$	Open
$t_{PHL}$	Open
$t_{PZH}$	Open
$t_{PZL}$	Closed
$t_{PHZ}$	Open
$t_{PLZ}$	Closed



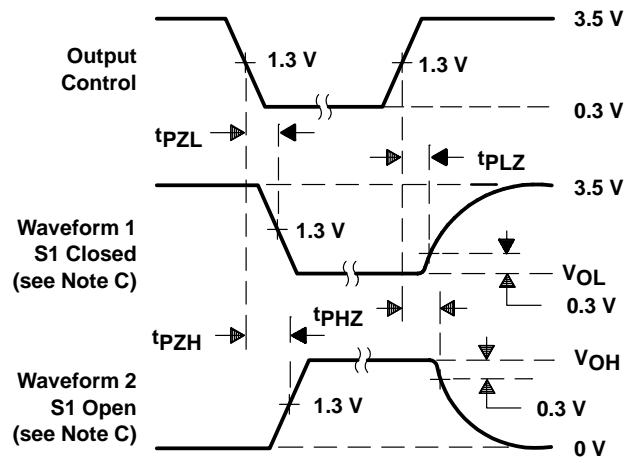
**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS  
PULSE DURATION**



**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**





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