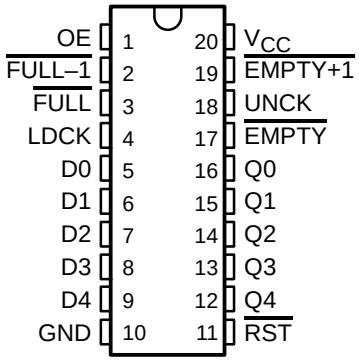
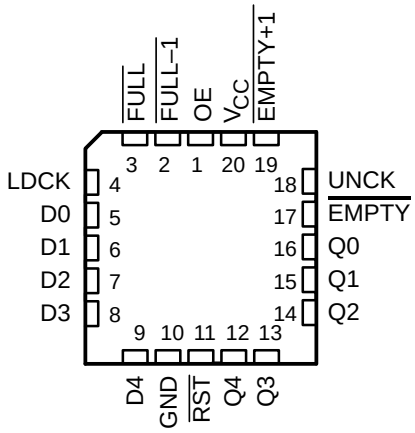
SCAS253 – MARCH 1990 – REVISED JUNE 1992

- **Independent Asychronous Inputs and Outputs**
- **16 Words by 5 Bits**
- **Data Rates From 0 to 40 MHz**
- **Fall-Through Time . . . 14 ns Typ**
- **3-State Outputs**
- **Package Options Include Plastic Small-Outline Packages (DW), Plastic Chip Carriers (FN), and Standard Plastic 300-mil DIPs (N)**

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

This 80-bit memory uses advanced low-power Schottky technology and features high speed and a fast fall-through time. It is organized as 16 words by 5 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

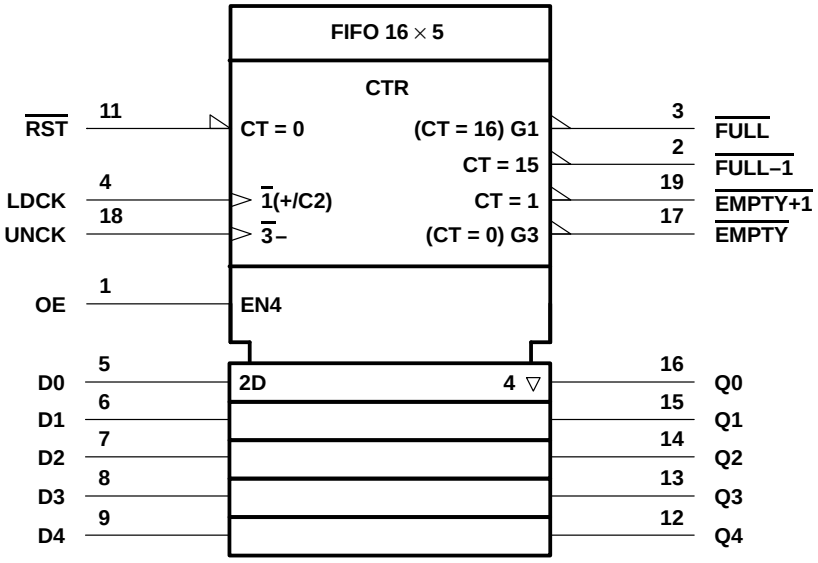
Data is written into memory on a low-to-high transition at the load clock (LDCK) input and is read out on a low-to-high transition at the unload clock (UNCK) input. The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$, $\overline{\text{FULL–1}}$, and $\overline{\text{EMPTY+1}}$ output flags. The $\overline{\text{FULL}}$ output is low when the memory is full and high when it is not full. The $\overline{\text{FULL–1}}$ output is low when the memory contains 15 data words. The $\overline{\text{EMPTY}}$ output is low when the memory is empty and high when it is not empty. The $\overline{\text{EMPTY+1}}$ output is low when one word remains in memory.

A low level on the reset ($\overline{\text{RST}}$) input resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and sets $\overline{\text{FULL}}$, $\overline{\text{FULL–1}}$, and $\overline{\text{EMPTY+1}}$ high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK, after either a $\overline{\text{RST}}$ pulse or from an empty condition, causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable (OE) input is low. OE does not affect the output flags. Cascading is easily accomplished in the word-width direction but is not possible in the word-depth direction.

The SN74ALS233B is characterized for operation from 0°C to 70°C.

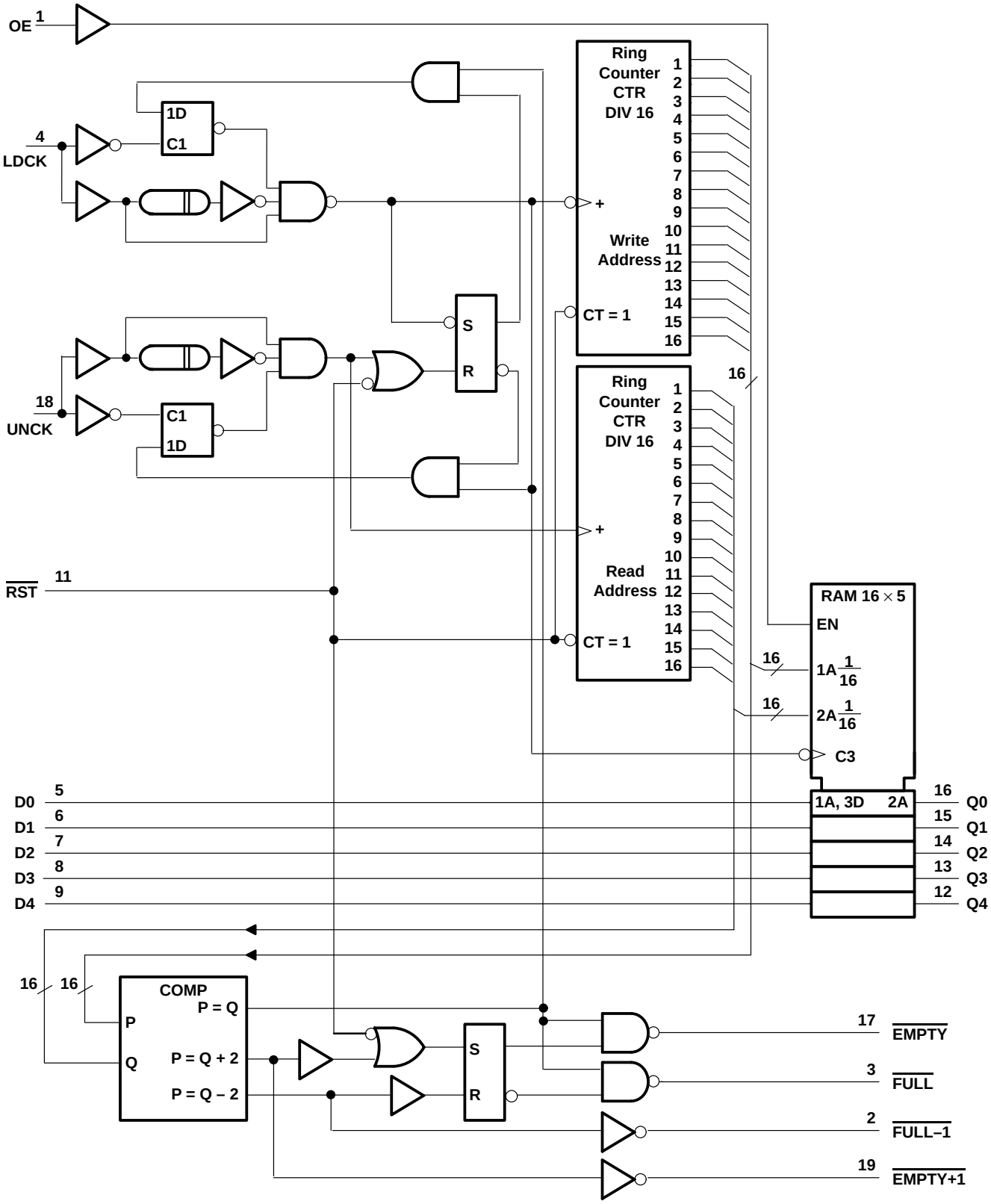
logic symbol†



† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

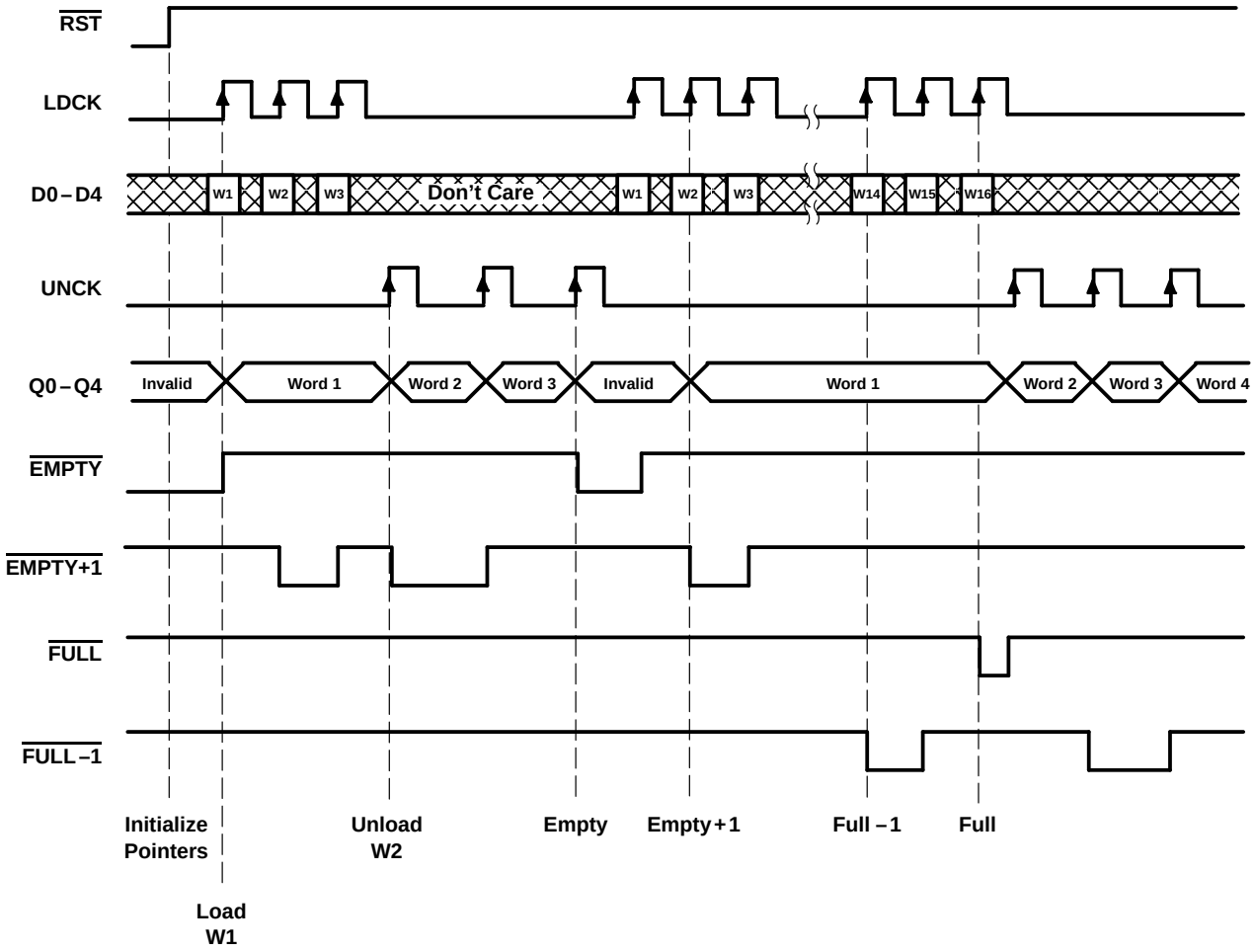
Pin numbers shown are for the DW and N packages.

logic diagram (positive logic)



Pin numbers shown are for the DW and N packages.

timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q outputs			–1.6	mA
		Status flags			–0.4	
I_{OL}	Low-level output current	Q outputs			24	mA
		Status flags			8	
f_{clock}	Clock frequency	LDCK	0		40	MHz
		UNCK	0		40	
t_w	Pulse duration	$\overline{RST}$ low	18			ns
		LDCK low	15			
		LDCK high	10			
		UNCK low	15			
		UNCK high	10			
t_{su}	Setup time	Data before LDCK↑	8			ns
		$\overline{RST}$ (inactive) before LDCK↑	5			
		LDCK (inactive) before $\overline{RST}$↑	5			
t_h	Hold time	Data after LDCK↑	5			ns
T_A	Operating free-air temperature		0		70	°C

NOTE 1: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates the V_{IL}, V_{IH}, or minimum pulse duration limits can cause a false clock or improper operation of the internal read and write pointers.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

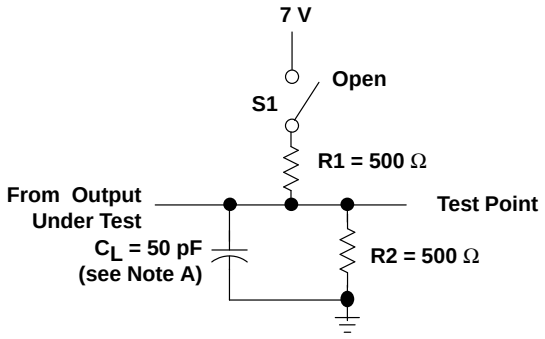
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	Q outputs	V_{CC} = 4.5 V,	I_{OH} = – 2.6 mA	2.4	3.2		V
	Status flags	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –0.4 mA	V_{CC}–2			
V_{OL}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
	Status flags	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			–20	µA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			–0.2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	mA
I_{CC}		V_{CC} = 5.5 V			88	133	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	MAX	
f_{max}	LDCK, UNCK		40		MHz
t_{pd}	LDCK↑	Any Q	6	32	ns
	UNCK↑		6	30	
t_{PLH}	LDCK↑	$\overline{\text{EMPTY}}$	5	25	ns
t_{PHL}	UNCK↑		6	27	
t_{PHL}	$\overline{\text{RST}}$↓	$\overline{\text{EMPTY}}$	5	25	ns
t_{pd}	LDCK↑	$\overline{\text{EMPTY+1}}$	7	34	ns
	UNCK↑		7	34	
t_{PLH}	$\overline{\text{RST}}$↓	$\overline{\text{EMPTY+1}}$	8	31	ns
t_{pd}	LDCK↑	$\overline{\text{FULL–1}}$	9	33	ns
	UNCK↑		8	32	
t_{PLH}	$\overline{\text{RST}}$↓	$\overline{\text{FULL–1}}$	11	32	ns
t_{PHL}	LDCK↑	$\overline{\text{FULL}}$	6	27	ns
t_{PLH}	UNCK↑	$\overline{\text{FULL}}$	5	25	ns
	$\overline{\text{RST}}$↓		9	30	
t_{en}	OE↑	Q	2	15	ns
t_{dis}	OE↓	Q	1	15	ns

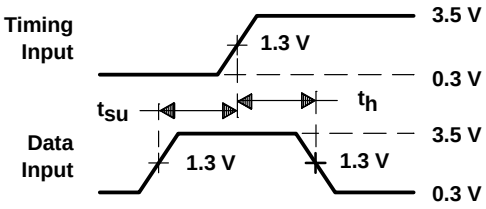
PARAMETER MEASUREMENT INFORMATION



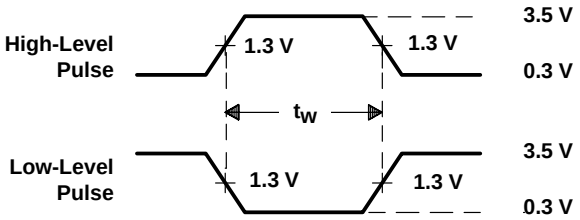
LOAD CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION TABLE

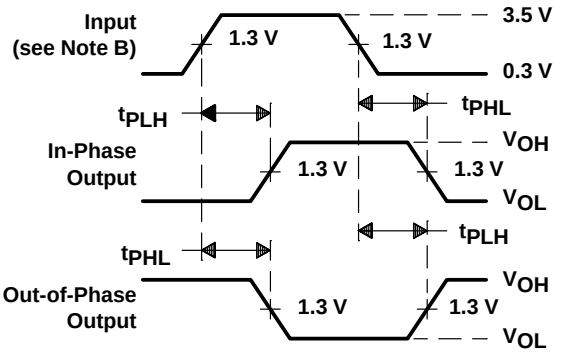
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



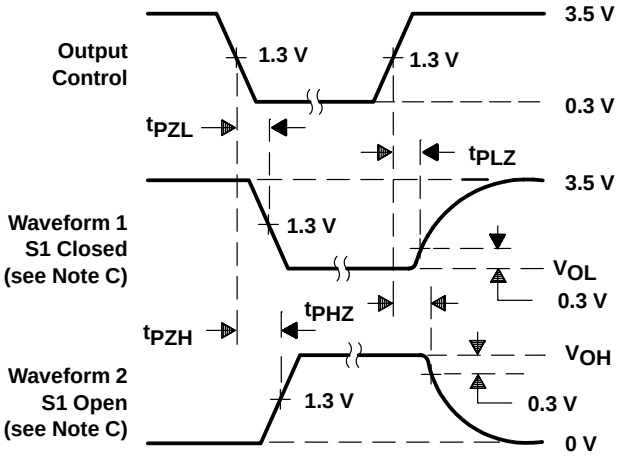
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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