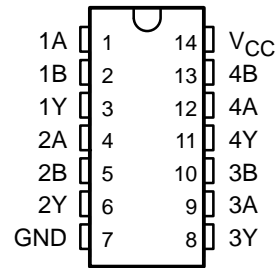


SN74LVC32A QUADRUPLE 2-INPUT POSITIVE-OR GATE

SCAS286C – JANUARY 1993 – REVISED AUGUST 1996

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per Mil-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-input positive-OR gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC32A performs the Boolean function $Y = A + B$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

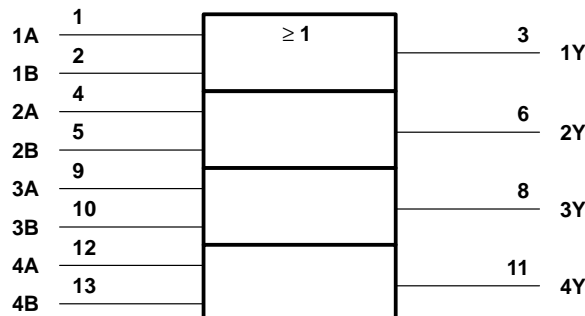
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC32A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each gate)

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | X | H |
| X | H | H |
| L | L | L |

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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**TEXAS
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SN74LVC32A
QUADRUPLE 2-INPUT POSITIVE-OR GATE

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logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Table with 2 columns: Parameter and Rating. Parameters include Supply voltage range, Input voltage range, Output voltage range, Input clamp current, Output clamp current, Continuous output current, Continuous current through VCC or GND, Maximum power dissipation, and Storage temperature range.

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- 2. The value of VCC is provided in the recommended operating conditions table.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the ABT Advanced BiCMOS Technology Data Book.

recommended operating conditions (see Note 4)

Table with 5 columns: Parameter, Description, Condition, MIN, MAX, UNIT. Parameters include VCC, VIH, VIL, VI, VO, IOH, IOL, Δt/Δv, and TA.

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

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QUADRUPLE 2-INPUT POSITIVE-OR GATE

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP† | MAX | UNIT |
|------------------|--|-----------------|-----------------------|------|-----|------|
| V _{OH} | I _{OH} = –100 µA | 2.7 V to 3.6 V | V _{CC} – 0.2 | | | V |
| | I _{OH} = –12 mA | 2.7 V | 2.2 | | | |
| | | 3 V | 2.4 | | | |
| | I _{OH} = –24 mA | 3 V | 2.2 | | | |
| V _{OL} | I _{OL} = 100 µA | 2.7 V to 3.6 V | 0.2 | | | V |
| | I _{OL} = 12 mA | 2.7 V | 0.4 | | | |
| | I _{OL} = 24 mA | 3 V | 0.55 | | | |
| I _I | V _I = 5.5 V or GND | 3.6 V | ±5 | | | µA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 3.6 V | 10 | | | µA |
| ΔI _{CC} | One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND | 2.7 V to 3.6 V | 500 | | | µA |
| C _i | V _I = V _{CC} or GND | 3.3 V | 5 | | | pF |

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 2.7 V | | UNIT |
|----------------------|--------------|-------------|---------------------------------|-----|-------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| t _{pd} | A or B | Y | 1.5 | 3.8 | 4.4 | | ns |
| t _{sk(o)} ‡ | | | 1 | | | | ns |

‡ Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

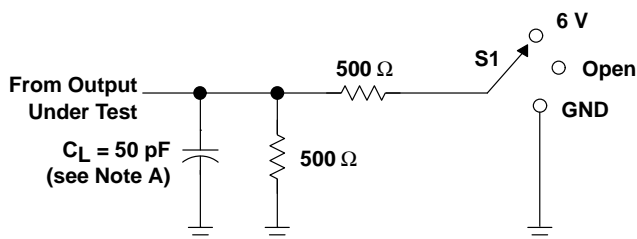
| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|--|------------------------------------|------|------|
| C _{pd} Power dissipation capacitance per gate | C _L = 50 pF, f = 10 MHz | 12.5 | pF |

SN74LVC32A

QUADRUPLE 2-INPUT POSITIVE-OR GATE

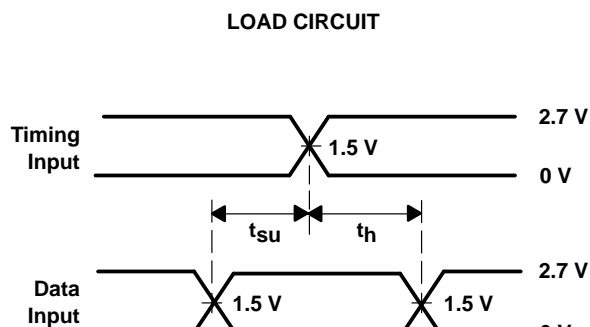
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PARAMETER MEASUREMENT INFORMATION

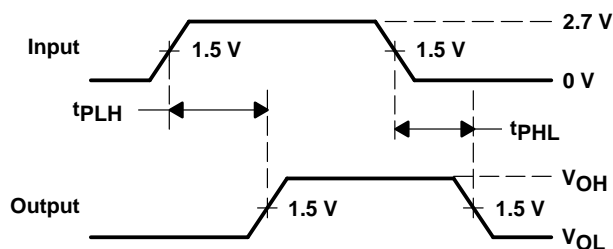


LOAD CIRCUIT

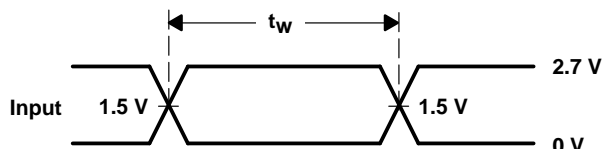
| TEST | S1 |
|-------------------|------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |



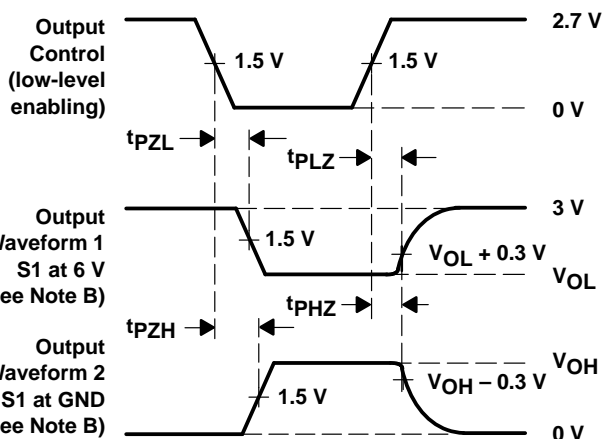
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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