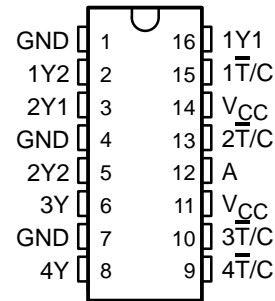


# CDC329A 1-LINE TO 6-LINE CLOCK DRIVER WITH SELECTABLE POLARITY

SCAS328A – DECEMBER 1992 – REVISED NOVEMBER 1995

- Low Output Skew for Clock-Distribution and Clock-Generation Applications
- TTL-Compatible Inputs and CMOS-Compatible Outputs
- Distributes One Clock Input to Six Clock Outputs
- Polarity Control Selects True or Complementary Outputs
- Distributed  $V_{CC}$  and GND Pins Reduce Switching Noise
- High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $32\text{-mA } I_{OL}$ )
- State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation
- Package Options Include Plastic Small-Outline (D) and Shrink Small-Outline (DB) Packages

D OR DB PACKAGE  
(TOP VIEW)



## description

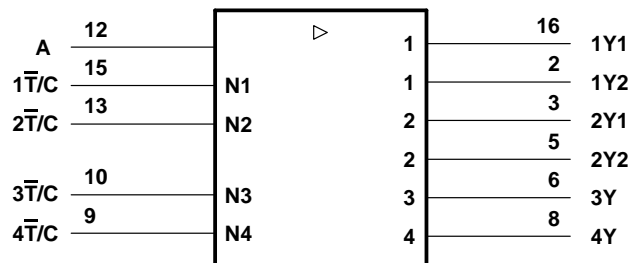
The CDC329A contains a clock-driver circuit that distributes one input signal to six outputs with minimum skew for clock distribution. Through the use of the polarity-control inputs ( $\overline{T/C}$ ), various combinations of true and complementary outputs can be obtained.

The CDC329A is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

INPUTS		OUTPUT Y
$\overline{T/C}$	A	
L	L	L
L	H	H
H	L	H
H	H	L

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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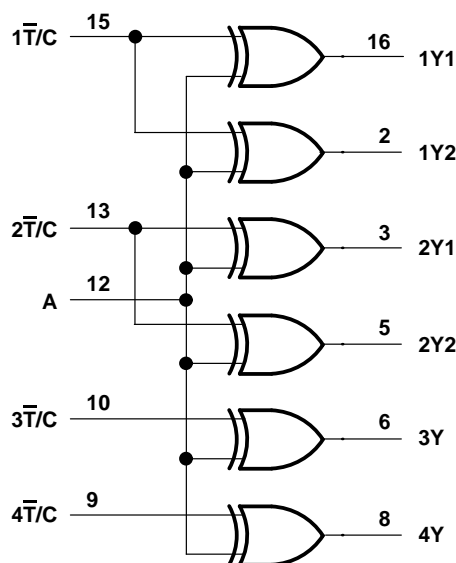
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, $I_O$	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): D package	0.77 W
DB package	0.6 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 300 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

# CDC329A

## 1-LINE TO 6-LINE CLOCK DRIVER WITH SELECTABLE POLARITY

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### recommended operating conditions (see Note 3)

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			V
$V_{IL}$ Low-level input voltage			0.8	V
$V_I$ Input voltage	0	$V_{CC}$		V
$I_{OH}$ High-level output current			-32	mA
$I_{OL}$ Low-level output current			32	mA
$\Delta t/\Delta v$ Input transition rise or fall rate			5	ns/V
$f_{clock}$ Input clock frequency			80	MHz
$T_A$ Operating free-air temperature	-40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.75$ V,	$I_I = -18$ mA			-1.2	V
$V_{OH}$	$V_{CC} = 4.75$ V,	$I_{OH} = -32$ mA	3.85			V
$V_{OL}$	$V_{CC} = 4.75$ V,	$I_{OL} = 32$ mA			0.55	V
$I_I$	$V_{CC} = 5.25$ V,	$V_I = V_{CC}$ or GND			$\pm 1$	$\mu$ A
$I_{CC}$	$V_{CC} = 5.25$ V, $V_I = V_{CC}$ or GND	$I_O = 0$ , Outputs high			10	mA
		Outputs low			40	
$C_i$	$V_I = 2.5$ V or 0.5 V			3		pF

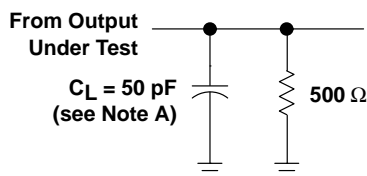
† All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$

### switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 and 2)

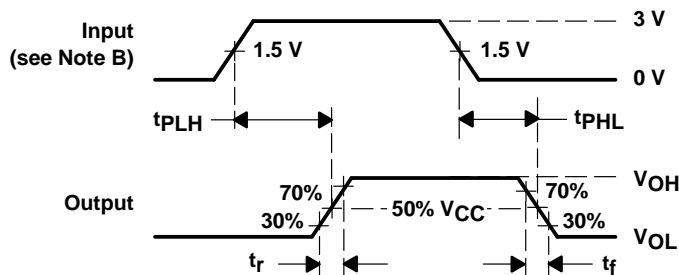
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
$t_{PLH}$	A	Any Y	2		5.9	ns
$t_{PHL}$			1.7		5.9	
$t_{PLH}$	$\overline{T}/C$	Any Y	1.5		5	ns
$t_{PHL}$			1.5		5	
$t_{sk(o)}$	A	Any Y (same phase)			0.6	ns
		Any Y (any phase)			1.5	
$t_r$				1.3		ns
$t_f$				0.85		ns



## PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS



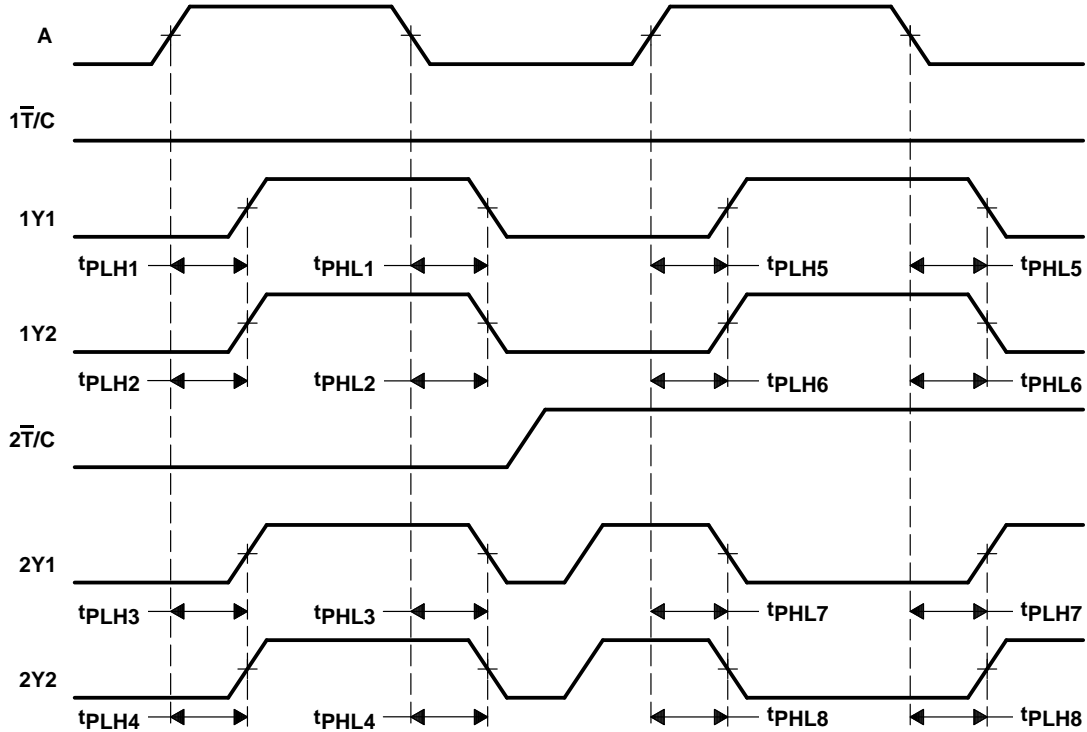
VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES

NOTES: A.  $C_L$  includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Output skew,  $t_{sk(o)}$ , from A to any Y (same phase), can be measured only between outputs for which the respective polarity-control inputs ( $\overline{T/C}$ ) are at the same logic level. It is calculated as the greater of:
- The difference between the fastest and slowest of  $t_{PHL}$  from  $A\downarrow$  to any Y (e.g.,  $t_{PHLn}$ ,  $n = 1$  to 4; or  $t_{PHLn}$ ,  $n = 5$  to 6)
  - The difference between the fastest and slowest of  $t_{PLH}$  from  $A\downarrow$  to any Y (e.g.,  $t_{PLHn}$ ,  $n = 1$  to 4; or  $t_{PLHn}$ ,  $n = 5$  to 6)
  - The difference between the fastest and slowest of  $t_{PLH}$  from  $A\downarrow$  to any Y (e.g.,  $t_{PLHn}$ ,  $n = 7$  to 8)
  - The difference between the fastest and slowest of  $t_{PHL}$  from  $A\uparrow$  to any Y (e.g.,  $t_{PHLn}$ ,  $n = 7$  to 8)
- B. Output skew,  $t_{sk(o)}$ , from A to any Y (any phase), can be measured between outputs for which the respective polarity-control inputs ( $\overline{T/C}$ ) are at the same or different logic levels. It is calculated as the greater of:
- The difference between the fastest and slowest of  $t_{PLH}$  from  $A\uparrow$  to any Y or  $t_{PHL}$  from  $A\uparrow$  to any Y (e.g.,  $t_{PLHn}$ ,  $n = 1$  to 4; or  $t_{PLHn}$ ,  $n = 5$  to 6, and  $t_{PHLn}$ ,  $n = 7$  to 8)
  - The difference between the fastest and slowest of  $t_{PHL}$  from  $A\downarrow$  to any Y or  $t_{PLH}$  from  $A\downarrow$  to any Y (e.g.,  $t_{PHLn}$ ,  $n = 1$  to 4; or  $t_{PHLn}$ ,  $n = 5$  to 6, and  $t_{PLHn}$ ,  $n = 7$  to 8)

**Figure 2. Waveforms for Calculation of  $t_{sk(o)}$**

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