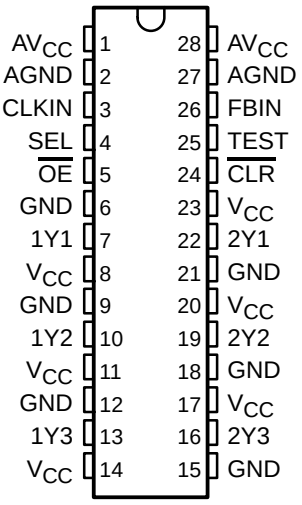
- **Low-Output Skew for Clock-Distribution and Clock-Generation Applications**
- **Operates at 3.3-V V_{CC}**
- **Distributes One Clock Input to Six Outputs**
- **One Select Input Configures Three Outputs to Operate at One-Half or Double the Input Frequency**
- **No External RC Network Required**
- **External Feedback Pin (FBIN) Is Used to Synchronize the Outputs to the Clock Input**
- **Application for Synchronous DRAM, High-Speed Microprocessor**
- **Negative-Edge-Triggered Clear for Half-Frequency Outputs**
- **TTL-Compatible Inputs and Outputs**
- **Outputs Drive 50-Ω Parallel-Terminated Transmission Lines**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **Packaged in Plastic 28-Pin Shrink Small Outline Package**

DL PACKAGE
(TOP VIEW)



description

The CDC536 is a high-performance, low-skew, low-jitter clock driver. It uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the clock output signals to the clock input (CLKIN) signal. It is specifically designed for use with synchronous DRAMs and popular microprocessors operating at speeds from 50 MHz to 100 MHz or down to 25 MHz on outputs configured as half-frequency outputs. The CDC536 operates at 3.3-V V_{CC} and is designed to drive a properly terminated 50-Ω transmission line.

The feedback input (FBIN) is used to synchronize the output clocks in frequency and phase to the input clock (CLKIN). One of the six output clocks must be fed back to FBIN for the PLL to maintain synchronization between CLKIN and the outputs. The output used as the feedback pin is synchronized to the same frequency as CLKIN.

The Y outputs can be configured to switch in phase and at the same frequency as CLKIN. The select (SEL) input configures three Y outputs to operate at one-half or double the CLKIN frequency depending on which pin is fed back to FBIN (see Tables 1 and 2). All output signal duty cycles are adjusted to 50% independent of the duty cycle at the input clock.

Output-enable ($\overline{OE}$) is provided for output control. When $\overline{OE}$ is high, the outputs are in the high-impedance state. When $\overline{OE}$ is low, the outputs are active. $\overline{CLR}$ is negative-edge triggered and can be used to reset the outputs operating at half frequency. TEST is used for factory testing of the device and can be use to bypass the PLL. TEST should be strapped to GND for normal operation.

Unlike many products containing PLLs, the CDC536 does not require external RC networks. The loop filter for the PLL is included on chip, minimizing component count, board space, and cost.

description (continued)

Because it is based on PLL circuitry, the CDC536 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required following power up and application of a fixed-frequency, fixed-phase signal at CLKIN as well as following any changes to the PLL reference or feedback signals. Such changes occur upon change of the select inputs, enabling the PLL via TEST, and upon enable of all outputs via $\overline{OE}$.

The CDC536 is characterized for operation from 0°C to 70°C.

detailed description of output configurations

The voltage-controlled oscillator (VCO) in the CDC536 has a frequency range of 100 MHz to 200 MHz, twice the operating frequency range of the CDC536 outputs. The output of the VCO is divided by two and by four to provide reference frequencies with a 50% duty cycle of one-half and one-fourth the VCO frequency. The SEL0 and SEL1 inputs determine which of the two signals are buffered to each bank of device outputs.

One device output must be externally wired to FBIN to complete the PLL. The VCO operates such that the frequency of this output matches that of the CLKIN signals. In the case that a VCO/2 output is wired to FBIN, the VCO must operate at twice the CLKIN frequency, resulting in device outputs that operate at the same or one-half the CLKIN frequency. If a VCO/4 output is wired to FBIN, the device outputs operate at the same or twice the CLKIN frequency.

output configuration A

Output configuration A is valid when any output configured as a 1× frequency output in Table 1 is fed back to the FBIN input. The input frequency range for the CLKIN input is 50 MHz to 100 MHz when using output configuration A. Outputs configured as 1/2× outputs operate at half the CLKIN frequency, while outputs configured as 1× outputs operate at the same frequency as the CLKIN input.

Table 1. Output Configuration A

INPUTS	OUTPUTS	
SEL	1/2× FREQUENCY	1× FREQUENCY
L	None	All
H	1Yn	2Yn

NOTE: n = 1, 2, 3

output configuration B

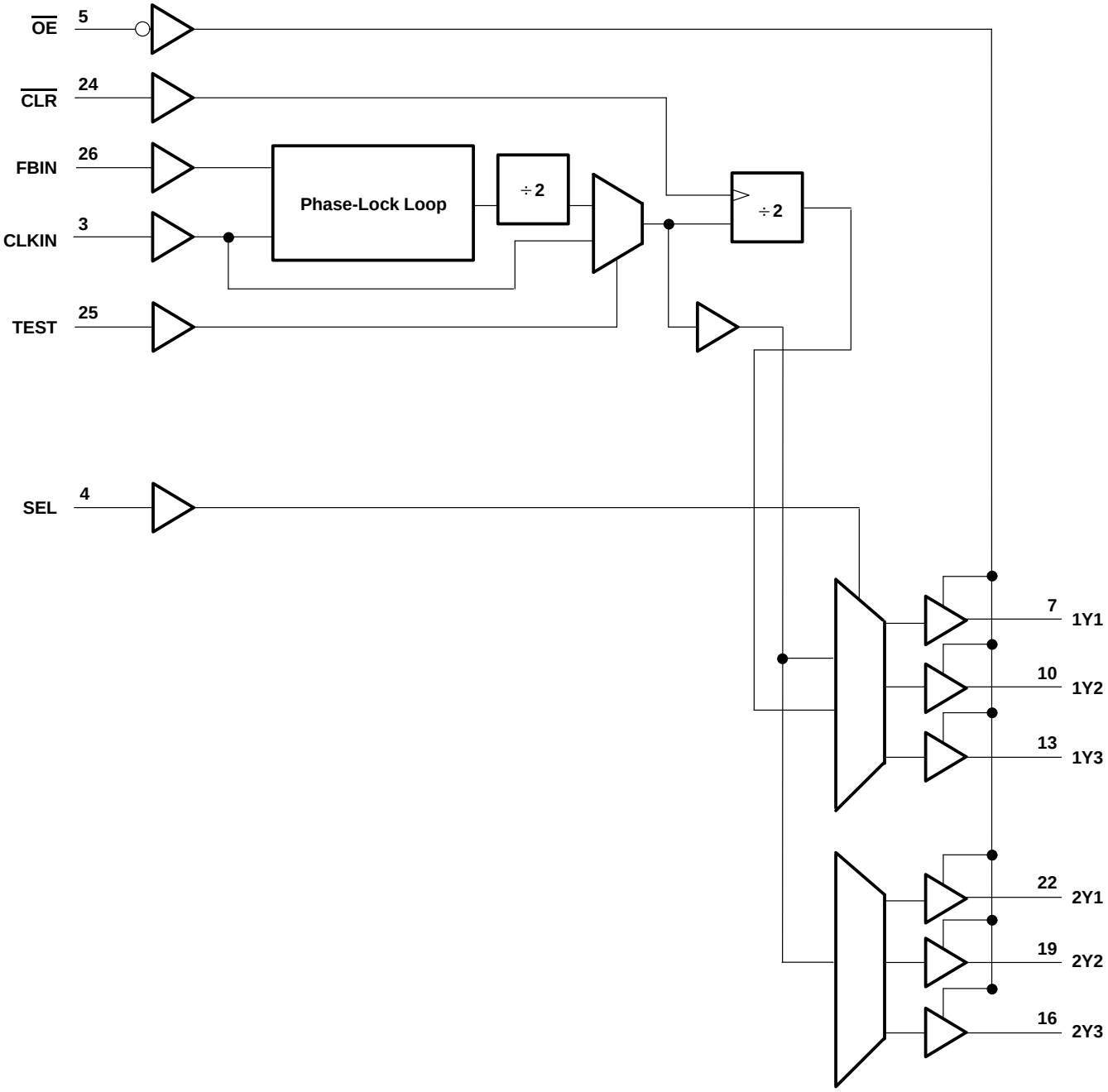
Output configuration B is valid when any output configured as a 1× frequency output in Table 2 is fed back to FBIN. The input frequency range for the CLKIN input is 25 MHz to 50 MHz when using output configuration B. Outputs configured as 1× outputs operate at the CLKIN frequency, while outputs configured as 2× outputs operate at double the frequency of the CLKIN input.

Table 2. Output Configuration B

INPUTS	OUTPUTS	
SEL	1× FREQUENCY	2× FREQUENCY
L	All	None
H	1Yn	2Yn

NOTE: n = 1, 2, 3

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLKIN	3	I	Clock input. CLKIN provides the clock signal to be distributed by the CDC536 clock-driver circuit. CLKIN is used to provide the reference signal to the integrated phase-lock loop that generates the clock output signals. CLKIN must have a fixed frequency and fixed phase in order for the phase-lock loop to obtain phase lock. Once the circuit is powered up and a valid CLKIN signal is applied, a stabilization time is required for the phase-lock loop to phase lock the feedback signal to its reference signal.
$\overline{\text{CLR}}$	24	I	Clear. $\overline{\text{CLR}}$ is used to reset the VCO/4 reference frequency. $\overline{\text{CLR}}$ is negative-edge triggered and should be strapped to V_{CC} or GND for normal operation.
FBIN	26	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard wired to one of the six clock outputs to provide frequency and phase lock. The internal PLL adjusts the output clocks to obtain zero phase delay between the FBIN and differential CLKIN inputs.
$\overline{\text{OE}}$	5	I	Output enable. $\overline{\text{OE}}$ is the output enable for all outputs. When $\overline{\text{OE}}$ is low, all outputs are enabled. When $\overline{\text{OE}}$ is high, all outputs are in the high-impedance state. Since the feedback signal for the phase-lock loop is taken directly from an output, placing the outputs in the high-impedance state interrupts the feedback loop; therefore, when a high-to-low transition occurs at $\overline{\text{OE}}$, enabling the output buffers, a stabilization time is required before the phase-lock loop obtains phase lock.
SEL	4	I	Output configuration select. SEL selects the output configuration for each output bank (e.g. 1×, 1/2×, or 2×). (see Tables 1 and 2).
TEST	25	I	TEST is used to bypass the phase-lock loop circuitry for factory testing of the device. When TEST is low, all outputs operate using the PLL circuitry. When TEST is high, the outputs are placed in a test mode that bypasses the PLL circuitry. TEST should be grounded for normal operation.
1Y1–1Y3	7, 10, 13	O	These outputs are configured by SEL to transmit one-half or one-fourth the frequency of the VCO. The relationship between the CLKIN frequency and the output frequency is dependent on SEL. The duty cycle of the Y output signals is nominally 50%, independent of the duty cycle of the CLKIN signal. Since the phase of the output signals configured as half-frequency outputs cannot be determined at power up, $\overline{\text{CLR}}$ is provided to allow the outputs of multiple CDC536 circuits operating at half-frequency to be reset to the same phase.
2Y1–2Y3	22, 19, 16	O	These outputs transmit one-half the frequency of the VCO. The relationship between the CLKIN frequency and the output frequency is dependent on the frequency of the output being fed back to FBIN. The duty cycle of the Y output signals is nominally 50% independent of the duty cycle of the CLKIN signal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O . . . . . 64 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –20 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) . . . . . 0.7 W
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
T_A	Operating free-air temperature	0	70	°C

NOTE 3: Unused inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C MIN	T_A = 25°C MAX	UNIT
V_{IK}	V_{CC} = 3 V,	I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2		V
	V_{CC} = 3 V,	I_{OH} = – 32 mA		2		
V_{OL}	V_{CC} = 3 V,	I_{OL} = 100 µA			0.2	V
	V_{CC} = 3 V,	I_{OL} = 32 mA			0.5	
I_I	V_{CC} = 0 or MAX‡,	V_I = 3.6 V			±10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1	
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			10	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0			–10	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		2	mA
			Outputs low		2	
			Outputs disabled		2	
C_i	V_I = V_{CC} or GND				6	pF
C_o	V_O = V_{CC} or GND				9	pF

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency	When VCO is operating at four times the CLKIN frequency	25	50	MHz
		When VCO is operating at double the CLKIN frequency	50	100	
	Input clock duty cycle		40%	60%	
	Stabilization time†	After SEL		50	µs
		After $\overline{OE}\downarrow$		50	
		After power up		50	
		After CLKIN		50	

† Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

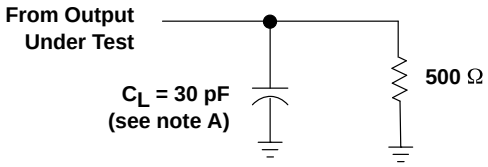
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Note 4 and Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}			100		MHz
Duty cycle		Y	45%	55%	
$t_{phase\ error}$‡	CLKIN↑	Y	–500	+500	ps
$Jitter_{(pk-pk)}$	CLKIN↑	Y		200	ps
$t_{sk(o)}$‡				0.5	ns
$t_{sk(pr)}$				1	ns
t_r				1.4	ns
t_f				1.4	ns

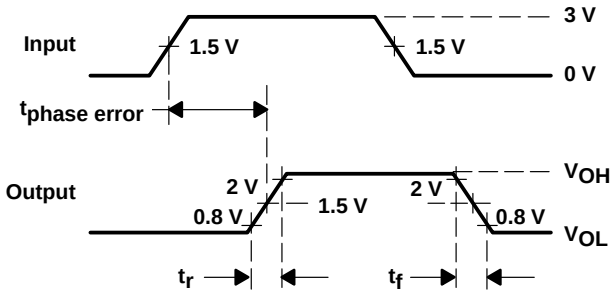
‡ The propagation delay, $t_{phase\ error}$, is dependent on the feedback path from any output to FBIN. The $t_{phase\ error}$, $t_{sk(o)}$, and $t_{sk(pk)}$ specifications are only valid for equal loading of all outputs.

NOTE 4: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS

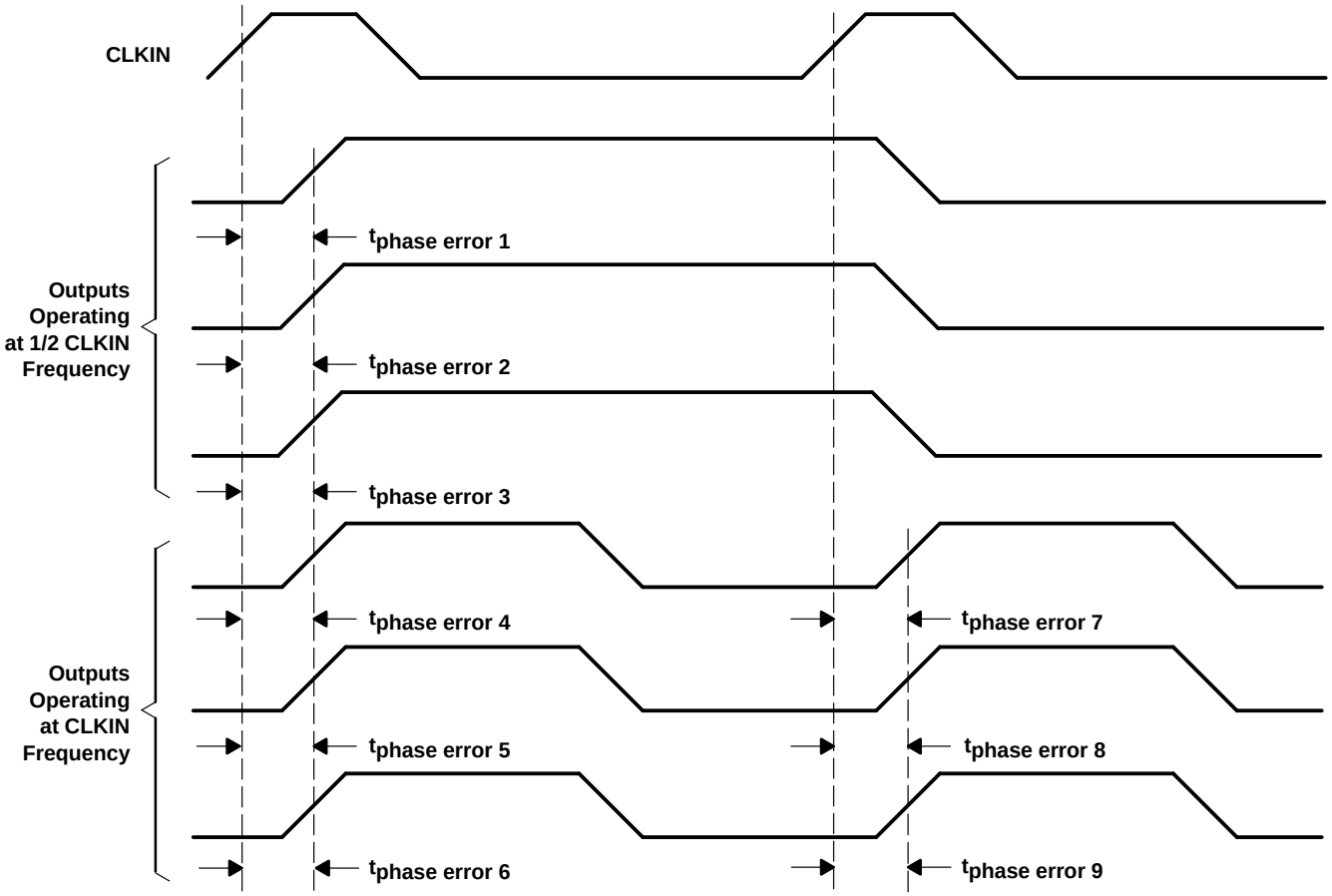


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 100 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

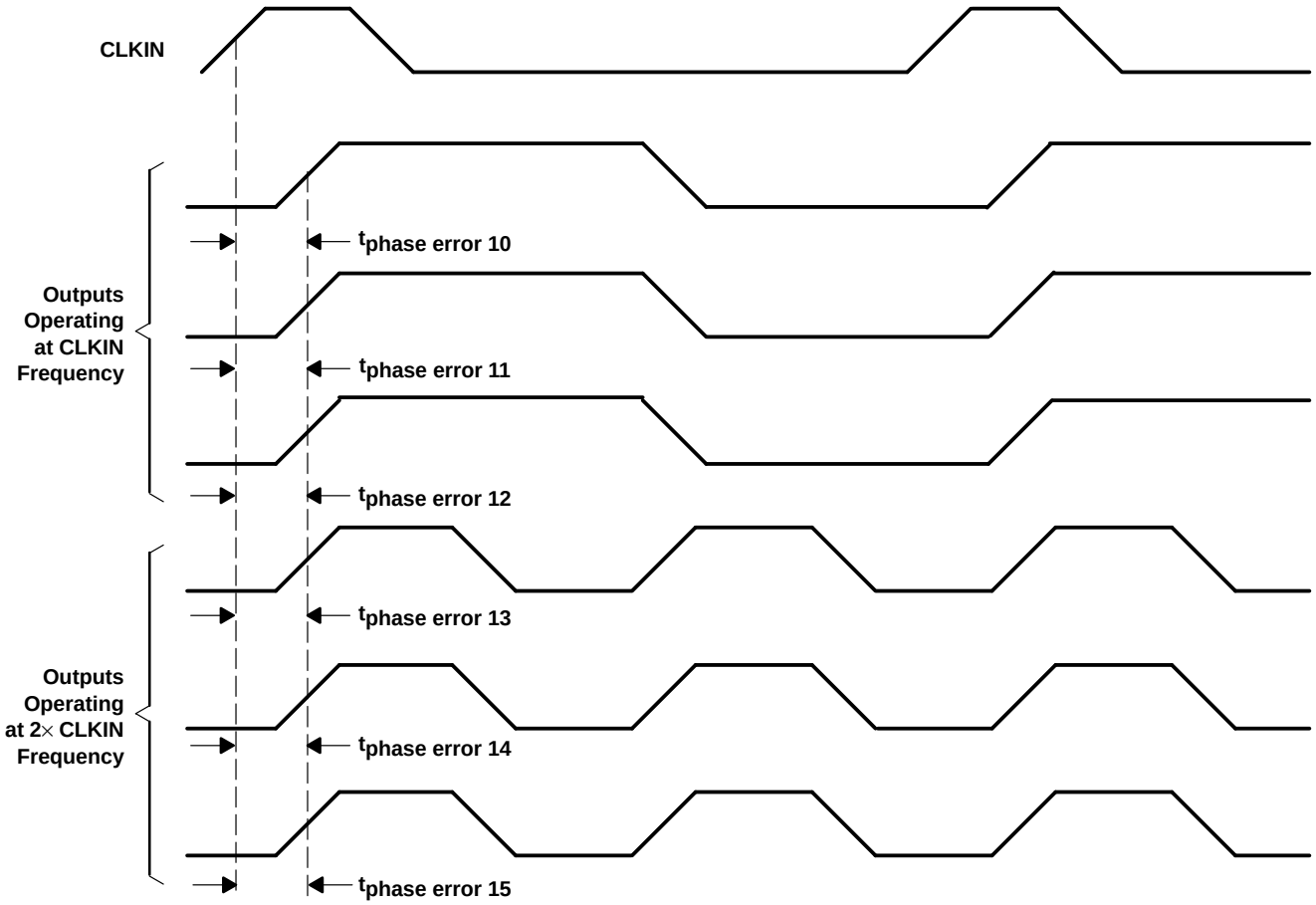


NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 1, 2, . . . 6)
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 7, 8, 9)

B. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
- The difference between the maximum and minimum $t_{phase\ error\ n}$ (n = 1, 2, . . . 6) across multiple devices under identical operating conditions.
- The difference between the maximum and minimum $t_{phase\ error\ n}$ (n = 7, 8, 9) across multiple devices under identical operating conditions.

Figure 2. Skew Waveforms and Calculations

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
– The difference between the fastest and slowest of $t_{\text{phase error n}}$ (n = 10, 11, . . . 15)
B. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
– The difference between the maximum and minimum $t_{\text{phase error n}}$ (n = 10, 11, . . . 15) across multiple devices under identical operating conditions.

Figure 3. Waveforms for Calculation of $t_{sk(o)}$ and $t_{sk(pr)}$

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