

# SN54AC573, SN74AC573 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SCAS542B - OCTOBER 1995 - REVISED NOVEMBER 1996

- 3-State Outputs Drive Bus Lines Directly
- **EPIC™** (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- Package Options Include Plastic Small-Outline (DW) Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic (N) and Ceramic (J) DIPs

## description

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

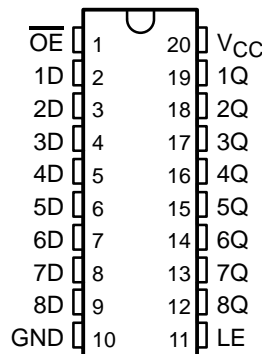
The eight latches are D-type transparent latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D Inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines in a bus-organized system without need for interface or pullup components.

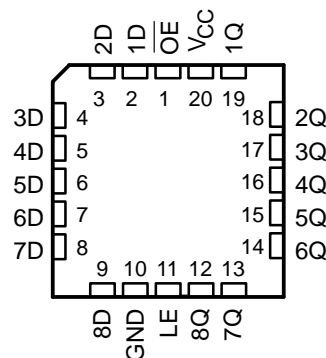
$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AC573 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74AC573 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

SN54AC573 . . . J OR W PACKAGE  
SN74AC573 . . . DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



SN54AC573 . . . FK PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z



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**TEXAS  
INSTRUMENTS**

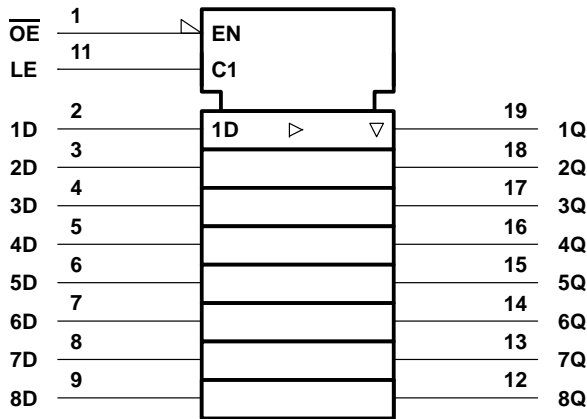
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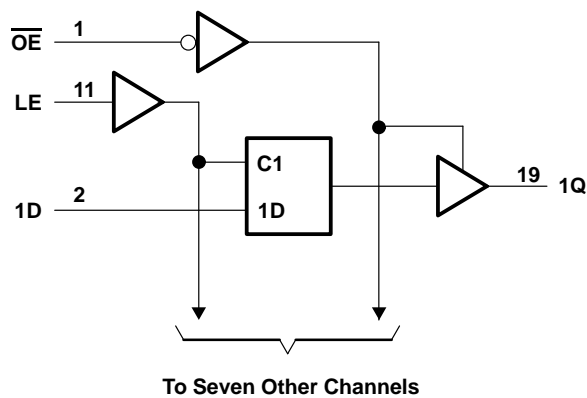
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logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	–0.5 V to + 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through, $V_{CC}$ or GND	±200 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package	0.6 W
DW package	1.6 W
N package	1.3 W
PW package	0.7 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

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## recommended operating conditions (see Note 3)

			SN54AC573		SN74AC573		UNIT
			MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage		2	6	2	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 3\text{ V}$	2.1		2.1		V
		$V_{CC} = 4.5\text{ V}$	3.15		3.15		
		$V_{CC} = 5.5\text{ V}$	3.85		3.85		
$V_{IL}$	Low-level input voltage	$V_{CC} = 3\text{ V}$		0.9		0.9	V
		$V_{CC} = 4.5\text{ V}$		1.35		1.35	
		$V_{CC} = 5.5\text{ V}$		1.65		1.65	
$V_I$	Input voltage		0	$V_{CC}$	0	$V_{CC}$	V
$V_O$	Output voltage		0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 3\text{ V}$		-12		-12	mA
		$V_{CC} = 4.5\text{ V}$		-24		-24	
		$V_{CC} = 5.5\text{ V}$		-24		-24	
$I_{OL}$	Low-level output current	$V_{CC} = 3\text{ V}$		12		12	mA
		$V_{CC} = 4.5\text{ V}$		24		24	
		$V_{CC} = 5.5\text{ V}$		24		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	8	0	8	ns/V
$T_A$	Operating free-air temperature		-55	125	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54AC573		SN74AC573		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$	$I_{OH} = -50\text{ }\mu\text{A}$	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	$I_{OH} = -12\text{ mA}$	3 V	2.58			2.48		2.48		
		4.5 V	3.94			3.8		3.8		
		5.5 V	4.94			4.8		4.8		
$V_{OL}$	$I_{OL} = 50\text{ }\mu\text{A}$	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	$I_{OL} = 12\text{ mA}$	3 V			0.36		0.44		0.44	
		4.5 V			0.36		0.44		0.44	
		5.5 V			0.36		0.44		0.44	
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu\text{A}$
		5.5 V			$\pm 0.25$		$\pm 5$		$\pm 2.5$	$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		80		40	$\mu\text{A}$
$C_i$	$V_I = V_{CC}$ or GND	5 V		5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

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# SN54AC573, SN74AC573

## OCTAL D-TYPE TRANSPARENT LATCHES

### WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54AC573		SN74AC573		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_W$	Pulse duration, LE high	6		8		7		ns
$t_{SU}$	Setup time, data before LE↓	3.5		5		4		ns
$t_H$	Hold time, data after LE↓	2		3		2		ns

timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54AC573		SN74AC573		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_W$	Pulse duration, LE high	4		6		5		ns
$t_{SU}$	Setup time, data before LE↓	3		4.5		3.5		ns
$t_H$	Hold time, data after LE↓	2		3		2		ns

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$		SN54AC573		SN74AC573		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	D	Q	2.5	13	1.5	16.5	2	15	ns
$t_{PHL}$			2.5	12	1.5	15.5	2	14	
$t_{PLH}$	LE	Q	2.5	13	1.5	16.5	2	15	ns
$t_{PHL}$			2.5	12	1.5	15.5	2	14	
$t_{PZH}$	OE	Q	2.5	11	1.5	13.5	2	12	ns
$t_{PZL}$			2.5	11	1.5	14	2	12.5	
$t_{PHZ}$	$\overline{OE}$	Q	2.5	12.5	1.5	15	2	13.5	ns
$t_{PLZ}$			2.5	9.5	1.5	12	2	10.5	

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$		SN54AC573		SN74AC573		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	D	Q	2.5	10	1.5	13	2	11.5	ns
$t_{PHL}$			2.5	9.5	1.5	12.5	2	11	
$t_{PLH}$	LE	Q	2.5	9.5	1.5	12.5	2	11	ns
$t_{PHL}$			2.5	8.5	1.5	11.5	2	10	
$t_{PZH}$	$\overline{OE}$	Q	2.5	9	1.5	11.5	2	10	ns
$t_{PZL}$			2.5	8.5	1.5	11	2	9.5	
$t_{PHZ}$	$\overline{OE}$	Q	2.5	11	1.5	13.5	2	12	ns
$t_{PLZ}$			2.5	8	1.5	10.5	2	9	

operating characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50 \text{ pF}$ , $f = 1 \text{ MHz}$	25	pF

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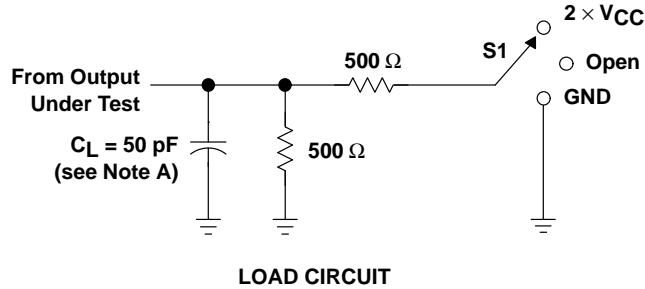


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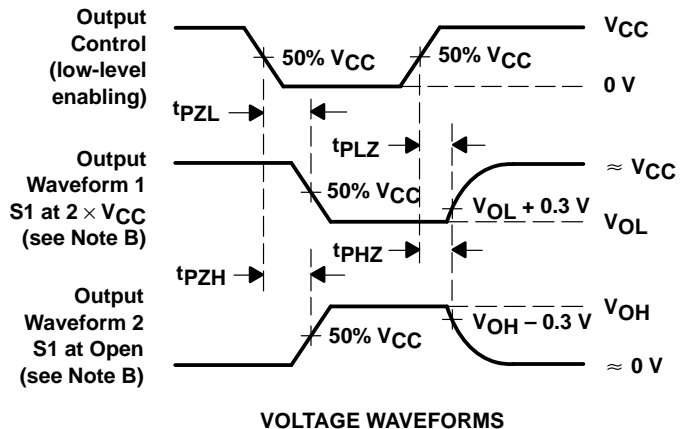
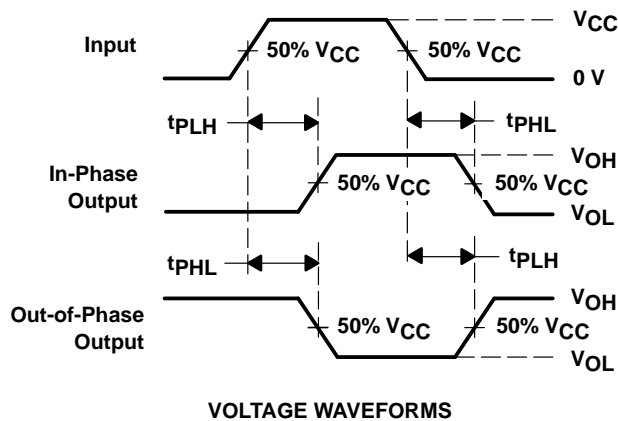
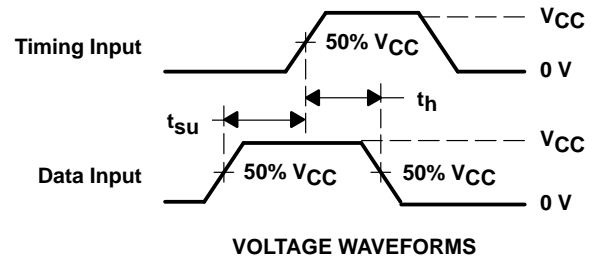
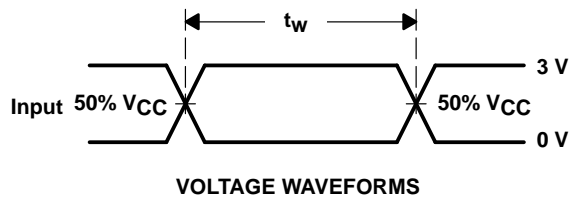
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## PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	Open



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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