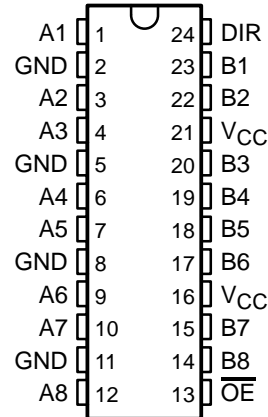


- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- Designed to Facilitate Incident-Wave Switching for Line Impedances of 25 Ω or Greater
- Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs
- Data Flow-Through Pinout (All Inputs on Opposite Side From Outputs)
- High-Impedance State During Power Up and Power Down
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (NT)

DW OR NT PACKAGE
(TOP VIEW)



description

The SN64BCT25245 is a 25-Ω octal bus transceiver designed for asynchronous communication between data buses. It improves both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented transceivers.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can disable the device so that both buses are effectively isolated.

This transceiver is capable of sinking 188-mA I_{OL} , which facilitates switching 25-Ω transmission lines on the incident wave. The distributed V_{CC} and GND pins minimize switching noise for more reliable system operation.

The outputs are in a high-impedance state during power up and power down while the supply voltage is less than approximately 3 V.

The SN64BCT25245 is characterized for operation from -40°C to 85°C and 0°C to 70°C.

FUNCTION TABLE

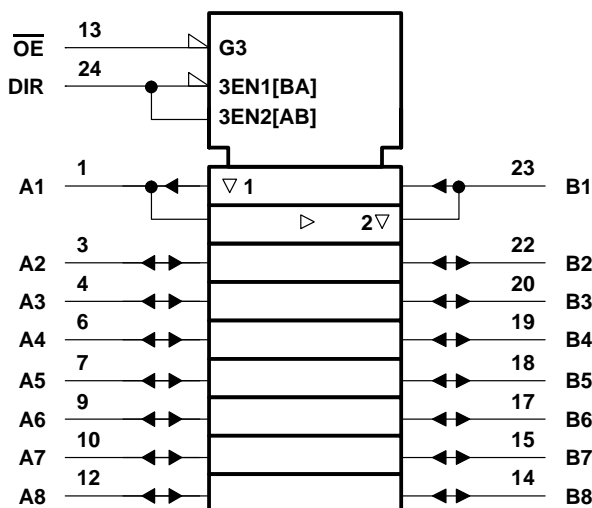
INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

SN64BCT25245

25-Ω OCTAL BUS TRANSCEIVER

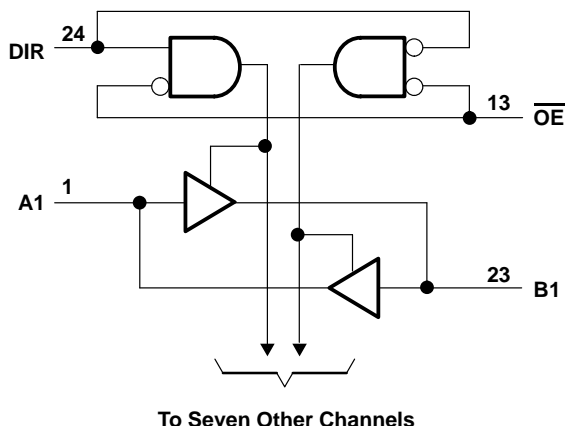
SCBS060A – JUNE 1990 – REVISED DECEMBER 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1): Control inputs	–0.5 V to 7 V
I/O ports	–0.5 V to 5.5 V
Voltage range applied to any output in the disabled or power-off state, V_O	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (B port)	–0.5 V to V_{CC}
Input clamp current, I_{IK}	–30 mA
Current into any output in the low state, I_O : A port	376 mA
B port	48 mA
Operating free-air temperature range	–40°C to 85°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–80	mA
				–3	
I_{OL}	Low-level output current			188	mA
				24	
T_A	Operating free-air temperature	–40		85	°C



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
V_{OH}	A port	$V_{CC} = 4.75\text{ V}$,	$I_{OH} = -3\text{ mA}$	2.7			V
	B port	$V_{CC} = 4.5\text{ V}$,	$I_{OH} = -80\text{ mA}$	2			
V_{OL}	A port	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 94\text{ mA}$		0.42	0.55	V
	B port	$V_{CC} = 4.5\text{ V}$,	$I_{OL} = 188\text{ mA}$			0.7	
I_{OZ}		$V_{CC} = 0\text{ to }2.3\text{ V}$ (power up)	$V_O = 2.7\text{ V}$			70	μA
			$V_O = 0.5\text{ V}$			-0.6	mA
		$V_{CC} = 1.8\text{ V to }0$ (power down)	$V_O = 2.7\text{ V}$			70	μA
			$V_O = 0.5\text{ V}$			-0.6	mA
I_I	A and B ports	$V_{CC} = 0\text{ to }5.5\text{ V}$,	$V_I = 5.5\text{ V}$			0.25	mA
	DIR and \overline{OE}					0.1	
I_{IH}^\ddagger	A and B ports	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$			70	μA
	DIR and \overline{OE}					20	
I_{IL}^\ddagger	A and B ports	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.5\text{ V}$			-0.6	mA
	DIR and \overline{OE}						
I_{OS}^\S	B port [¶]	$V_{CC} = 5.5\text{ V}$,	$V_O = 0$	-60		-150	mA
I_{CCL}	A to B port	$V_{CC} = 5.5\text{ V}$			48	60	mA
	B to A port				95	125	
I_{CCH}	A to B port	$V_{CC} = 5.5\text{ V}$			36	46	mA
	B to A port				63	80	
I_{CCZ}		$V_{CC} = 5.5\text{ V}$			12	16	mA
C_i	\overline{OE} and DIR	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.5\text{ V to }0.5\text{ V}$		8		pF
C_{io}	A port	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.5\text{ V to }0.5\text{ V}$		18		pF
	B port				8		

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state outputs current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ Testing for this parameter on the A port is not recommended.

SN64BCT25245

25-Ω OCTAL BUS TRANSCEIVER

SCBS060A – JUNE 1990 – REVISED DECEMBER 1993

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω				UNIT
						T _A = –40°C to 85°C		T _A = 0°C to 70°C		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	B	1.2	3.3	5.1	1.2	5.7	1.2	5.7	ns
t _{PHL}			1.9	4.3	6.7	1.9	7.3	1.9	7.2	
t _{PLH}	B	A	1.2	3.3	4.8	1.2	5.5	1.2	5.5	ns
t _{PHL}			2.1	4	5.6	2.1	6.3	2.1	6.2	
t _{PZH}	$\overline{\text{OE}}$	A	3.7	6.3	8.4	3.7	9.7	3.7	9.6	ns
t _{PZL}			4.5	7.4	9.2	4.5	10.6	4.5	10.3	
t _{PHZ}	$\overline{\text{OE}}$	A	1.8	3.7	5.5	1.8	6.2	1.8	6.2	ns
t _{PLZ}			3.3	5.1	7.2	3.3	8.8	3.3	8.3	
t _{PZH}	$\overline{\text{OE}}$	B	3.4	5.7	7.9	3.4	8.9	3.4	8.9	ns
t _{PZL}			4.3	6.6	8.7	4.3	9.9	4.3	9.7	
t _{PHZ}	$\overline{\text{OE}}$	B	2.7	4.5	6.3	2.7	6.9	2.7	6.9	ns
t _{PLZ}			1.7	4.5	6.8	1.7	7.7	1.7	7.5	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.