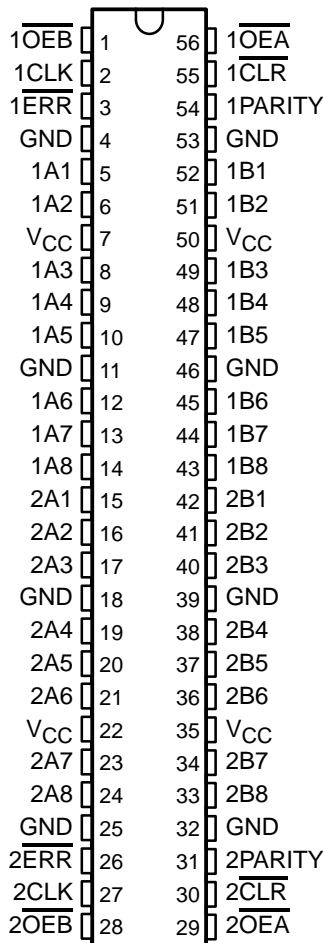


# SN54ABT16833, SN74ABT16833 DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

SCBS097C – FEBRUARY 1991 – REVISED JULY 1994

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 1$  V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )
- Parity Error Flag With Parity Generator/Checker
- Register for Storage of the Parity Error Flag
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54ABT16833 . . . WD PACKAGE  
SN74ABT16833 . . . DL PACKAGE  
(TOP VIEW)



## description

The 'ABT16833 consists of two noninverting 8-bit to 9-bit parity bus transceivers and is designed for communication between data buses. For each transceiver, when data is transmitted from the A bus to the B bus, an odd-parity bit is generated and output on the parity I/O pin (1PARITY or 2PARITY). When data is transmitted from the B bus to the A bus, 1PARITY (or 2PARITY) is configured as an input and combined with the B-input data to generate an active-low error flag if odd parity is not detected.

The error ( $\overline{1ERR}$  or  $\overline{2ERR}$ ) output is configured as an open-collector output. The B-to-A parity error flag is clocked into  $\overline{1ERR}$  (or  $\overline{2ERR}$ ) on the low-to-high transition of the clock (1CLK or 2CLK) input.  $\overline{1ERR}$  (or  $\overline{2ERR}$ ) is cleared (set high) by taking the clear ( $\overline{1CLR}$  or  $\overline{2CLR}$ ) input low.

The output-enable ( $\overline{OE_A}$  and  $\overline{OE_B}$ ) inputs can be used to disable the device so that the buses are effectively isolated. When both  $\overline{OE_A}$  and  $\overline{OE_B}$  are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16833 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16833 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT16833 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

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DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

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FUNCTION TABLE

INPUTS						OUTPUT AND I/O				FUNCTION
$\overline{\text{OEB}}$	$\overline{\text{OEA}}$	$\overline{\text{CLR}}$	CLK	Ai $\Sigma$ OF H's	Bi† $\Sigma$ OF H's	A	B	PARITY	$\overline{\text{ERR}}\ddagger$	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and generate parity
H	L	H	$\uparrow$	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
X	X	L	X	X	X	X	NA	NA	H	Check error flag register
H	H	H	No $\uparrow$	X		Z	Z	Z	NC	
		L	No $\uparrow$	X					H	
		H	$\uparrow$	O d	X d				H	
		H	$\uparrow$	E v	e n				L	
L	L	X	X	O d E v	d e n	A N	<b>A</b>	H L	N	A g e n e r a t e r e r

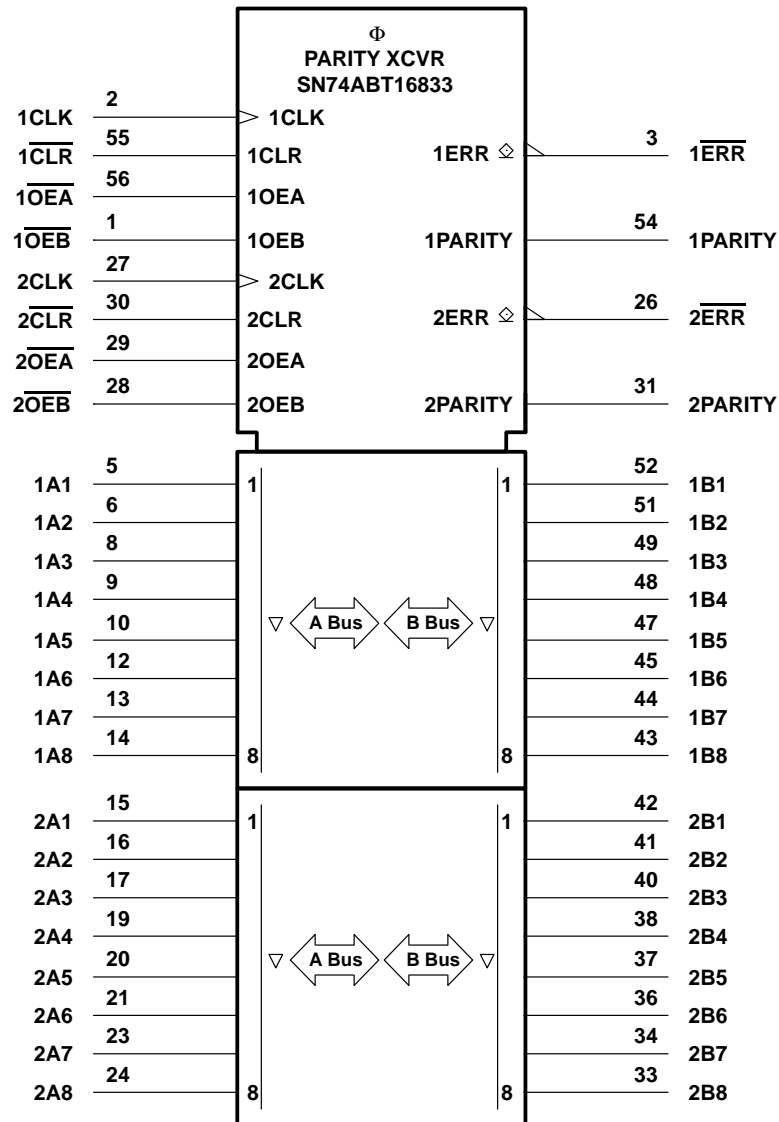
†S u m m a t o r i o n a p p l i c a b l e  
‡O u t p u t o u s t t p a u t t e s w a s s h o p w r r  
§I n t o h u i t s p u m t o d ( e w , h e t n h e c l E



# SN54ABT16833, SN74ABT16833 DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

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logic symbol†

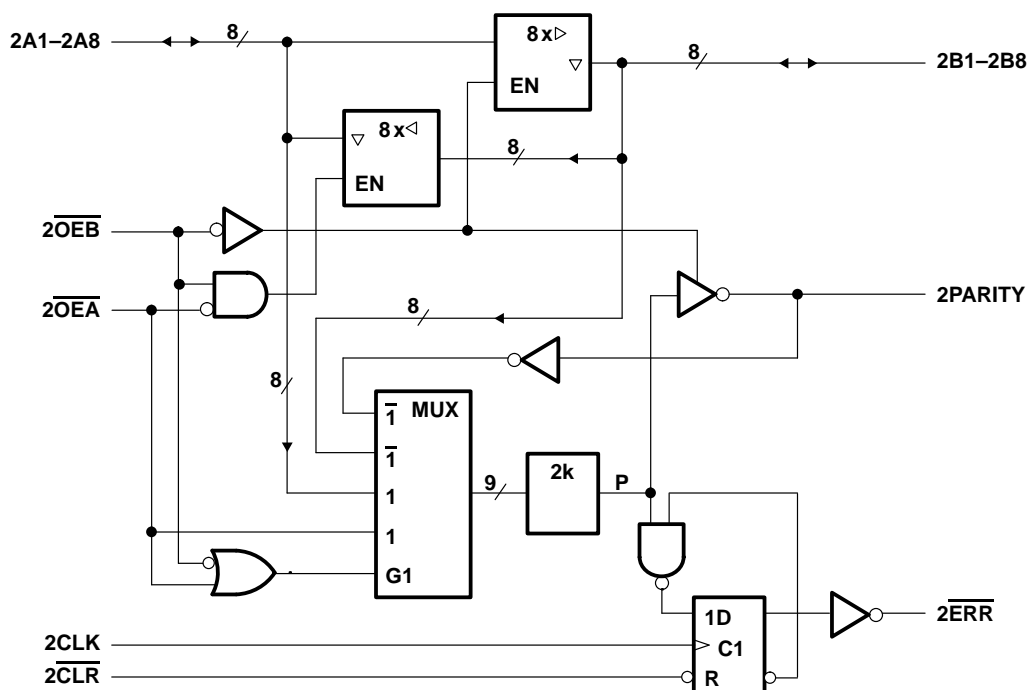
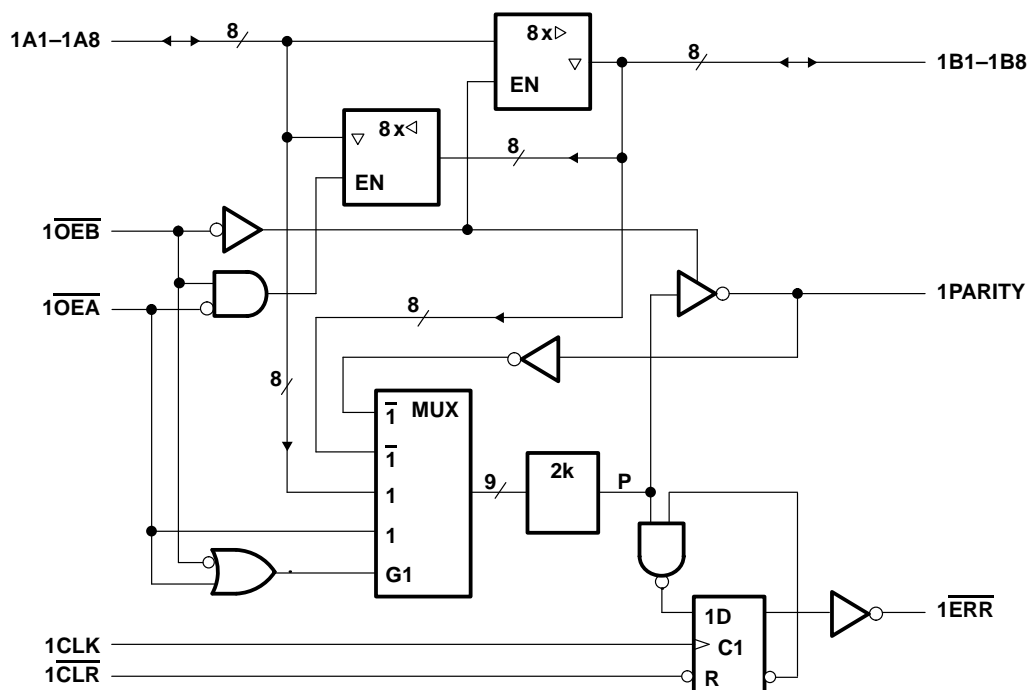


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# SN54ABT16833, SN74ABT16833 DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

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## logic diagram (positive logic)

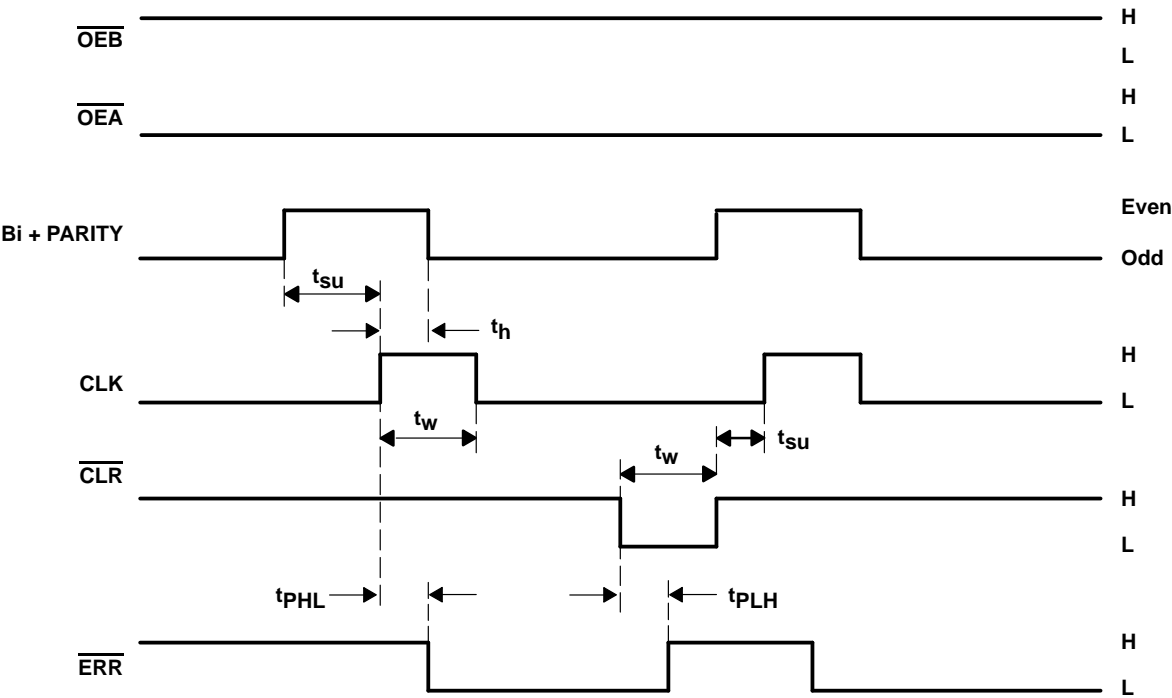


ERROR-FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT ERR	FUNCTION
CLR	CLK	POINT P	ERR <sub>n-1</sub>		
H	↑	H	H	H	Sample
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	Clear

† The state of the ERR output before any changes at CLR, CLK, or point P.

error-flag waveforms



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## DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$	–0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT16833	96 mA
SN74ABT16833	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DL package	1.4 W
Storage temperature range	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.  
For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

### recommended operating conditions (see Note 3)

		SN54ABT16833		SN74ABT16833		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$V_{OH}$	High-level output voltage		ERR		5.5	V
$I_{OH}$	High-level output current		Except ERR		–32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

# SN54ABT16833, SN74ABT16833

## DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABT16833		SN74ABT16833		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	V
V <sub>OH</sub>	All outputs except $\overline{\text{ERR}}$	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA	2.5	3		2.5				V
		V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA	3	3.4		3		3		
		V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -24 mA			2				
			I <sub>OH</sub> = -32 mA		2*	2.7		2		
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 24 mA		0.25	0.55				V
			I <sub>OL</sub> = 64 mA		0.3	0.55*			0.55	
I <sub>OH</sub>	$\overline{\text{ERR}}$	V <sub>CC</sub> = 4.5 V, V <sub>OH</sub> = 5.5 V			20	20		20		μA
I <sub>off</sub>		V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100			±100		μA
I <sub>CEX</sub>	Outputs high	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V			50	50		50		μA
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND			±1	±1		±1		μA
	A or B ports				±100	±100		±100		
I <sub>IL</sub>	A or B ports	V <sub>CC</sub> = 0, V <sub>I</sub> = GND			-50	-50		-50		μA
I <sub>O†</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V	-50	-100	-180	-50	-180	-50	-180	mA
I <sub>OZH</sub> §		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V			50	50		50		μA
I <sub>OZL</sub> §		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V			-50	-50		-50		μA
I <sub>CC</sub>	A or B ports	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high		1.5	2	2	2		mA
			Outputs low		28	36	36	36		
			Outputs disabled		1	2	2	2		
ΔI <sub>CC</sub> ¶		V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			50	50		50		μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 2.5 V or 0.5 V			3					pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = 2.5 V or 0.5 V			9					pF

\* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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## DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$		SN54ABT16833		SN74ABT16833		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	CLK high or low	3		3		3		ns
$t_{su}$	Setup time before CLK $\uparrow$	A port	4.5		4.5		4.5		ns
		$\overline{\text{CLR}}$	1		1		1		
		$\overline{\text{OEA}}$	5		5		5		
$t_h$	Hold time after CLK $\uparrow$	A port or $\overline{\text{OEA}}$	0		0		0		ns

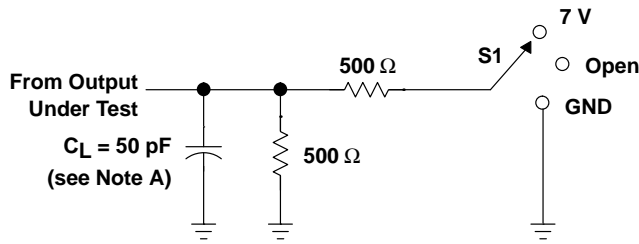
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$			SN54ABT16833		SN74ABT16833		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	1.5	2.5	3.3	1.5	4.2	1.5	4.1	ns
$t_{PHL}$			2	3.1	3.9	2	4.5	2	4.3	
$t_{PZH}$	$\overline{\text{OE}}$	A or B	2	3.9	4.9	2	5.8	2	5.6	ns
$t_{PZL}$			2.5	4.3	5.1	2.5	6.2	2.5	6	
$t_{PHZ}$	$\overline{\text{OE}}$	A or B	2	3.6	4.5	2	5.5	2	5.4	ns
$t_{PLZ}$			1.5	3	3.8	1.5	4.7	1.5	4.3	
$t_{PLH}$	A or $\overline{\text{OE}}$	PARITY	2	4.6	5.4	2	7	2	6.7	ns
$t_{PHL}$			2	4.3	5.1	2	6.5	2	6.1	
$t_{PZH}$	$\overline{\text{OE}}$	PARITY	2	3.6	5	2	5.8	2	5.7	ns
$t_{PZL}$			2.5	4.4	5.8	2.5	6.7	2.5	6.5	
$t_{PHZ}$	$\overline{\text{OE}}$	PARITY	1.5	3.2	4	1.5	4.8	1.5	4.7	ns
$t_{PLZ}$			1.5	2.9	3.7	1.5	4.2	1.5	4.1	
$t_{PLH}$	CLK, $\overline{\text{CLR}}$	$\overline{\text{ERR}}$	2	3.4	4.2	2	4.8	2	4.6	ns
$t_{PHL}$	CLK		2	2.8	3.6	2	4.1	2	3.9	

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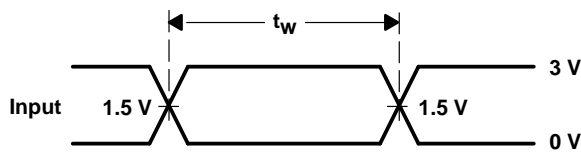
## PARAMETER MEASUREMENT INFORMATION



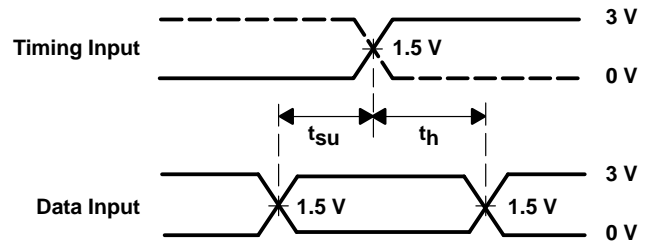
LOAD CIRCUIT FOR OUTPUTS

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open

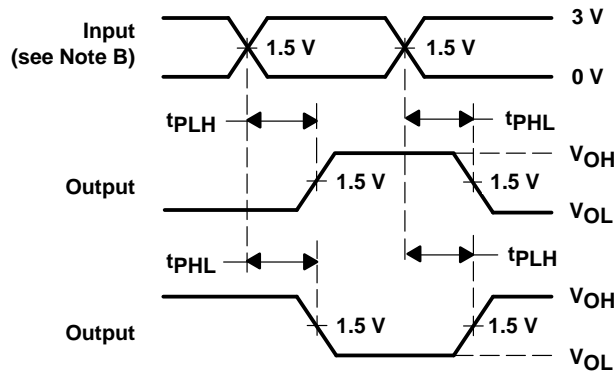
$\overline{ERR}$	S1
$t_{PHL}$ (see Note E)	7 V
$t_{PLH}$ (see Note F)	7 V



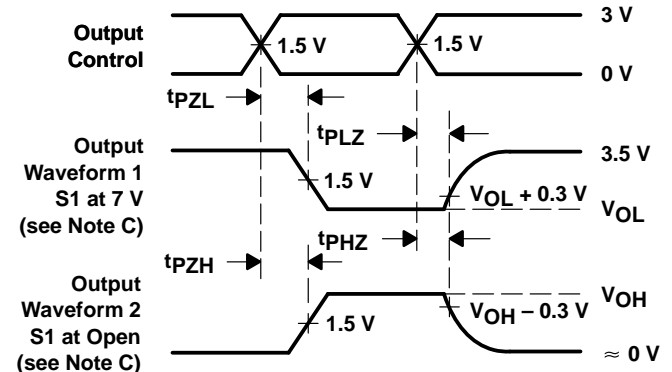
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

NOTES: A.  $C_L$  includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one transition per measurement.

E.  $t_{PHL}$  is measured at 1.5 V.

F.  $t_{PLH}$  is measured at  $V_{OL} + 0.3$  V.

Figure 1. Load Circuit and Voltage Waveforms



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