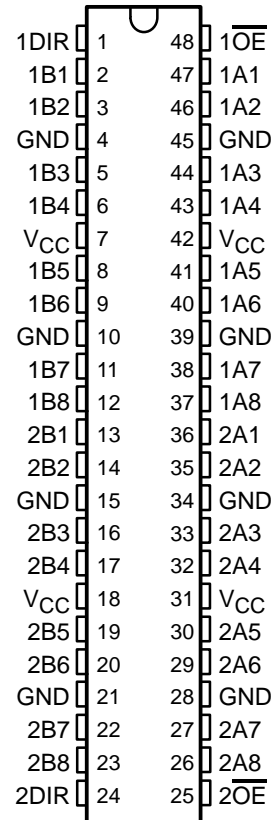


SN54ABT16640, SN74ABT16640 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS107B – APRIL 1992 – REVISED JULY 1994

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54ABT16640 . . . WD PACKAGE
SN74ABT16640 . . . DL PACKAGE
(TOP VIEW)



description

The 'ABT16640 are inverting 16-bit transceivers designed for asynchronous communication between data buses.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (1DIR and 2DIR) inputs. The output-enable ($1\overline{OE}$ and $2\overline{OE}$) inputs can be used to disable the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16640 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16640 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT16640 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	\overline{B} data to A bus
L	H	\overline{A} data to B bus
H	X	Isolation

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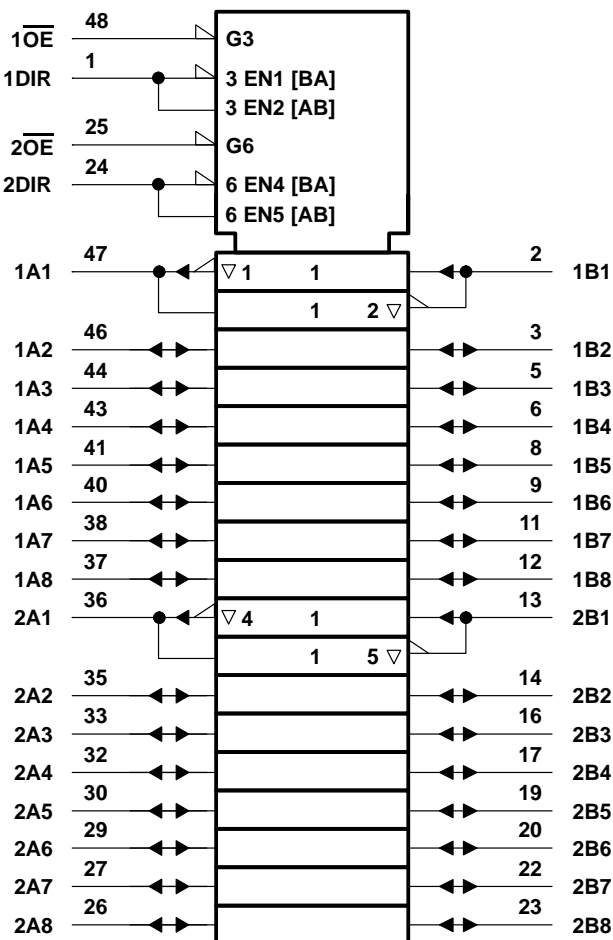
 **TEXAS
INSTRUMENTS**

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logic diagram (positive logic)

[illegible]

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	−0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT16640	96 mA
SN74ABT16640	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	−18 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DL package	1.2 W
Storage temperature range	−65°C to 150°C

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

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recommended operating conditions (see Note 3)

			SN54ABT16640		SN74ABT16640		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			-24		-32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		-55	125	-40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54ABT16640		SN74ABT16640		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}		$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2		-1.2		-1.2	V
V_{OH}		$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$	2.5			2.5		2.5		V
		$V_{CC} = 5\text{ V}$, $I_{OH} = -3\text{ mA}$	3			3		3		
		$V_{CC} = 4.5\text{ V}$, $I_{OH} = -24\text{ mA}$	2			2				
		$V_{CC} = 4.5\text{ V}$, $I_{OH} = -32\text{ mA}$	2*					2		
V_{OL}		$V_{CC} = 4.5\text{ V}$, $I_{OL} = 48\text{ mA}$			0.55		0.55			V
		$V_{CC} = 4.5\text{ V}$, $I_{OL} = 64\text{ mA}$			0.55*				0.55	
I_I	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}$ or GND			± 1		± 1		± 1	μA
	A or B ports	$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}$ or GND			± 100		± 100		± 100	
I_{OZH}^\ddagger		$V_{CC} = 5.5\text{ V}$, $V_O = 2.7\text{ V}$			50		50		50	μA
I_{OZL}^\ddagger		$V_{CC} = 5.5\text{ V}$, $V_O = 0.5\text{ V}$			-50		-50		-50	μA
I_{off}		$V_{CC} = 0$, V_I or $V_O \leq 4.5\text{ V}$			± 100				± 100	μA
I_{CEX}	Outputs high	$V_{CC} = 5.5\text{ V}$, $V_O = 5.5\text{ V}$			50		50		50	μA
I_O^\S		$V_{CC} = 5.5\text{ V}$, $V_O = 2.5\text{ V}$	-50	-100	-180	-50	-180	-50	-180	mA
I_{CC}	A or B ports	$V_{CC} = 5.5\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND			2		2		2	mA
		Outputs low			32		32		32	
		Outputs disabled			2		2		2	
ΔI_{CC}^\P	Data inputs	$V_{CC} = 5.5\text{ V}$, One input at 3.4 V, Other inputs at V_{CC} or GND			1		1.5		1	mA
		Outputs enabled								
	Control inputs	$V_{CC} = 5.5\text{ V}$, One input at 3.4 V, Other inputs at V_{CC} or GND			1.5		1.5		1.5	
C_i	Control inputs	$V_I = 2.5\text{ V}$ or 0.5 V			3					pF
C_{io}	A or B ports	$V_O = 2.5\text{ V}$ or 0.5 V			8					pF

* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

† All typical values are at $V_{CC} = 5\text{ V}$.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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16-BIT BUS TRANSCEIVERS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

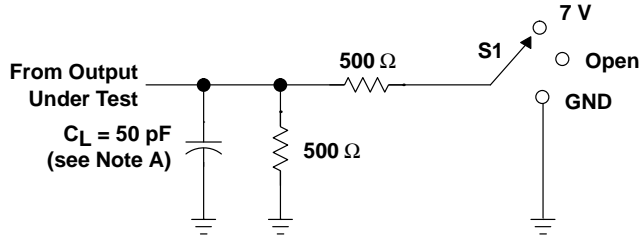
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			SN54ABT16640		SN74ABT16640		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	2.5	3.4	1	4.4	1	4.3	ns
t_{PHL}			1.1	2.8	3.6	1.1	4	1.1	3.9	
t_{PZH}	\overline{OE}	A or B	1.2	3.5	4.5	1.2	5.6	1.2	5.5	ns
t_{PZL}			1.5	3.9	5	1.5	6.4	1.5	6.3	
t_{PHZ}	\overline{OE}	A or B	1.8	3.8	4.8	1.8	6.5	1.8	6.3	ns
t_{PLZ}			1.5	3	3.9	1.5	4.4	1.5	4.2	

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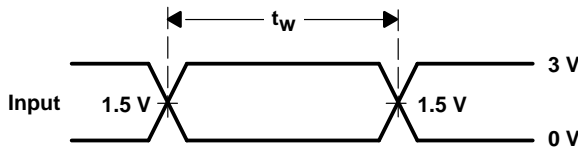
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PARAMETER MEASUREMENT INFORMATION

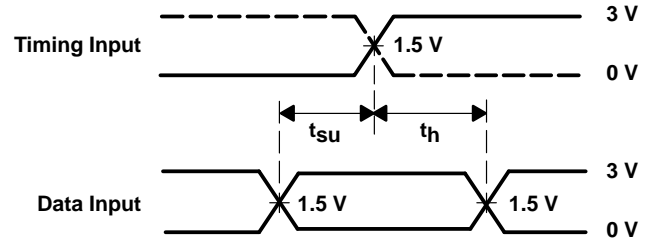


LOAD CIRCUIT FOR OUTPUTS

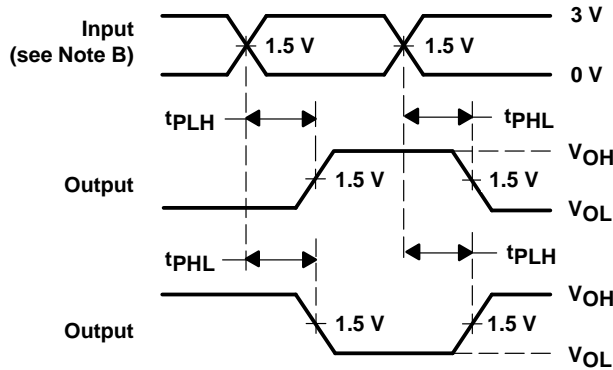
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



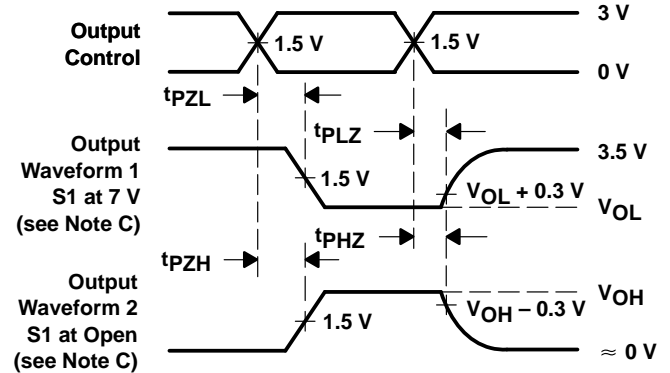
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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