

# SN54ABT620, SN74ABT620 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS113B – FEBRUARY 1991 – REVISED JULY 1994

- State-of-the-Art *EPIC-II<sup>TM</sup>* BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Drive Outputs (–32-mA  $I_{OH}$ , 64-mA  $I_{OL}$ )
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK), and Plastic (N) and Ceramic (J) DIPs

## description

These octal bus transceivers are designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing. The 'ABT620 provides inverted data at its outputs.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable (OEAB and  $\overline{\text{OEBA}}$ ) inputs.

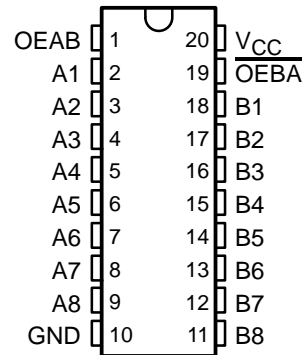
The output-enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability of storing data by simultaneously enabling OEAB and  $\overline{\text{OEBA}}$ . When both OEAB and  $\overline{\text{OEBA}}$  are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. In this way, each output reinforces its input in this configuration.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OEBA}}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

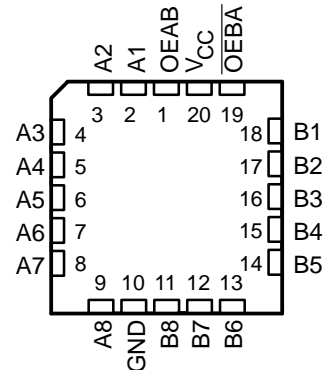
The SN74ABT620 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT620 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT620 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54ABT620 . . . J PACKAGE  
SN74ABT620 . . . DB, DW, OR N PACKAGE  
(TOP VIEW)



SN54ABT620 . . . FK PACKAGE  
(TOP VIEW)



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 **TEXAS  
INSTRUMENTS**

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# SN54ABT620, SN74ABT620

## OCTAL BUS TRANSCEIVERS

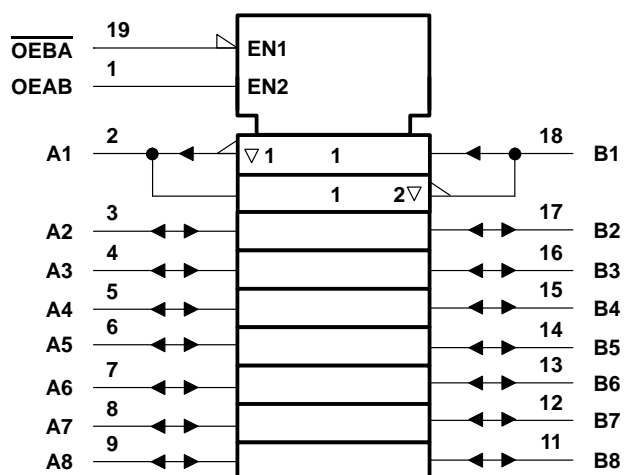
### WITH 3-STATE OUTPUTS

SCBS113B – FEBRUARY 1991 – REVISED JULY 1994

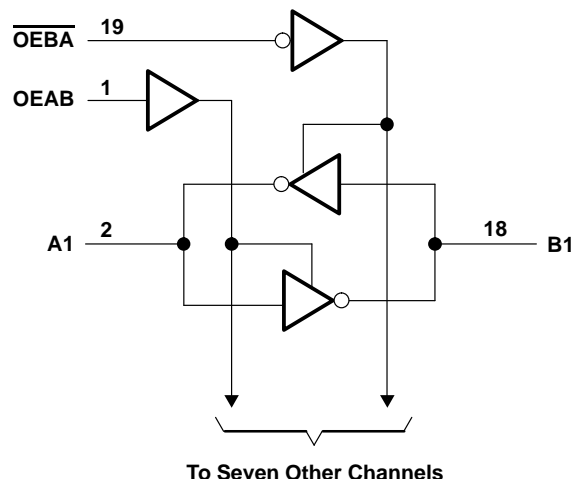
FUNCTION TABLE

INPUTS		OPERATION
OEBA	OEAB	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus
H	L	Isolation
H	H	$\overline{A}$ data to B bus

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$	–0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT620	96 mA
SN74ABT620	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DB package	0.6 W
DW package	1.6 W
N package	1.3 W
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

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SCBS113B – FEBRUARY 1991 – REVISED JULY 1994

## recommended operating conditions (see Note 3)

			SN54ABT620		SN74ABT620		UNIT
			MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage		4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage		2		2		V
$V_{IL}$	Low-level input voltage			0.8		0.8	V
$V_I$	Input voltage		0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current			–24		–32	mA
$I_{OL}$	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
$T_A$	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54ABT620		SN74ABT620		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			–1.2		–1.2		–1.2	V
$V_{OH}$		$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -3\text{ mA}$	2.5			2.5		2.5		V
		$V_{CC} = 5\text{ V}$ , $I_{OH} = -3\text{ mA}$	3			3		3		
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -24\text{ mA}$	2			2				
		$I_{OH} = -32\text{ mA}$	2*					2		
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$			0.55		0.55			V
		$I_{OL} = 64\text{ mA}$			0.55*				0.55	
$I_I$	Control inputs	$V_{CC} = 5.5\text{ V}$ , $V_I = V_{CC}$ or GND			$\pm 1$		$\pm 1$		$\pm 1$	$\mu\text{A}$
	A or B ports				$\pm 100$		$\pm 100$		$\pm 100$	
$I_{OZH}^\ddagger$		$V_{CC} = 5.5\text{ V}$ , $V_O = 2.7\text{ V}$			50		50		50	$\mu\text{A}$
$I_{OZL}^\ddagger$		$V_{CC} = 5.5\text{ V}$ , $V_O = 0.5\text{ V}$			–50		–50		–50	$\mu\text{A}$
$I_{off}$		$V_{CC} = 0$ , $V_I$ or $V_O \leq 4.5\text{ V}$			$\pm 100$				$\pm 100$	$\mu\text{A}$
$I_{CEX}$		$V_{CC} = 5.5\text{ V}$ , $V_O = 5.5\text{ V}$ Outputs high			50		50		50	$\mu\text{A}$
$I_O^\S$		$V_{CC} = 5.5\text{ V}$ , $V_O = 2.5\text{ V}$	–50	–100	–180	–50	–180	–50	–180	mA
$I_{CC}$	A or B ports	$V_{CC} = 5.5\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}$ or GND	Outputs high		5	250		250		$\mu\text{A}$
			Outputs low		24	30		30		mA
			Outputs disabled		0.5	250		250		$\mu\text{A}$
$\Delta I_{CC}^\P$	Data inputs	$V_{CC} = 5.5\text{ V}$ , One input at 3.4 V, Other inputs at $V_{CC}$ or GND	Outputs enabled		1.5		1.5		1.5	mA
			Outputs disabled		0.05		0.05		0.05	
	Control inputs	$V_{CC} = 5.5\text{ V}$ , One input at 3.4 V, Other inputs at $V_{CC}$ or GND			1.5		1.5		1.5	
$C_i$	Control inputs	$V_I = 2.5\text{ V}$ or $0.5\text{ V}$			4					pF
$C_{io}$	A or B ports	$V_O = 2.5\text{ V}$ or $0.5\text{ V}$			7					pF

\* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

† All typical values are at  $V_{CC} = 5\text{ V}$ .

‡ The parameters  $I_{OZH}$  and  $I_{OZL}$  include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

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## OCTAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SCBS113B – FEBRUARY 1991 – REVISED JULY 1994

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

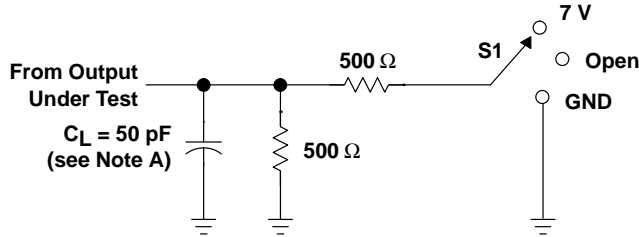
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$		SN54ABT620		SN74ABT620		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	1	4.1	1		1	4.8	ns
$t_{PHL}$			1	4.3	1		1	4.8	
$t_{PZH}$	$\overline{OEBA}$	A	1.3	4.6	1.3		1.3	5.5	ns
$t_{PZL}$			1	6.1	1		1	7.1	
$t_{PHZ}$	$\overline{OEBA}$	A	2	6.3	2		2	7	ns
$t_{PLZ}$			1.4	5.4	1.4		1.4	5.8	
$t_{PZH}$	OEAB	B	1.6	6.2	1.6		1.6	6.8	ns
$t_{PZL}$			2	5.9	2		2	6.4	
$t_{PHZ}$	OEAB	B	1.2	5.6	1.2		1.2	6.5	ns
$t_{PLZ}$			1.1	4.7	1.1		1.1	5.6	

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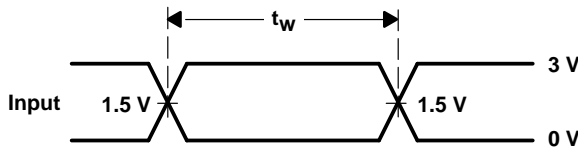
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## PARAMETER MEASUREMENT INFORMATION

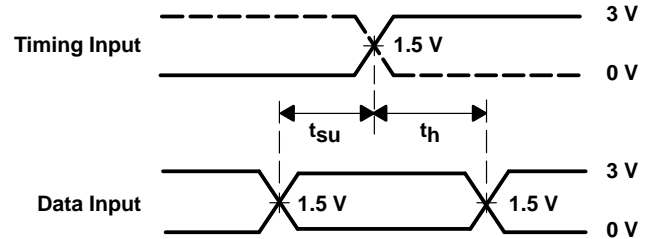


LOAD CIRCUIT FOR OUTPUTS

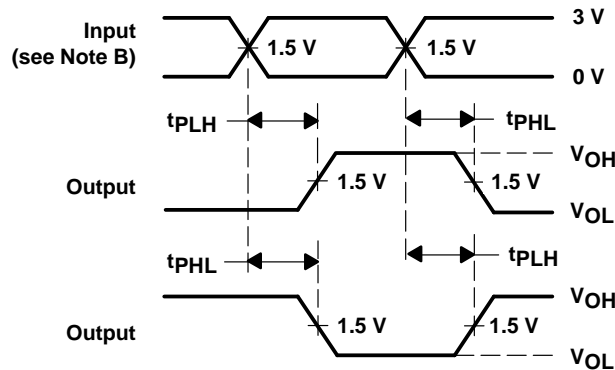
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



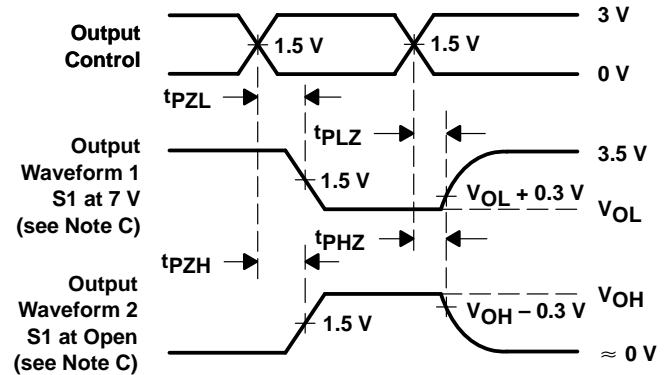
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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