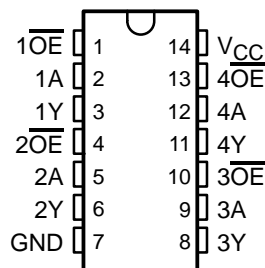


SN54LVT125, SN74LVT125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

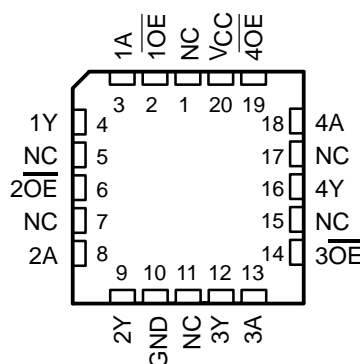
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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs

SN54LVT125 ... J PACKAGE
SN74LVT125 ... D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LVT125 ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These bus buffers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT125 feature independent line drivers with 3-state outputs. Each output is in the high-impedance state when the associated output-enable (\overline{OE}) input is high.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT125 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT125 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT125 is characterized for operation from -40°C to 85°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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SN54LVT125, SN74LVT125

3.3-V ABT QUADRUPLE BUS BUFFERS

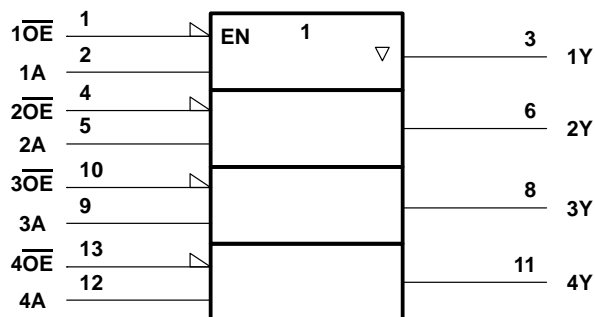
WITH 3-STATE OUTPUTS

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FUNCTION TABLE
(each buffer)

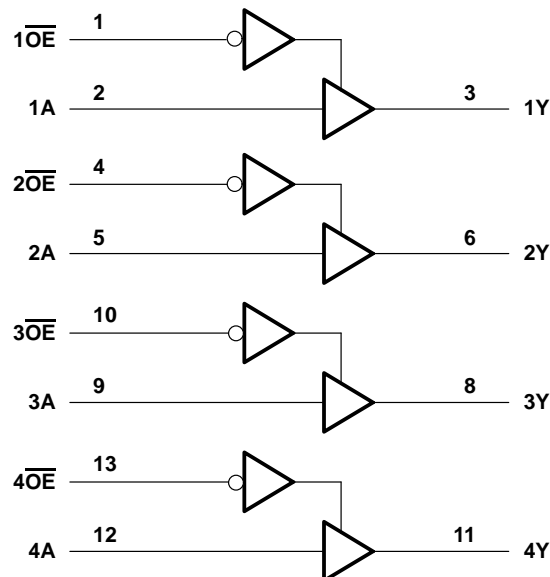
INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Current into any output in the low state, I_O : SN54LVT125	96 mA
SN74LVT125	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT125	48 mA
SN74LVT125	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): D package	1.25 W
DB or PW package	0.5 W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.



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recommended operating conditions (see Note 4)

		SN54LVT125		SN74LVT125		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT125			SN74LVT125			UNIT	
				MIN	TYP†	MAX	MIN	TYP†	MAX		
V _{IK}	V _{CC} = 2.7 V, I _I = −18 mA			−1.2			−1.2			V	
V _{OH}	V _{CC} = MIN to MAX‡, I _{OH} = −100 μA			V _{CC} −0.2			V _{CC} −0.2			V	
	V _{CC} = 2.7 V, I _{OH} = − 8 mA			2.4			2.4				
	V _{CC} = 3 V	I _{OH} = − 24 mA		2							
		I _{OH} = − 32 mA					2				
V _{OL}	V _{CC} = 2.7 V	I _{OL} = 100 μA		0.2			0.2			V	
		I _{OL} = 24 mA		0.5			0.5				
	V _{CC} = 3 V	I _{OL} = 16 mA		0.4			0.4				
		I _{OL} = 32 mA		0.5			0.5				
		I _{OL} = 48 mA		0.55							
		I _{OL} = 64 mA					0.55				
I _I	V _{CC} = 0 or MAX‡, V _I = 5.5 V			10			10			μA	
	V _{CC} = 3.6 V	V _I = V _{CC} or GND	Control inputs	±1			±1				
		V _I = V _{CC}	Data inputs	1			1				
		V _I = 0		−5			−5				
		I _{off}			V _{CC} = 0, V _I or V _O = 0 to 4.5 V			±100			μA
I _I (hold)	V _{CC} = 3 V	V _I = 0.8 V		Data inputs	75			75			μA
		V _I = 2 V			−75			−75			μA
I _{OZH}	V _{CC} = 3.6 V, V _O = 3 V			5			5			μA	
I _{OZL}	V _{CC} = 3.6 V, V _O = 0.5 V			−5			−5			μA	
I _{CC}	V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND		Outputs high	0.12	0.19	0.12		0.19		mA	
			Outputs low	4.5	7	4.5		7			
			Outputs disabled	0.12	0.19	0.12		0.19			
ΔI _{CC} §	V _{CC} = 3 V to 3.6 V, One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND			0.3			0.2			mA	
C _i	V _I = 3 V or 0			4			4			pF	
C _O	V _O = 3 V or 0			8			8			pF	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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SN54LVT125, SN74LVT125

3.3-V ABT QUADRUPLE BUS BUFFERS

WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

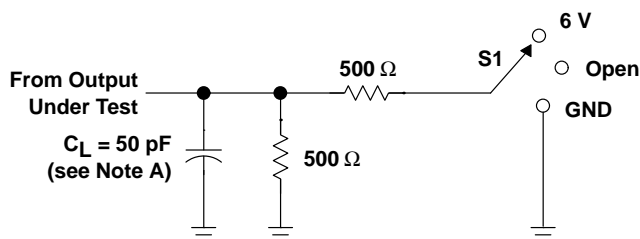
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT125				SN74LVT125				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t _{PLH}	A	Y	1	4.2		4.7	1	2.7	4		4.5	ns
t _{PHL}			1	4.1		5.1	1	2.9	3.9		4.9	
t _{PZH}	$\overline{\text{OE}}$	Y	1	4.9		6.2	1	3.4	4.7		6	ns
t _{PZL}			1.1	4.9		6.7	1.1	3.4	4.7		6.5	
t _{PHZ}	$\overline{\text{OE}}$	Y	1.8	5.3		5.9	1.8	3.7	5.1		5.7	ns
t _{PLZ}			1.3	4.7		4.2	1.3	2.6	4.5		4	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

SN54LVT125, SN74LVT125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

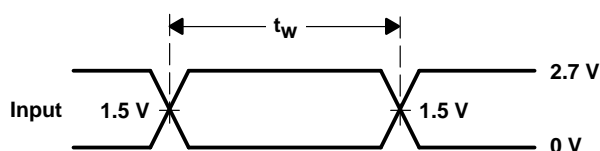
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PARAMETER MEASUREMENT INFORMATION

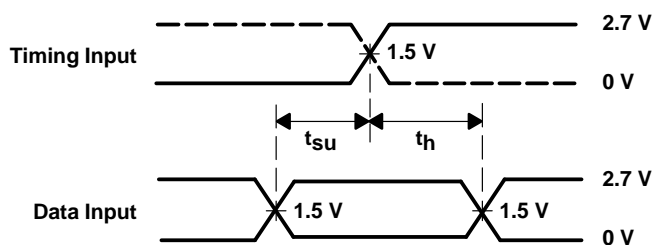


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

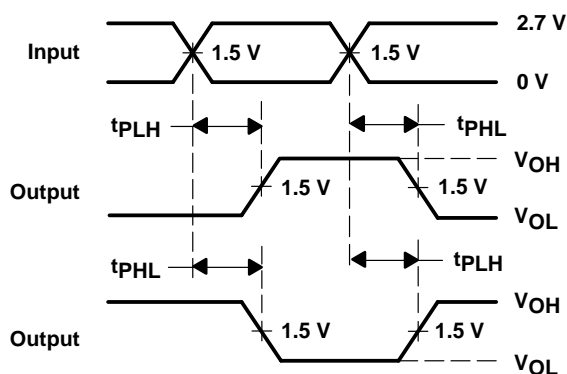
LOAD CIRCUIT FOR OUTPUTS



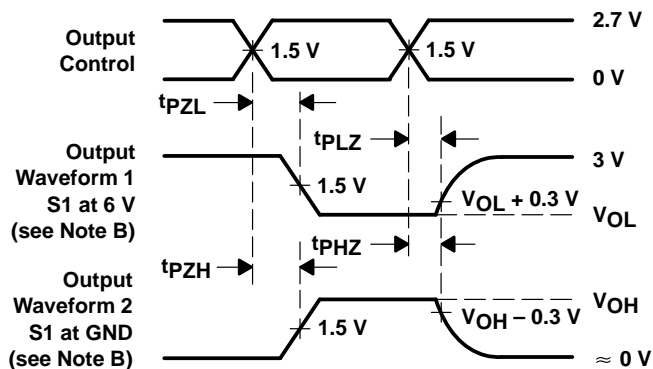
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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