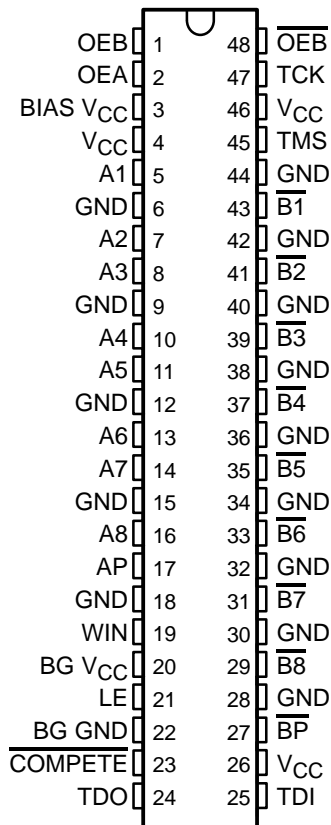


# SN54FB2032, SN74FB2032 9-BIT TTL/BTL COMPETITION TRANSCEIVERS

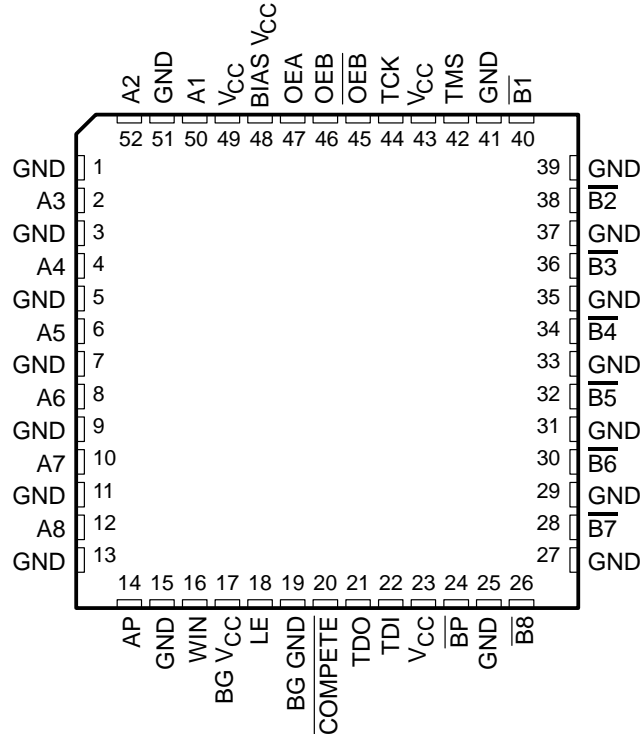
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- Compatible With IEEE 1194.1-1991 (BTL) Standard
- TTL A Port, Backplane Transceiver Logic (BTL)  $\bar{B}$  Port
- Open-Collector  $\bar{B}$ -Port Outputs Sink 100 mA
- BIAS  $V_{CC}$  Pin Minimizes Signal Distortion During Live Insertion or Withdrawal
- $\bar{B}$ -Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage
- TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination
- Package Options Include Plastic Quad Flat (RC) Package and Ceramic Flat (WD) Package

SN54FB2032 . . . WD PACKAGE  
(TOP VIEW)



SN74FB2032 . . . RC PACKAGE  
(TOP VIEW)



## description

The 'FB2032 are 9-bit transceivers designed to translate signals between TTL and backplane transceiver logic (BTL) environments and to perform bus arbitration. They are specifically designed to be compatible with IEEE 1194.1-1991 (BTL) standard.

The  $\bar{B}$  port operates at BTL-signal levels. The open-collector  $\bar{B}$  ports are specified to sink 100 mA and have minimum output edge rates of 2 ns. Two output enables, OEB and  $\bar{OEB}$ , are provided for the  $\bar{B}$  outputs. When OEB is low,  $\bar{OEB}$  is high, or  $V_{CC}$  is less than 2.1 V, the  $\bar{B}$  port is turned off.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
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# SN54FB2032, SN74FB2032

## 9-BIT TTL/BTL COMPETITION TRANSCEIVERS

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### description (continued)

The A port operates at TTL-signal levels. The A outputs reflect the inverse of the data at the  $\bar{B}$  port when the A-port output enable, OEA, is high. When OEA is low or when  $V_{CC}$  is less than 2.1 V, the A outputs are in the high-impedance state.

The A-port data is latched when the latch enable (LE) is high. When LE is low, the latches are transparent.

The Futurebus+ protocol logic can be activated by taking  $\overline{COMPETE}$  low. The module (device) then compares its A data (arbitration number) against the A data of another identical module also connected to the  $\bar{B}$  arbitration bus, and sets WIN high if the A data is greater than the A data of the other module (i.e., has higher priority). A8 and  $\bar{B}8$  are the most significant bits, and A1 and  $\bar{B}1$  are the least significant bits. If OEB is high and  $\bar{OEB}$  is low during this operation, and the A bus of the first module wins priority, the A bus asserts its arbitration number on the  $\bar{B}$ -arbitration bus.

AP and  $\bar{BP}$  are the bus-parity bits. The winning module can assert  $\bar{BP}$  low if its parity bit (AP) is high.

In a typical operating sequence, a Futurebus+ arbitration controller latches its arbitration number into the A port and waits for the results of a competition. When the competition is complete, and if the controller's arbitration number did not win, the controller reads back the current value of the  $\bar{B}$  bus (by taking OEA high) and determines the winning arbitration number. This allows the module to change its arbitration number for the next competition cycle, if desired.

Pins are allocated for the four-wire IEEE 1149.1 (JTAG) test bus, which will be implemented in a future version of the 'FB2032. Currently, TMS and TCK are not connected and TDI is shorted to TDO.

BIAS  $V_{CC}$  establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when  $V_{CC}$  is not connected.

BG  $V_{CC}$  and BG GND are the supply inputs for the bias generator.

The SN54FB2032 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74FB2032 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .



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## Function Tables

### TRANSCEIVER

INPUTS			FUNCTION
OEA	OEB	$\overline{\text{OEB}}$	
L	H	L	$\overline{\text{A}}$ data to B bus
H	L	X	$\overline{\text{B}}$ data to A bus
H	X	H	$\overline{\text{B}}$ data to A bus
H	H	L	$\overline{\text{A}}$ data to B bus, $\overline{\text{B}}$ data to A bus
L	L	X	Isolation
L	X	H	

### WIN

INPUTS				WIN
OEB	$\overline{\text{OEB}}$	$\overline{\text{COMPETE}}$	DATA A1, A2†	
H	H	X	X	L
H	L	H	X	L
H	L	L	A1 < A2	L
H	L	L	A2 ≤ A1	H

† A1 refers to the A data of Module 1 and A2 refers to the A data of Module 2. If LE=L, A=current A data. If LE=H, A=the value of A8–A1 prior to the most recent low-to-high transition of LE.

### $\overline{\text{BP}}$

INPUTS				$\overline{\text{BP}}$
OEB	$\overline{\text{OEB}}$	WIN	AP‡	
L	X	X	X	H
X	H	X	X	H
H	L	L	X	H
H	L	H	L	H
H	L	H	H	L

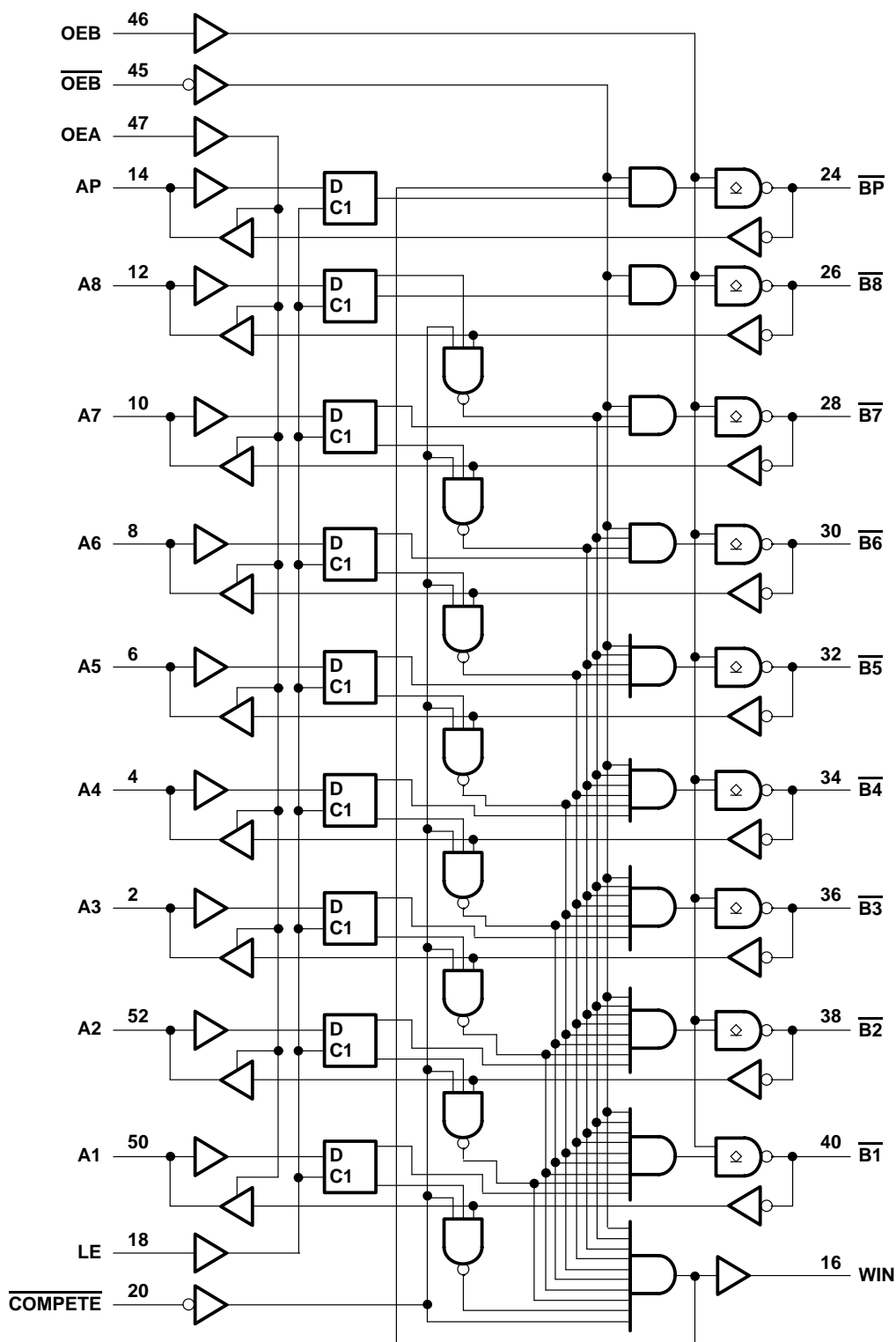
‡ If LE=L, AP=current AP data. If LE=H, AP=the level of AP prior to the most recent low-to-high transition of LE.

# SN54FB2032, SN74FB2032

## 9-BIT TTL/BTL COMPETITION TRANSCEIVERS

SCBS175D – NOVEMBER 1991 – REVISED AUGUST 1996

## functional block diagram



Pin numbers shown are for the RC package.

# SN54FB2032, SN74FB2032

## 9-BIT TTL/BTL COMPETITION TRANSCEIVERS

SCBS175D – NOVEMBER 1991 – REVISED AUGUST 1996

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state, $V_O$	–0.5 V to 3.5 V
Voltage range applied to any output in the high state, $V_O$	–0.5 V to $V_{CC}$
Input voltage range, $V_I$ : Except $\overline{BP}$ , $\overline{B}$ port	–1.2 V to 7 V
$\overline{BP}$ , $\overline{B}$ port	–1.2 V to 3.5 V
Input clamp current, $I_{IK}$ : Except $\overline{B}$ port	–40 mA
$\overline{B}$ port	–18 mA
Current applied to any single output in the low state, $I_O$ : A port	48 mA
$\overline{B}$ port	200 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 1): RC package	1.4 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils.

### recommended operating conditions (see Note 2)

		SN54FB2032			SN74FB2032			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ , BIAS $V_{CC}$ , BG $V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	$\overline{BP}$ , $\overline{B}$ port*		2.3	$\overline{BP}$ , $\overline{B}$ port*		2.3	V
		Except $\overline{B}$ port		2	Except $\overline{B}$ port		2	
$V_{IL}$	Low-level input voltage	$\overline{BP}$ , $\overline{B}$ port*		1.47	$\overline{BP}$ , $\overline{B}$ port*		1.47	V
		Except $\overline{B}$ port		0.8	Except $\overline{B}$ port		0.8	
$I_{IK}$	Input clamp current	–18			–18			mA
$I_{OH}$	High-level output current	AP, WIN, A port		–3	AP, WIN, A port		–3	mA
$I_{OL}$	Low-level output current	AP, WIN, A port		24	AP, WIN, A port		24	mA
		$\overline{BP}$ , $\overline{B}$ port		100	$\overline{BP}$ , $\overline{B}$ port		100	
$T_A$	Operating free-air temperature	–55		125	0		70	°C

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

NOTE 2: Unused pins (input or I/O) must be held high or low to prevent them from floating.



# SN54FB2032, SN74FB2032

## 9-BIT TTL/BTL COMPETITION TRANSCEIVERS

SCBS175D – NOVEMBER 1991 – REVISED AUGUST 1996

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		SN54FB2032			SN74FB2032			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$\overline{BP}$ , $\overline{B}$ port	$V_{CC} = 4.5\text{ V}$	$I_I = -18\text{ mA}$			-1.2			-1.2	V
	Except $\overline{BP}$ , $\overline{B}$ port		$I_I = -40\text{ mA}$			-0.5			-0.5	
$V_{OH}$	AP, WIN, A port	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -1\text{ mA}$			3.2				V
			$I_{OH} = -3\text{ mA}$	2.5	3.3		2.5	3.3		
$V_{OL}$	AP, WIN, A port	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 20\text{ mA}$			0.31				V
			$I_{OL} = 24\text{ mA}$			0.35	0.55		0.35	
	$\overline{BP}$ , $\overline{B}$ port	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 80\text{ mA}$	0.75		1.15	0.75		1.1	
			$I_{OL} = 100\text{ mA}$						1.15	
$I_I$	Except $\overline{BP}$ , $\overline{B}$ port	$V_{CC} = 5.5\text{ V}$ , $V_I = 5.5\text{ V}$				50			50	$\mu\text{A}$
$I_{IH}^\ddagger$	Except $\overline{BP}$ , $\overline{B}$ port	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$				50			50	$\mu\text{A}$
$I_{IL}^\ddagger$	Except $\overline{BP}$ , $\overline{B}$ port	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.5\text{ V}$				-50			-50	$\mu\text{A}$
	$\overline{BP}$ , $\overline{B}$ port	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.75\text{ V}$				-100			-100	
$I_{OZH}$	AP, WIN, A port	$V_{CC} = 2.1\text{ V to } 5.5\text{ V}$ $V_O = 2.7\text{ V}$							50	mA
$I_{OZL}$	AP, WIN, A port	$V_{CC} = 2.1\text{ V to } 5.5\text{ V}$ $V_O = 0.5\text{ V}$							-50	mA
$I_{OZPU}$	AP, WIN, A port	$V_{CC} = 0\text{ V to } 2.1\text{ V}$ $V_O = 0.5\text{ V to } 2.7\text{ V}$							50	mA
$I_{OZPD}$	AP, WIN, A port	$V_{CC} = 2.1\text{ V to } 0\text{ V}$ $V_O = 0.5\text{ V to } 2.7\text{ V}$							-50	mA
$I_{OH}$	$\overline{BP}$ , $\overline{B}$ port	$V_{CC} = 0\text{ to } 5.5\text{ V}$ , $V_O = 2.1\text{ V}$				200			100	$\mu\text{A}$
$I_{OS}^\S$	AP, WIN, A port	$V_{CC} = 5.5\text{ V}$ , $V_O = 0$				-30	-150	-30	-150	mA
$I_{CC}$	A port to $\overline{B}$ port	$V_{CC} = 5.5\text{ V}$ , $I_O = 0$				65			55	mA
	$\overline{B}$ port to A port					70			65	
$C_i$	Control Inputs	$V_I = 0.5\text{ V or } 2.5\text{ V}$				4			4	pF
$C_o$	WIN port	$V_O = 0.5\text{ V or } 2.5\text{ V}$				8			8	pF
$C_{io}^\P$	A port	$V_O = 0.5\text{ V to } 2.5\text{ V}$				7			7	pF
	$\overline{B}$ port per P1194.0	$V_{CC} = 0\text{ V to } 5.5\text{ V}$							5	

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

¶ Parameter is based on characterization but is not production tested.



# SN54FB2032, SN74FB2032

## 9-BIT TTL/BTL COMPETITION TRANSCEIVERS

SCBS175D – NOVEMBER 1991 – REVISED AUGUST 1996

### live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		SN54FB2032		SN74FB2032		UNIT	
				MIN	MAX	MIN	MAX		
I <sub>CC</sub> (BIAS V <sub>CC</sub> )		V <sub>CC</sub> = 0 to 4.5 V	V <sub>B</sub> = 0 to 2 V,    V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V		450		450		μA
		V <sub>CC</sub> = 4.5 V to 5.5 V			10		10		
V <sub>O</sub> <sup>*</sup>	B̄ port	V <sub>CC</sub> = 0,                    V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 5 V		1.62	2.1	1.62	2.1	V	
I <sub>O</sub>	B̄ port	V <sub>CC</sub> = 0 ,                    V <sub>B</sub> = 1 V,                    V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V		−30		−1		μA	
		V <sub>CC</sub> = 0 to 5.5 V,        OEB = 0 to 0.8 V		140		100			
		V <sub>CC</sub> = 0 to 2.2 V,        OEB = 0 to 5 V		100		100			

\* For the SN54FB2032, this parameter is for  $T_A = 25^\circ C$  only.

### timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		SN54FB2032		SN74FB2032		UNIT		
		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C	MIN	MAX	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		MIN	MAX
t <sub>w</sub>	Pulse duration, LE high or low	4.1	4.1	3.3	3.3	ns		
t <sub>su</sub>	Setup time	Data high before LE↑ (A to B)	2.3	2.3	1.5	1.5	ns	
		Data low before LE↑	2.2	2.3	1.4	1.4		
		Data high before LE↑ (A to WIN)	2.7	2.7	1.9	1.9		
		Data low before LE↑	2.5	2.5	1.7	1.7		
t <sub>h</sub>	Hold time	Data high before LE↑ (A to B)	2.5	2.5	1.7	1.7	ns	
		Data low after LE↑	2.1	2.1	1.3	1.3		
		Data high before LE↑ (A to WIN)	2.4	2.5	1.6	1.6		
		Data low after LE↑	1.7	1.7	0.9	0.9		



# SN54FB2032, SN74FB2032

## 9-BIT TTL/BTL COMPETITION TRANSCEIVERS

SCBS175D – NOVEMBER 1991 – REVISED AUGUST 1996

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	SN54FB2032					UNIT
				V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t <sub>PLH</sub>		A or AP	$\overline{B}$ or $\overline{BP}$	2.2	5.2	7.3	1.1	8.3	ns
t <sub>PHL</sub>				1.8	4.9	6.9	1	8.3	
t <sub>PLH</sub>		A	$\overline{B}_n - 1$	1	5.6	9.2	0.7	10.9	ns
t <sub>PHL</sub>				1.4	5.6	6.8	0.6	9.4	
t <sub>PLH</sub>		A	$\overline{BP}$	1	6.6	6.2	1	10	ns
t <sub>PHL</sub>				2.2	6.3	7.3	1.3	10	
t <sub>PLH</sub>		$\overline{B}$	$\overline{B}_n - 1$	0.3	8.4	10.8	1	11.4	ns
t <sub>PHL</sub>				1.4	7.4	8.9	1.4	10	
t <sub>PLH</sub>		LE	$\overline{B}$ or $\overline{BP}$	2.3	5.6	7.4	0.6	8.8	ns
t <sub>PHL</sub>				2.8	5.1	7.8	1	8.8	
t <sub>PLH</sub>		$\overline{B}$ or $\overline{BP}$	A or AP	2.8	5.3	7.6	1	8.9	ns
t <sub>PHL</sub>				2.6	4.6	7.3	1.2	8.5	
t <sub>PLH</sub>		$\overline{B}$	WIN	2.8	6	7.8	1.3	10.4	ns
t <sub>PHL</sub>				4.4	6.6	8.8	1.1	10.4	
t <sub>PLH</sub>		A	WIN	2.1	4.1	7.1	1.2	8.6	ns
t <sub>PHL</sub>				2.3	4	7	1.4	9.8	
t <sub>PLH</sub>		LE	WIN	1.2	4.4	8.8	1.1	8.6	ns
t <sub>PHL</sub>				2.3	3.5	6.9	1.6	7.2	
t <sub>PLH</sub>		$\overline{\text{COMPETE}}$	WIN	1.6	3.4	6.2	1.3	6.4	ns
t <sub>PHL</sub>				1.7	3.4	6.5	1.3	7.2	
t <sub>PLH</sub>		$\overline{\text{OEB}}$	WIN	1.7	3.5	5.7	1.4	7.7	ns
t <sub>PHL</sub>				2	3.8	5.5	1.6	6.5	
t <sub>PLH</sub>		$\overline{\text{COMPETE}}$	$\overline{B}$	2.6	5.2	7.3	1.7	8.9	ns
t <sub>PHL</sub>				2.4	5.6	7.8	1.3	8.9	
t <sub>PLH</sub>		$\overline{\text{COMPETE}}$	$\overline{BP}$	2.8	6.2	7	2.1	9.2	ns
t <sub>PHL</sub>				3.1	5.7	7.1	2	8.9	
t <sub>PLH</sub>		OEB	$\overline{B}$	2.4	5.3	7.4	1.6	9	ns
t <sub>PHL</sub>				2.3	5.4	7.4	1.5	8	
t <sub>PLH</sub>		$\overline{\text{OEB}}$	$\overline{B}$	3	6.7	8.3	1.7	9.3	ns
t <sub>PHL</sub>				2.2	5.9	6.3	1.2	8.4	
t <sub>PZH</sub>		OEA	A	1.9	4.3	6.7	1.4	9.6	ns
t <sub>PZL</sub>				1.8	3.9	6.6	1.3	7.7	
t <sub>PHZ</sub>		OEA	A	1.7	3.4	7.5	1.3	9.9	ns
t <sub>PLZ</sub>				1.5	3.7	6.4	1.1	7.8	
t <sub>sk(p)</sub>	Skew for any single channel  t <sub>PHL</sub> – t <sub>PLH</sub>  , A to $\overline{B}$ or $\overline{B}$ to A			0.8					ns
				0.5					
t <sub>sk(o)</sub>	Skew between drivers in the same package, A to $\overline{B}$ or $\overline{B}$ to A			0.8					ns
				0.6					
t <sub>r</sub>	Rise time, 1.3 V to 1.8 V, $\overline{B}$ outputs			1	2.2	3.2	1	4.2	ns
t <sub>f</sub>	Fall time, 1.3 V to 1.8 V, $\overline{B}$ outputs			1	1.3	2.3	1	2.5	ns
$\overline{B}$ -port input pulse rejection				1			1		ns



# SN54FB2032, SN74FB2032 9-BIT TTL/BTL COMPETITION TRANSCEIVERS

SCBS175D – NOVEMBER 1991 – REVISED AUGUST 1996

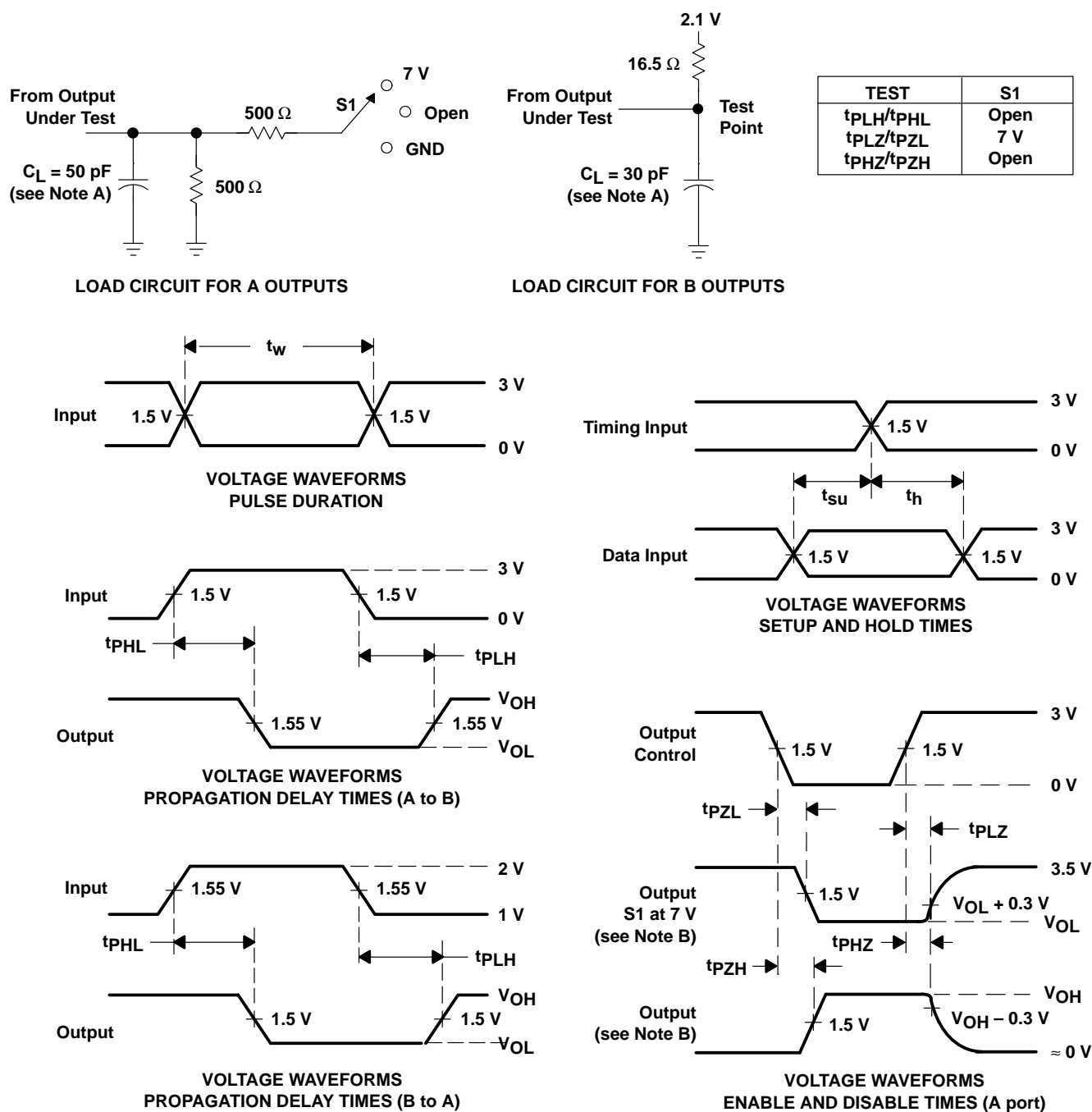
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	SN74FB2032					UNIT
				V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t <sub>PLH</sub>		A or AP	$\overline{B}$ or $\overline{BP}$	2.9	5.2	6.5	2.7	7	ns
t <sub>PHL</sub>				3	4.9	6.3	2.8	6.6	
t <sub>PLH</sub>		A	$\overline{B}_{n-1}$	3.1	5.6	7.4	2.5	8.4	ns
t <sub>PHL</sub>				3.4	5.6	7.4	3.2	9	
t <sub>PLH</sub>		A	$\overline{BP}$	4.5	6.6	8.1	4	8.9	ns
t <sub>PHL</sub>				4.1	6.3	7.7	3.8	8.4	
t <sub>PLH</sub>		$\overline{B}$	$\overline{B}_{n-1}$	5.5	8.4	10.8	4.8	11.4	ns
t <sub>PHL</sub>				5.5	7.4	8.9	4.9	10	
t <sub>PLH</sub>		LE	$\overline{B}$ or $\overline{BP}$	3.7	5.6	6.8	3.4	7.3	ns
t <sub>PHL</sub>				3.5	5.1	6.1	3.1	6.8	
t <sub>PLH</sub>		$\overline{B}$ or $\overline{BP}$	A or AP	3	5.3	7	2.9	7.2	ns
t <sub>PHL</sub>				2.8	4.6	5.9	2	6.1	
t <sub>PLH</sub>		$\overline{B}$	WIN	4	6	7.2	3.4	8.2	ns
t <sub>PHL</sub>				4.2	6.6	8.6	3.9	8.9	
t <sub>PLH</sub>		A	WIN	1.9	4.1	5.4	1.7	5.9	ns
t <sub>PHL</sub>				1.9	4	5.3	1.6	6	
t <sub>PLH</sub>		LE	WIN	2.4	4.4	5.7	2.1	6.4	ns
t <sub>PHL</sub>				1.9	3.5	4.5	1.6	4.9	
t <sub>PLH</sub>		$\overline{\text{COMPETE}}$	WIN	1.6	3.4	4.5	1.3	5	ns
t <sub>PHL</sub>				1.7	3.4	4.4	1.5	4.9	
t <sub>PLH</sub>		$\overline{\text{OEB}}$	WIN	1.7	3.5	4.7	1.4	5.4	ns
t <sub>PHL</sub>				2.2	3.8	4.7	2	5	
t <sub>PLH</sub>		$\overline{\text{COMPETE}}$	$\overline{B}$	3.2	5.2	6.6	2.7	7.3	ns
t <sub>PHL</sub>				3.8	5.6	6.7	3.5	7.3	
t <sub>PLH</sub>		$\overline{\text{COMPETE}}$	$\overline{BP}$	3.9	6.2	7.6	3.8	7.8	ns
t <sub>PHL</sub>				3.9	5.7	7	3.4	7.8	
t <sub>PLH</sub>		OEB	$\overline{B}$	3.1	5.3	6.7	2.9	7.3	ns
t <sub>PHL</sub>				3.4	5.4	6.7	3.2	7.2	
t <sub>PLH</sub>		$\overline{\text{OEB}}$	$\overline{B}$	4.6	6.7	8.1	4.4	8.6	ns
t <sub>PHL</sub>				3.7	5.9	8.1	3.4	8.9	
t <sub>PZH</sub>		OEA	A	2.5	4.3	6	2.2	6.3	ns
t <sub>PZL</sub>				2.2	3.9	5.3	2.2	5.8	
t <sub>PHZ</sub>		OEA	A	1.7	3.4	4.9	1.3	5.5	ns
t <sub>PLZ</sub>				1.9	3.7	5.4	1.7	5.7	
t <sub>sk(p)</sub>	Skew for any single channel  t <sub>PHL</sub> – t <sub>PLH</sub>  , A to $\overline{B}$ or $\overline{B}$ to A			0.8					ns
				0.5					
t <sub>sk(o)</sub>	Skew between drivers in the same package, A to $\overline{B}$ or $\overline{B}$ to A			0.8					ns
				0.6					
t <sub>r</sub>	Rise time, 1.3 V to 1.8 V, $\overline{B}$ outputs			1	2.2	3.2	1	3.2	ns
t <sub>f</sub>	Fall time, 1.3 V to 1.8 V, B outputs			1	1.3	2.3	1	2.5	ns
B-port input pulse rejection				1			1		ns

# SN54FB2032, SN74FB2032 9-BIT TTL/BTL COMPETITION TRANSCEIVERS

SCBS175D – NOVEMBER 1991 – REVISED AUGUST 1996

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: TTL inputs: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ ; BTL inputs: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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