

SN54ABT16377, SN74ABT16377 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

SCBS206 – OCTOBER 1992 – REVISED JULY 1993

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings

description

The 'ABT16377 is a 16-bit positive-edge-triggered D-type flip-flop with a clock (1CLK or 2CLK) input. It is particularly suitable for implementing buffer and storage registers, shift registers, and pattern generators.

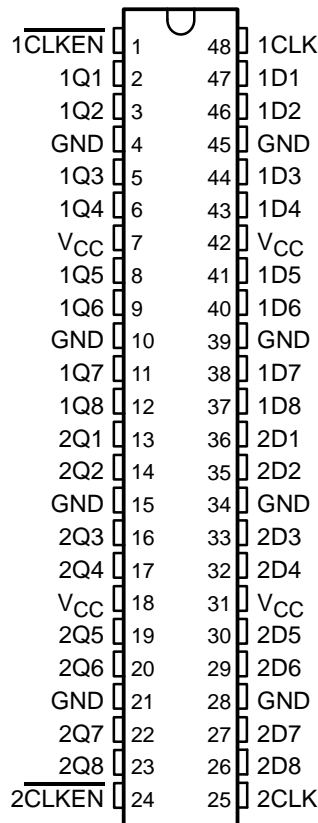
The device can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

Data input information that meets the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the common clock-enable (1CLKEN or 2CLKEN) input is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the buffered clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at CLKEN.

The SN74ABT16377 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16377 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT16377 is characterized for operation from -40°C to 85°C .

SN54ABT16377 . . . WD PACKAGE
SN74ABT16377 . . . DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

Widebus and EPIC-II B are trademarks of Texas Instruments Incorporated.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1993, Texas Instruments Incorporated

SN54ABT16377, SN74ABT16377

16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS

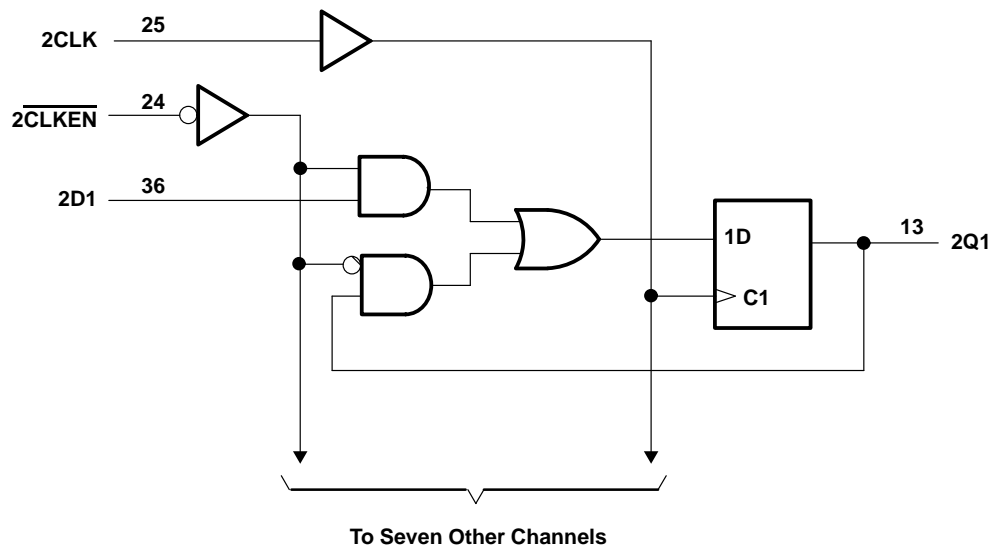
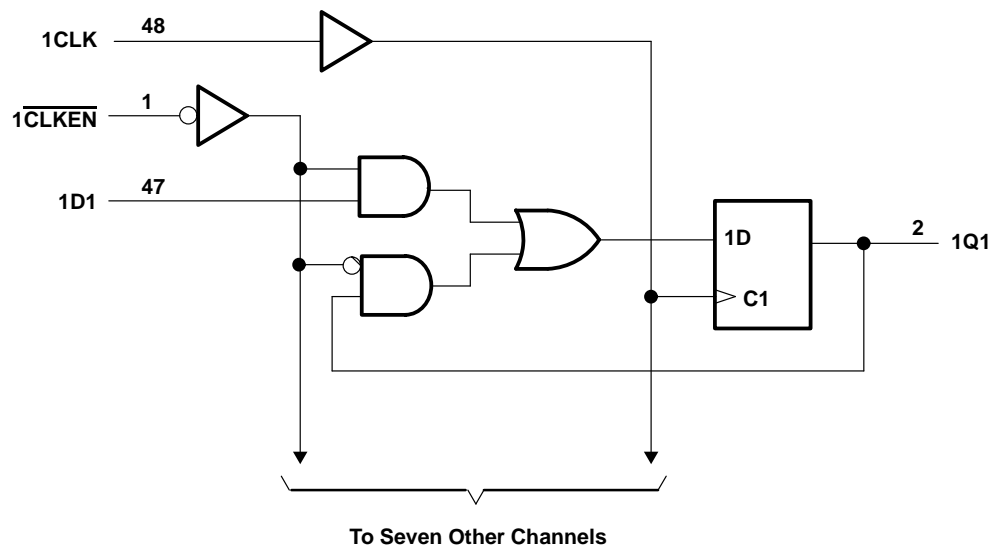
WITH CLOCK ENABLE

SCBS206 – OCTOBER 1992 – REVISED JULY 1993

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT Q
CLKEN	CLK	D	
H	X	X	Q ₀
L	↑	H	H
L	↑	L	L
X	H or L	X	Q ₀

logic diagram (positive logic)



PRODUCT PREVIEW



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54ABT16377, SN74ABT16377
16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH CLOCK ENABLE

SCBS206 – OCTOBER 1992 – REVISED JULY 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT16377	96 mA
SN74ABT16377	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air)	0.85 W
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT16377		SN74ABT16377		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW



SN54ABT16377, SN74ABT16377

16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH CLOCK ENABLE

SCBS206 – OCTOBER 1992 – REVISED JULY 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T _A = 25°C			SN54ABT16377		SN74ABT16377		UNIT	
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V _{IK}	V _{CC} = 4.5 V, I _I = −18 mA		−1.2			−1.2		−1.2		V	
V _{OH}	V _{CC} = 4.5 V, I _{OH} = −3 mA		2.5			2.5		2.5		V	
	V _{CC} = 5 V, I _{OH} = −3 mA		3			3		3			
	V _{CC} = 4.5 V, I _{OH} = −24 mA		2			2					
	V _{CC} = 4.5 V, I _{OH} = −32 mA		2‡					2			
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 48 mA		0.55			0.55				V	
	V _{CC} = 4.5 V, I _{OL} = 64 mA		0.55‡					0.55			
I _I	V _{CC} = 5.5 V, V _I = V _{CC} or GND		±1			±1		±1		μA	
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V		±100					±100		μA	
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high	50			50		50		μA	
I _O §	V _{CC} = 5.5 V, V _O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA	
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND		Outputs high		2		2		2		mA
			Outputs low		67		67		67		
			Outputs disabled		2		2		2		
ΔI _{CC} ¶	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		1.5			1.5		1.5		mA	
C _i	V _I = 2.5 V or 0.5 V									pF	
C _O	V _O = 2.5 V or 0.5 V									pF	

† All typical values are at V_{CC} = 5 V.

‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW



IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.