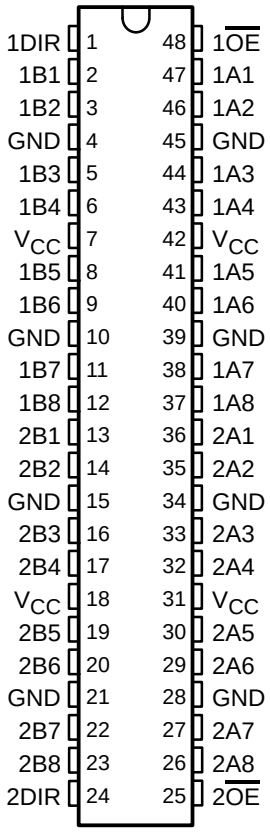
- **A-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABT162245 . . . WD PACKAGE
SN74ABT162245 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The ′ABT162245 are 16-bit (dual-octal) noninverting 3-state transceivers designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

The A-port outputs, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT162245 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

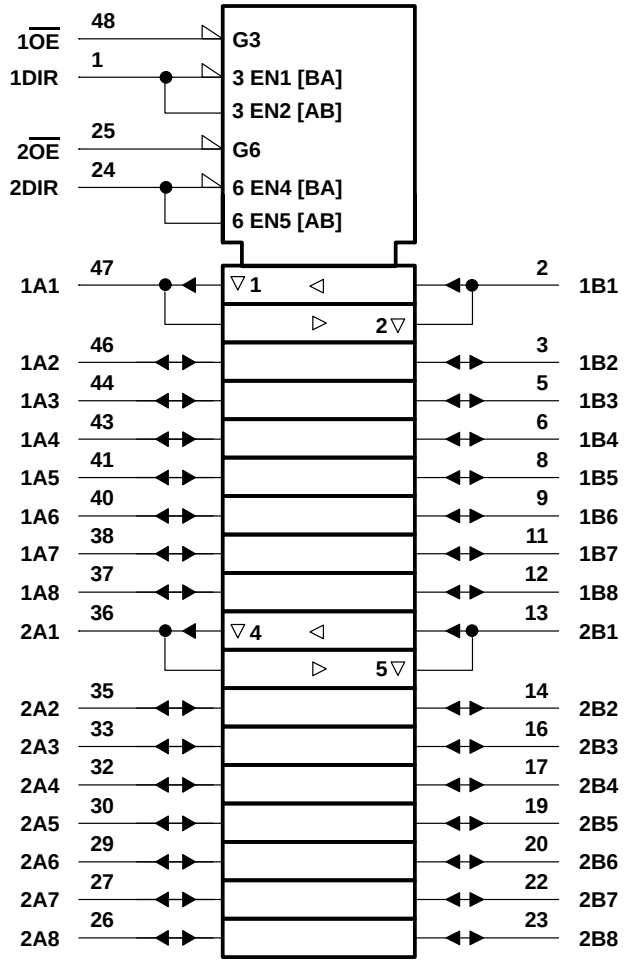
The SN54ABT162245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT162245 is characterized for operation from –40°C to 85°C.

Widebus and EPIC-IIB are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE
(each 8-bit section)

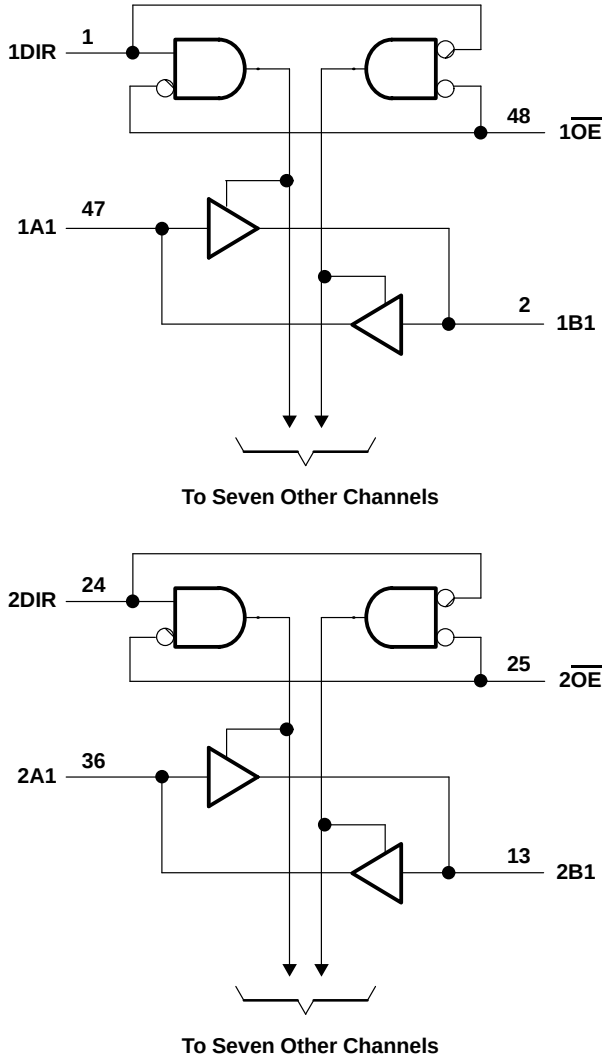
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT162245 (B port) . . . . . 96 mA
SN74ABT162245 (B port) . . . . . 128 mA
SN54/74ABT162245 (A port) . . . . . 30 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package . . . . . 0.85 W
DL package . . . . . 1.2 W
Operating free-air temperature range, T_A: SN54ABT162245 . . . . . –55°C to 125°C
SN74ABT162245 . . . . . –40°C to 85°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

			SN54ABT162245		SN74ABT162245		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	B port		–24		–32	mA
		A port		–12		–12	
I_{OL}	Low-level output current	B port		48		64	mA
		A port		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

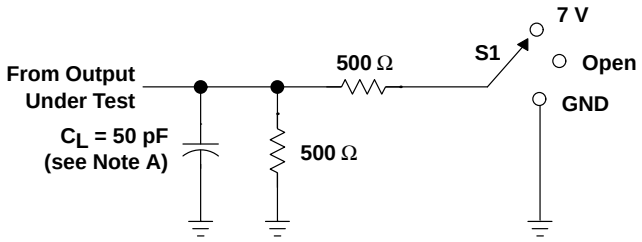
PARAMETER		TEST CONDITIONS		T_A = 25°C			SN54ABT162245		SN74ABT162245		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2		–1.2		–1.2	V
V_{OH}	A port	V_{CC} = 5 V,	I_{OH} = – 1 mA	3.8			2.5		2.5		V
		V_{CC} = 4.5 V	I_{OH} = – 1 mA	3.3			3		3		
			I_{OH} = – 3 mA	3.1			3		3.1		
			I_{OH} = – 12 mA	2.6*					2.6		
	B port	V_{CC} = 5 V,	I_{OH} = – 3 mA	3			3		3		
		V_{CC} = 4.5 V	I_{OH} = – 3 mA	2.5			2.5		2.5		
			I_{OH} = – 24 mA				2				
			I_{OH} = – 32 mA	2*					2		
V_{OL}	A port	V_{CC} = 4.5 V	I_{OL} = 12 mA			0.8		0.8		0.8	V
	B port		I_{OL} = 48 mA			0.45		0.45		0.45	
			I_{OL} = 64 mA			0.55*		0.55		0.55	
I_I	Control inputs	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
	A or B ports					±20		±20		±20	
I_{OZH}‡		V_{CC} = 5.5 V,	V_O = 2.7 V			10		10		10	µA
I_{OZL}‡		V_{CC} = 5.5 V,	V_O = 0.5 V			–10		–10		–10	µA
I_{off}		V_{CC} = 0,	V_I or $V_O \le$ 4.5 V			±100				±100	µA
I_{CEX}	Outputs high	V_{CC} = 5.5 V,	V_O = 5.5 V			50		50		50	µA
I_O§	A port	V_{CC} = 5.5 V,	V_O = 2.5 V	–25	–50	–100	–25	–100	–25	–100	mA
	B port			–50	–100	–180	–50	–180	–50	–180	
I_{CC}	A or B ports	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			2		2		2	mA
			Outputs low			32		32		32	
			Outputs disabled			2		2		2	
ΔI_{CC}¶	Data inputs	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled			1		2		2	mA
			Outputs disabled			0.05		1		0.05	
	Control inputs	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	
C_i		V_I = 2.5 V or 0.5 V			3						pF
C_{io}		V_O = 2.5 V or 0.5 V			6						pF

* On products compliant to MIL-STD-883, Class B, this parameter does not apply.
† All typical values are at V_{CC} = 5 V.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

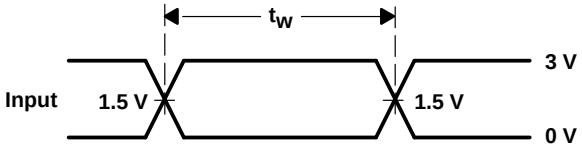
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT162245		SN74ABT162245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1	2.2	3.4	1	4.1	1	3.9	ns
t_{PHL}			1	2.3	3.7	1	4.4	1	4.2	
t_{PLH}	B	A	1	2.7	4.1	1	4.9	1	4.6	ns
t_{PHL}			1.5	3.1	4.6	1.5	5.2	1.5	5.1	
t_{PZH}	$\overline{OE}$	B	1	3.6	5.2	1	6.4	1	6.3	ns
t_{PZL}			1	3.7	5.4	1	6.5	1	6.4	
t_{PHZ}	$\overline{OE}$	B	2	4.4	5.8	2	6.4	2	6.3	ns
t_{PLZ}			1.5	3.3	4.7	1.5	5.6	1.5	5.2	
t_{PZH}	$\overline{OE}$	A	1.5	4.1	6	1.5	7.2	1.5	7.1	ns
t_{PZL}			1.5	4.3	6.1	1.5	7.3	1.5	7	
t_{PHZ}	$\overline{OE}$	A	2	4.5	6.1	2	6.8	2	6.6	ns
t_{PLZ}			1.5	3.7	5.1	1.5	6.1	1.5	5.7	

PARAMETER MEASUREMENT INFORMATION

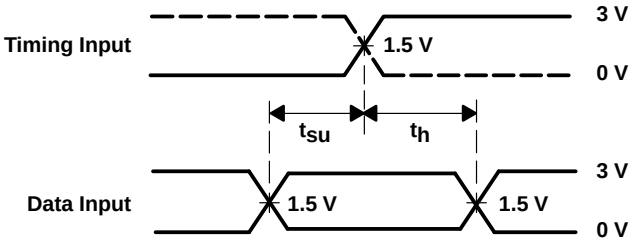


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

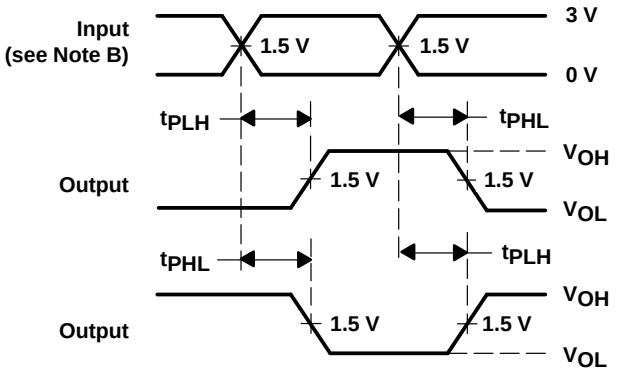
LOAD CIRCUIT FOR OUTPUTS



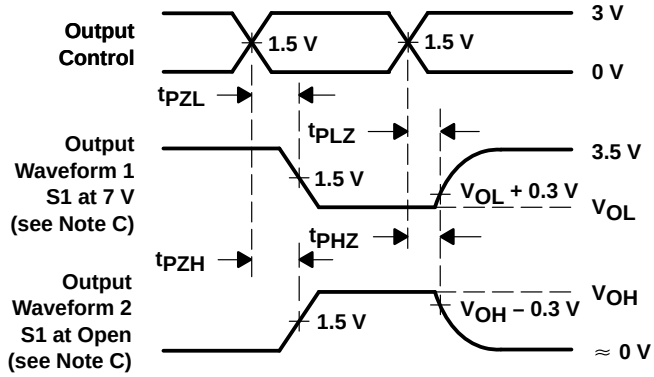
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.