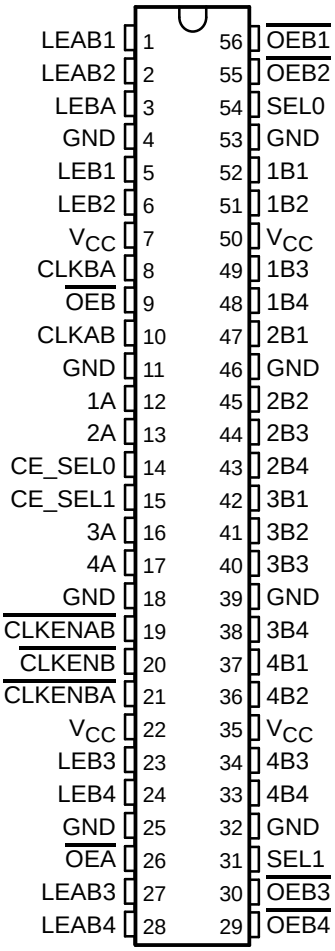
- **B-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Typical $V_{OLP}$ (Output Ground Bounce) < 1 V at $V_{CC}$ = 5 V, $T_A$ = 25°C**
- **Distributed $V_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Bus-Hold Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

**SN54ABT162460 . . . WD PACKAGE**
**SN74ABT162460 . . . DL PACKAGE**
**(TOP VIEW)**




## description

The ′ABT162460 are 4-bit-to-1-bit multiplexed registered transceivers used in applications where four separate data paths must be multiplexed onto or demultiplexed from a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor or bus-interface applications. This device is also useful in memory-interleaving applications.

Five 4-bit I/O ports (1A–4A, 1B1–4, 2B1–4, 3B1–4, and 4B1–4) are available for address and/or data transfer. The output-enable ($\overline{OEB}$, $\overline{OEB1}$–$\overline{OEB4}$, and $\overline{OEA}$) inputs control the bus transceiver functions. These control signals also allow 4-bit or 16-bit control depending on the $\overline{OEB}$ level.

Address and/or data information can be stored using the internal storage latches/flip-flops. The latch-enable (LEB1–LEB4, LEBA, and LEAB1–LEAB4) and clock/clock-enable (CLK/$\overline{CLKEN}$) inputs are used to control data storage. When either one of the latch-enable inputs is high, the latch is transparent (clock is a don't care as long as the latch-enable is high). When the latch-enable input goes low (providing that the clock does not transit from low to high), the data present at the inputs is latched and remains latched until the latch-enable input is returned high. When the clock-enable is low and the corresponding latch-enable is low, data can be clocked on the low to high transition of the clock. When either the clock-enable or the corresponding latch-enable is high, the clock is a don't care.

Four select (SEL0, SEL1, CE_SEL0, and CE_SEL1) pins are provided to multiplex data (A port), or to select one of four clock-enables (B port). This allows the user to have the flexibility of controlling one bit at a time.

The B-port outputs, which are designed to sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

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## description (continued)

To ensure the high-impedance state during power-up or power-down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT162460 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT162460 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT162460 is characterized for operation from –40°C to 85°C.

### Function Tables

**A-TO-B OUTPUT ENABLE†**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OEB}$ | $\overline{OEBn}$ | Bn |
| H | H | Z |
| H | L | Z |
| L | H | Z |
| L | L | Active |

† n = 1, 2, 3, 4

**A-TO-B STORAGE**
**(assuming $\overline{OEB}$ = L, $\overline{OEBn}$ = L)‡**

| INPUTS | | | | | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{CLKENAB}$ | CE_SEL1 | CE_SEL0 | CLKAB | LEAB1 | LEAB2 | LEAB3 | LEAB4 | B1 | B2 | B3 | B4 |
| X | X | X | H or L | H | L | L | L | A | $A_0$ | $A_0$ | $A_0$ |
| X | X | X | H or L | H | H | H | L | A | A | A | $A_0$ |
| L | X | X | L | L | L | L | L | $A_0$ | $A_0$ | $A_0$ | $A_0$ |
| L | L | L | ↑ | L | L | L | L | A | $A_0$ | $A_0$ | $A_0$ |
| L | L | H | ↑ | L | L | L | L | $A_0$ | A | $A_0$ | $A_0$ |
| L | H | L | ↑ | L | L | L | L | $A_0$ | $A_0$ | A | $A_0$ |
| L | H | H | ↑ | L | L | L | L | $A_0$ | $A_0$ | $A_0$ | A |
| H | X | X | ↑ | L | L | L | L | $A_0$ | $A_0$ | $A_0$ | $A_0$ |

‡ This table does not cover all the latch-enable cases since they have similar results.

## Function Tables (Continued)

**B-TO-A STORAGE**
**(before point P)**

| INPUTS | | | | | | | | P |
|---|---|---|---|---|---|---|---|---|
| $\overline{\text{CLKENB}}$ | CLKBA | LEB1 | LEB2 | LEB3 | LEB4 | SEL1 | SEL0 | |
| X | X | H | L | L | L | L | L | B1 |
| X | X | L | H | L | L | L | H | B2 |
| X | X | L | L | H | L | H | L | B3 |
| X | X | L | L | L | H | H | H | B4 |
| L | ↑ | L | L | L | L | L | L | B1 |
| | | | | | | L | H | B2 |
| | | | | | | H | L | B3 |
| | | | | | | H | H | B4 |
| L | L | L | L | L | L | L | L | $B1_0$† |
| | | | | | | L | H | $B2_0$† |
| | | | | | | H | L | $B3_0$† |
| | | | | | | H | H | $B4_0$† |

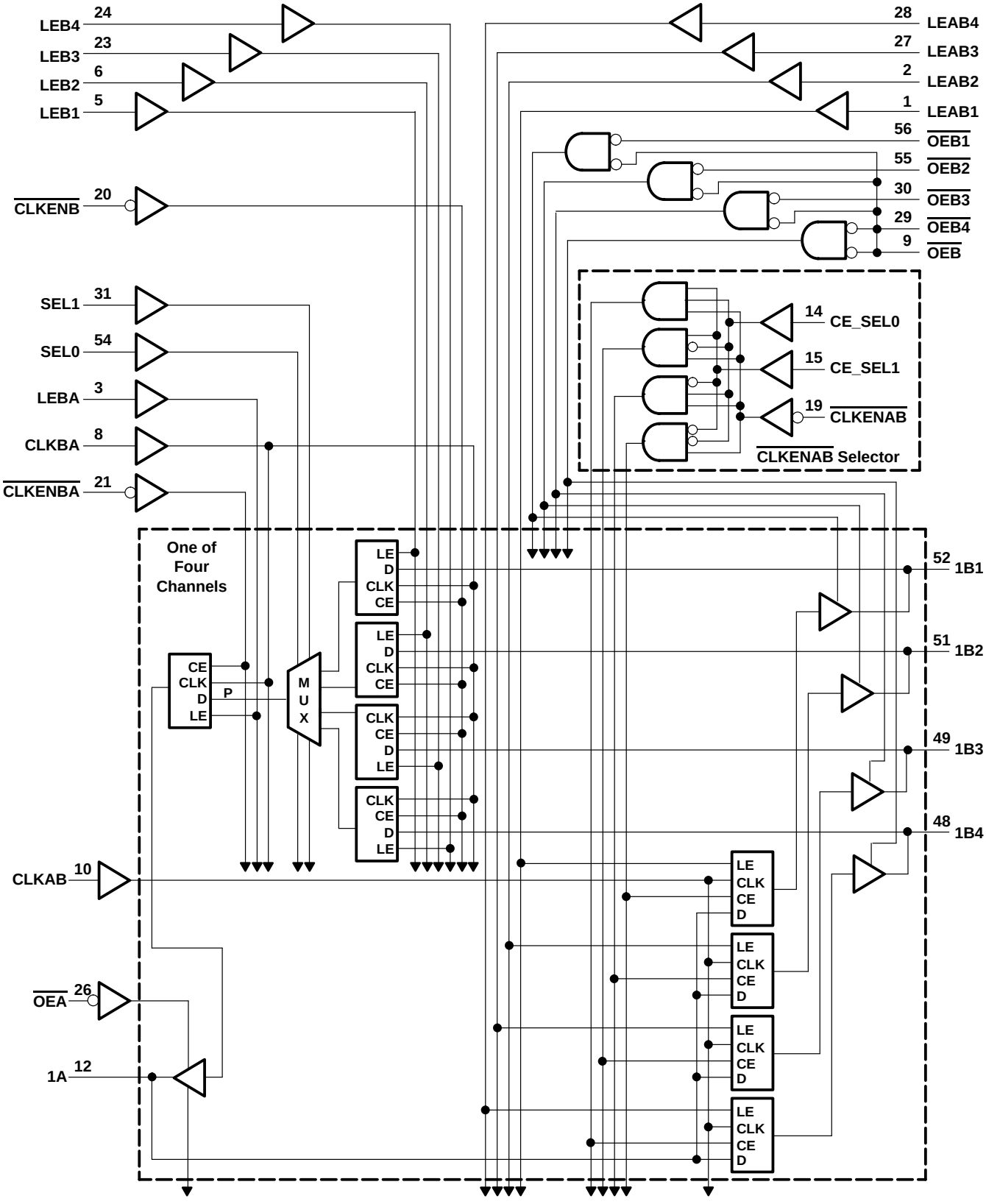
† Output level before the indicated steady-state input conditions were established.

**B-TO-A STORAGE**
**(after point P)**

| INPUTS | | | | | OUTPUT |
|---|---|---|---|---|---|
| $\overline{\text{CLKENBA}}$ | CLKBA | LEBA | $\overline{\text{OEA}}$ | B | A |
| X | X | X | H | X | Z |
| X | X | H | L | L | L |
| X | X | H | L | H | H |
| H | X | L | L | X | $A_0$† |
| L | ↑ | L | L | L | L |
| L | ↑ | L | L | H | H |
| L | L | L | L | X | $A_0$† |

† Output level before the indicated steady-state input conditions were established.

## logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ . . . . . –0.5 V to 5.5 V
Current into any output in the low state, $I_O$: SN54ABT162460 (A port) . . . . . 96 mA
SN74ABT162460 (A port) . . . . . 128 mA
B port . . . . . 30 mA
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –18 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . –50 mA
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 2): DL package . . . . . 1.4 W
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

### recommended operating conditions (see Note 3)

| | | | SN54ABT162460 | | | SN74ABT162460 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | A port | | | –24 | | | –32 | mA |
| | | B port | | | –12 | | | –12 | |
| $I_{OL}$ | Low-level output current | A port | | | 48 | | | 64 | mA |
| | | B port | | | 12 | | | 12 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | | 10 | | | 10 | ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | | 200 | | | 200 | | | µs/V |
| $T_A$ | Operating free-air temperature | | –55 | | 125 | –40 | | 85 | °C |

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54ABT162460 | | | SN74ABT162460 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | A port | $V_{CC}$ = 5 V, | $I_{OH}$ = – 3 mA | 3 | 3.4 | | 3 | 3.4 | | V |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = – 3 mA | 2.5 | 3 | | | | | |
| | | | $I_{OH}$ = – 32 mA | | | | 2 | 2.7 | | |
| | B port | $V_{CC}$ = 5 V, | $I_{OH}$ = – 1 mA | 3.8 | 4.2 | | 4.2 | | | |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = – 1 mA | 3.3 | 3.7 | | 3.7 | | | |
| | | | $I_{OH}$ = – 3 mA | 3 | 3.6 | | 3.6 | | | |
| | | | $I_{OH}$ = – 12 mA | | | | 3.3 | | | |
| $V_{OL}$ | A port | $V_{CC}$ = 4.5 V | $I_{OL}$ = 24 mA | | 0.25 | 0.55 | | | | V |
| | | | $I_{OL}$ = 64 mA | | | | | 0.3 | 0.55 | |
| | B port | $V_{CC}$ = 4.5 V | $I_{OL}$ = 8 mA | | 0.4 | 0.8 | | 0.4 | 0.65 | |
| | | | $I_{OL}$ = 12 mA | | | | | 0.5 | 0.8 | |
| $I_I$ | Control inputs | $V_{CC}$ = 0 to 5.5 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | | ±1 | µA |
| | A or B ports | $V_{CC}$ = 2.1 V to 5.5 V, | $V_I$ = $V_{CC}$ or GND | | | ±20 | | | ±20 | |
| $I_{I(hold)}$ | A or B ports | $V_{CC}$ = 5.5 V, | $V_I$ = 0.8 V | 75 | | 500 | 75 | | 500 | µA |
| | | $V_{CC}$ = 4.5 V, | $V_I$ = 2 V | –75 | | –500 | –75 | | –500 | |
| $I_O$‡ | A port | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | –50 | –110 | –180 | –50 | | –180 | mA |
| | B port | $V_{CC}$ = 5.5 V | $V_O$ = 2.5 V | –25 | –55 | –90 | –25 | | –90 | |
| | | | $V_O$ = 0 | –50 | –110 | –180 | –50 | | –180 | |
| $I_{CEX}$ | Outputs high | $V_{CC}$ = 5.5 V, | $V_O$ = 5.5 V | | | 50 | | | 50 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ ≤ 4.5 V | | | ±100 | | | ±100 | µA |
| $I_{OZPU}$§ | | $V_{CC}$ = 0 to 2.1 V, $\overline{OE}$ = X | $V_O$ = 0.5 V to 2.7 V, | | | ±50 | | | ±50 | µA |
| $I_{OZPD}$§ | | $V_{CC}$ = 2.1 V to 0, $\overline{OE}$ = X | $V_O$ = 0.5 V to 2.7 V, | | | ±50 | | | ±50 | µA |
| $I_{OZH}$¶ | | $V_{CC}$ = 2.1 V to 5.5 V, $\overline{OE}$ ≥ 2 V | $V_O$ = 2.7 V, | | | 10 | | | 10 | µA |
| $I_{OZL}$¶ | | $V_{CC}$ = 2.1 V to 5.5 V, $\overline{OE}$ ≥ 2 V | $V_O$ = 0.5 V, | | | –10 | | | –10 | µA |
| $I_{CC}$ | Outputs high | $V_{CC}$ = 5.5 V, | Outputs open | | | 1.5 | | 0.7 | 1.5 | mA |
| | A port low | | | | | 10 | | 6 | 10 | |
| | B port low | | | | | 32 | | 18 | 32 | |
| | Outputs disabled | | | | | 1.5 | | 0.7 | 1.5 | |
| $\Delta I_{CC}$# | | $V_{CC}$ = 5.5 V, Other inputs at $V_{CC}$ or GND | One input at 3.4 V, | | | 1 | | | 1 | mA |
| $C_i$ | Control inputs | $V_I$ = 2.5 V or 0.5 V | | | 3.5 | | | 3.5 | | pF |
| $C_{io}$ | A or B ports | $V_O$ = 2.5 V or 0.5 V | | | 8 | | | 8 | | pF |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ This parameter is characterized but not tested.
¶ The parameters $I_{OZH}$ and $I_{OZL}$ include the input leakage current.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

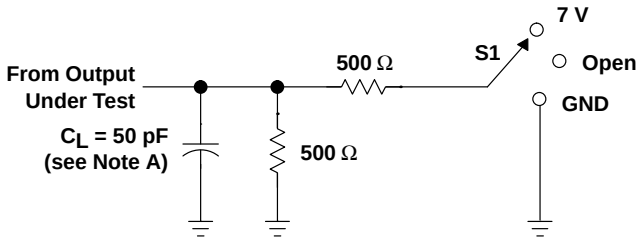
**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(see Figure 1)**

| | | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | SN54ABT162460 | | SN74ABT162460 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | | 0 | 160 | 0 | 160 | 0 | 160 | MHz |
| $t_w$ | Pulse duration | CLKAB high or low | | 3.8 | | 3.8 | | 3.8 | | ns |
| | | CLKBA high or low | | 4.5 | | 4.5 | | 4.5 | | |
| | | LEAB1, 2, 3, or 4 high | | 2.8 | | 2.8 | | 2.8 | | |
| | | LEBA high | | 2.8 | | 2.8 | | 2.8 | | |
| | | LEB1, 2, 3, or 4 high | | 3 | | 3 | | 3 | | |
| $t_{su}$ | Setup time | Before CLKAB↑ | A bus | 2.5 | | 2.5 | | 2.5 | | ns |
| | | | CE_SEL0/1 | 3.2 | | 3.2 | | 3.2 | | |
| | | | $\overline{\text{CLKENAB}}$ | 3.2 | | 3.2 | | 3.2 | | |
| | | Before LEAB1, 2, 3, or 4 ↓ | A bus | 3.6 | | 3.6 | | 3.6 | | |
| | | Before CLKBA↑ | B bus | 3.8 | | 3.8 | | 3.8 | | |
| | | | $\overline{\text{CLKENB}}$ | 2.3 | | 2.3 | | 2.3 | | |
| | | | $\overline{\text{CLKENBA}}$ | 2.5 | | 2.5 | | 2.5 | | |
| | | | LEB1, 2, 3, or 4 | 4.3 | | 4.3 | | 4.3 | | |
| | | | SEL0/1 | 4.5 | | 4.5 | | 4.5 | | |
| | | Before LEB1, 2, 3, or 4 ↓ | B bus | 3.2 | | 3.2 | | 3.2 | | |
| | | Before LEBA↓ | B bus | 4 | | 4 | | 4 | | |
| | | | LEB1, 2, 3, or 4 | 4.4 | | 4.4 | | 4.4 | | |
| | | | SEL0/1 | 4.3 | | 4.3 | | 4.3 | | |
| $t_h$ | Hold time | After CLKAB↑ | A bus | 0.5 | | 0.5 | | 0.5 | | ns |
| | | | CE_SEL0/1 | 1.1 | | 1.1 | | 1.1 | | |
| | | | $\overline{\text{CLKENAB}}$ | 0.5 | | 0.5 | | 0.5 | | |
| | | After LEAB1, 2, 3, or 4 ↓ | A bus | 1.2 | | 1.2 | | 1.2 | | |
| | | After CLKBA↑ | B bus | 1.3 | | 1.3 | | 1.3 | | |
| | | | $\overline{\text{CLKENB}}$ | 1 | | 1 | | 1 | | |
| | | | $\overline{\text{CLKENBA}}$ | 1 | | 1 | | 1 | | |
| | | | SEL0/1 | 0 | | 0 | | 0 | | |
| | | After LEB1, 2, 3, or 4 ↓ | B bus | 1.5 | | 1.5 | | 1.5 | | |
| | | After LEBA↓ | B bus | 0.4 | | 0.4 | | 0.4 | | |
| | | | SEL0/1 | 0.1 | | 0.1 | | 0.1 | | |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)**

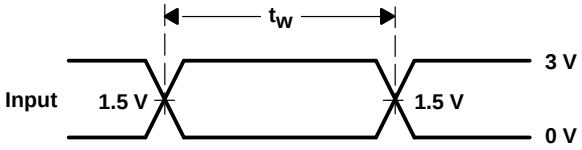
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABT162460 | | SN74ABT162460 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 160 | | | 160 | | 160 | | MHz |
| $t_{PLH}$ | B | A | 2 | 3.6 | 5.9 | 2 | 7.1 | 2 | 6.5 | ns |
| $t_{PHL}$ | | | 2 | 3.5 | 5.8 | 2 | 6.8 | 2 | 6.5 | |
| $t_{PZH}$ | $\overline{OEA}$ | A | 1.5 | 2.8 | 4.8 | 1.5 | 5.9 | 1.5 | 5.6 | ns |
| $t_{PZL}$ | | | 1.5 | 2.6 | 4.8 | 1.5 | 5.7 | 1.5 | 5.5 | |
| $t_{PHZ}$ | $\overline{OEA}$ | A | 2 | 3.8 | 5.3 | 2 | 6 | 2 | 5.9 | ns |
| $t_{PLZ}$ | | | 1.5 | 4 | 6.1 | 1.5 | 7 | 1.5 | 6.5 | |
| $t_{PLH}$ | A | B | 2 | 3.3 | 5.5 | 2 | 6.5 | 2 | 6.2 | ns |
| $t_{PHL}$ | | | 2 | 3.7 | 5.8 | 2 | 6.8 | 2 | 6.5 | |
| $t_{PZH}$ | $\overline{OEB}$ | B | 2 | 3.9 | 5.8 | 2 | 7.1 | 2 | 6.8 | ns |
| $t_{PZL}$ | | | 2 | 3.7 | 5.6 | 2 | 6.6 | 1.5 | 6.3 | |
| $t_{PHZ}$ | $\overline{OEB}$ | B | 2 | 4 | 5.6 | 2 | 6.4 | 2 | 6.2 | ns |
| $t_{PLZ}$ | | | 2 | 3.7 | 5.2 | 2 | 6.1 | 2 | 5.8 | |
| $t_{PZH}$ | $\overline{OEB1}$, $\overline{2}$, $\overline{3}$, $\overline{4}$ | B | 2 | 3.7 | 5.8 | 2 | 6.8 | 2 | 6.6 | ns |
| $t_{PZL}$ | | | 2 | 3.5 | 5.4 | 2 | 6.4 | 2 | 6.2 | |
| $t_{PHZ}$ | $\overline{OEB1}$, $\overline{2}$, $\overline{3}$, $\overline{4}$ | B | 1.5 | 3.3 | 4.8 | 1.5 | 5.4 | 1.5 | 5.3 | ns |
| $t_{PLZ}$ | | | 1.5 | 3.1 | 4.4 | 1.5 | 5.1 | 1.5 | 4.9 | |
| $t_{PLH}$ | CLKBA | A | 1.5 | 4.2 | 6.7 | 1.5 | 8.1 | 1.5 | 7.4 | ns |
| $t_{PHL}$ | | | 1.5 | 4.4 | 6.9 | 1.5 | 8.4 | 1.5 | 7.7 | |
| $t_{PLH}$ | CLKAB | B | 2 | 3.5 | 5.8 | 2 | 6.9 | 2 | 6.5 | ns |
| $t_{PHL}$ | | | 2 | 3.7 | 6 | 2 | 7 | 2 | 6.5 | |
| $t_{PLH}$ | LEBA | A | 1.5 | 3 | 5.2 | 1.5 | 6.3 | 1.5 | 5.8 | ns |
| $t_{PHL}$ | | | 1.5 | 3 | 5 | 1.5 | 6.3 | 1.5 | 5.8 | |
| $t_{PLH}$ | LEAB1, 2, 3, 4 | B | 2 | 3.4 | 5.4 | 2 | 6.5 | 2 | 6.2 | ns |
| $t_{PHL}$ | | | 2 | 3.6 | 5.7 | 2 | 6.3 | 2 | 6.2 | |
| $t_{PLH}$ | LEBA1, 2, 3, 4 | A | 2 | 4 | 6.5 | 2 | 7.8 | 2 | 7.2 | ns |
| $t_{PHL}$ | | | 2 | 4 | 6.1 | 2 | 7.5 | 2 | 6.8 | |
| $t_{PLH}$ | SEL | A | 2 | 4.1 | 6.7 | 2 | 8.1 | 2 | 7.5 | ns |
| $t_{PHL}$ | | | 2 | 3.8 | 6.2 | 2 | 7.3 | 2 | 6.9 | |

## PARAMETER MEASUREMENT INFORMATION

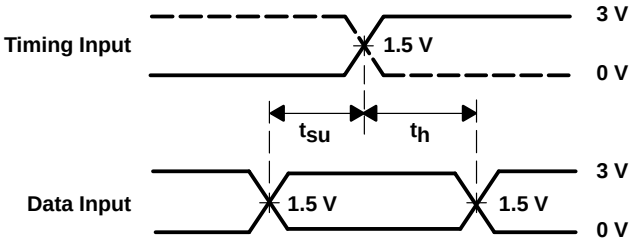



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |

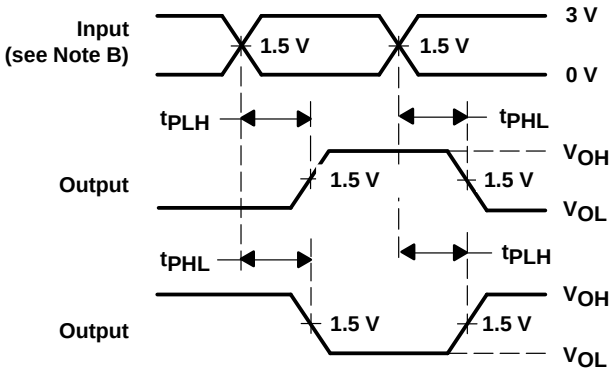
LOAD CIRCUIT FOR OUTPUTS



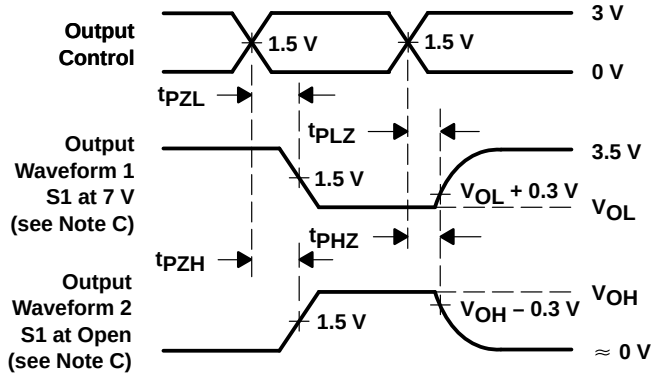

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

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