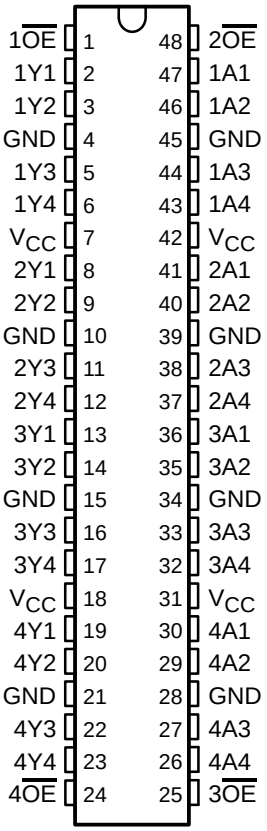
# SN74ABT16240
# 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCBS346 – MAY 1994

- **Member of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical $V_{OLP}$ (Output Ground Bounce) < 1 V at $V_{CC}$ = 5 V, $T_A$ = 25°C**
- **Distributed $V_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA $I_{OH}$, 64-mA $I_{OL}$)**
- **Packaged in Plastic 300-mil Shrink Small-Outline (SSOP) Packages**

**DL PACKAGE**
**(TOP VIEW)**




## description

The SN74ABT16240 is a 16-bit buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides inverting outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16240 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ABT16240 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each 4-bit buffer)**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | L |
| L | L | H |
| H | X | Z |

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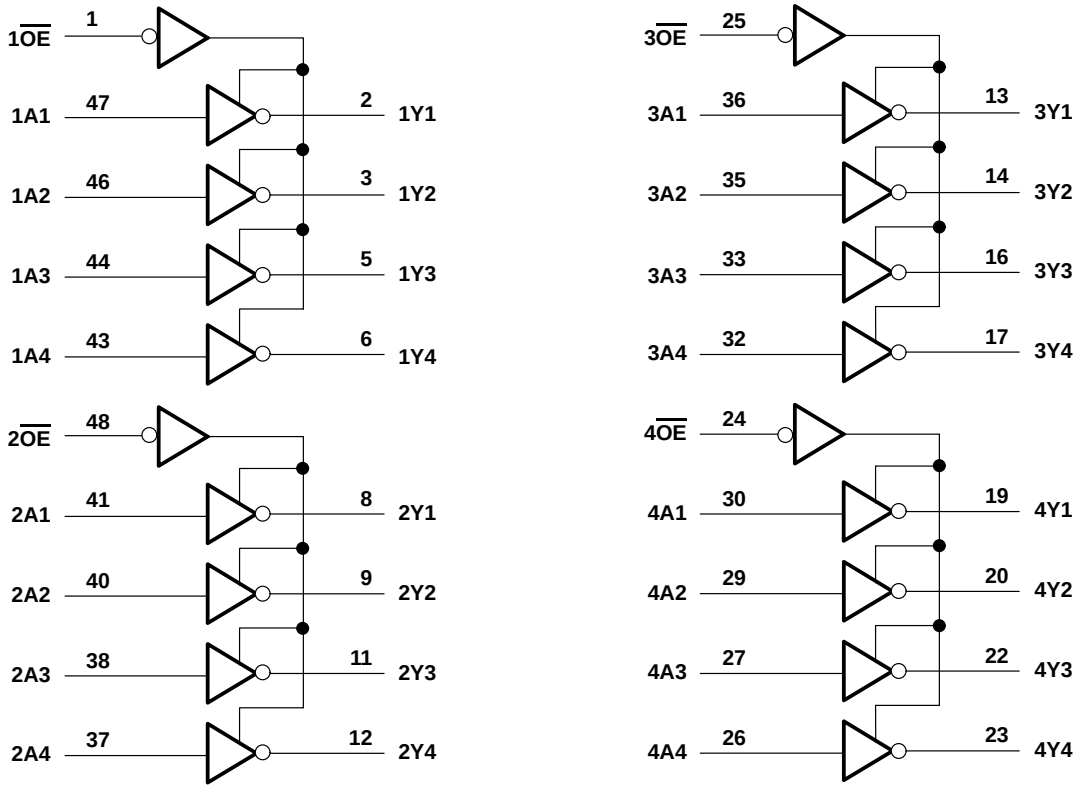
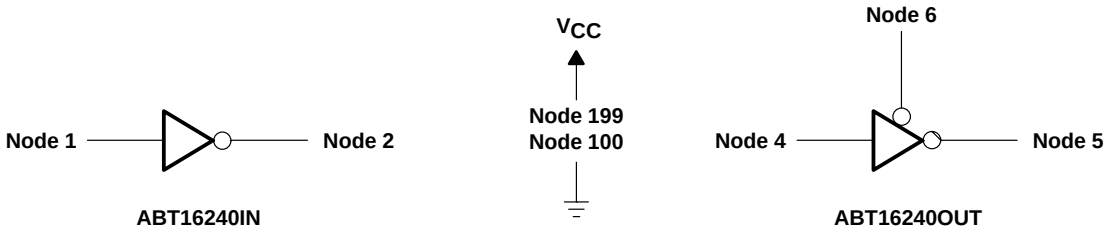
## logic diagram (positive logic)




## SPICE block diagram




**SPICE FUNCTION TABLE**

| NODE | | OPERATION | NODE | | | OPERATION |
|---|---|---|---|---|---|---|
| 1 | 2 | | 4 | 5 | 6 | |
| L | H | Input | L | H | L | Output |
| H | L | Input | H | L | L | Output |
| | | | X | Z | H | Hi-Z |

## SPICE netlist

```
*    ABT16240 SPICE I/O MODEL SUBCIRCUIT
*    ADVANCED BUS INTERFACE
*    ADVANCED SYSTEM LOGIC, TEXAS INSTRUMENTS
*
*    SUBCIRCUITS:  ABT16240IN, ABT16240OUT
*
*    PACKAGE PARASITICS
       .LIB 'PKGS.LIB'   SSOP48
*
*    PROCESS MODELS
       .LIB 'EPIC2B.LIB' NOMINAL_L13
*      .LIB 'EPIC2B.LIB' STRONG_L13
*      .LIB 'EPIC2B.LIB' WEAK_L13
*
* ABT16240 INPUT SUBCIRCUIT
*    NODES:              INPUT NODE
*                        |     INTERNAL OUTPUT NODE
*                        |     |     VCC
*                        |     |     |     GND
*                        |     |     |     |
.SUBCKT ABT16240IN       1     2     199   100
 X_PKGIN           1     1001                    SSOP48_47
 X_PKGVCC          199   1199                    SSOP48_07
 X_PKGGND          100   1100                    SSOP48_04
 XABT16240IN       1001  2     1199  1100        ABT16240__IN
.ENDS ABT16240IN
*
* ABT16240 OUTPUT SUBCIRCUIT
*    NODES:              INTERNAL INPUT NODE
*                        |     OUTPUT NODE
*                        |     |     INTERNAL OE NODE
*                        |     |     |     VCC
*                        |     |     |     |     GND
*                        |     |     |     |     |
.SUBCKT ABT16240OUT      4     5     6     199   100
 X_PKGOUT          5     1005                    SSOP48_02
 X_PKGVCC          199   1199                    SSOP48_07
 X_PKGGND          100   1100                    SSOP48_04
 XABT16240OUT      4     1005  6     1199  1100  ABT16240__OUT
.ENDS ABT16240OUT
*
.SUBCKT ABT16240__IN     501   502   599   500
 XP1         502   504   506   599   PM          WP=200U     LP=0.8U
 XP2         509   502   599   599   PM          WP=20U      LP=0.8U
 XP3         506   509   599   599   PM          WP=85U      LP=0.8U
 XP4         508   500   599   599   PM          WP=50U      LP=0.8U
 XN1         502   504   500   500   NM          WN=220U     LN=0.8U
 XN2         509   502   500   500   NM          WN=20U      LN=0.8U
 XN4         599   500   508   500   NM          WN=20U      LN=0.8U
 QA          599   508   507         Q2_NPN      10
 QB          599   507   506         Q5_NPN      60
 Q_ESD1      501   500   500         Q7_NPN      200
 Q_ESD       504   505   500         Q5_NPN      46
 XR1         506   507   507   507   RMOS        WR=4U       RES=6K
 RESD1       501   504                           50
 RESD2       505   500                           1K
 CBP         501   500                           0.3P
 CL          502   500                           0.2P
.ENDS ABT16240__IN
*
.SUBCKT ABT16240__OUT    601   602   603   699   600
 XP1         605   603   699   699   PM          WP=200U     LP=0.8U
 XP4         601   603   621   699   PM          WP=40U      LP=0.8U
 XP5         613   601   605   699   PM          WP=30U      LP=0.8U
 XP10        618   603   699   699   PM          WP=50U      LP=0.8U
 XP11        607   612   605   699   PM          WP=60U      LP=0.8U
 XN1         607   601   608   600   NM          WN=100U     LN=0.8U
```

## SPICE netlist (continued)

```
XN2          606   619   607   600   NM          WN=50U      LN=0.8U
XN3          608   609   600   600   NM          WN=25U      LN=0.8U
XN4          608   603   600   600   NM          WN=80U      LN=0.8U
XN6          613   603   600   600   NM          WN=25U      LN=0.8U
XN7          602   621   600   600   NM          WN=100U     LN=0.8U
XN8          621   603   600   600   NM          WN=10U      LN=0.8U
XN9          601   622   621   600   NM          WN=20U      LN=0.8U
XN10         619   619   620   600   NM          WN=25U      LN=0.8U
XN11         620   604   602   600   NM          WN=25U      LN=0.8U
XN12         613   601   600   600   NM          WN=40U      LN=0.8U
QM1          616   615   602         Q9_NPN      200
QM2          602   608   600         Q11_NPN     600
QM3          614   613   615         Q4_NPN      15
QD4          614   614   616         Q2_NPN      8
QDR1         615   615   613         Q2_NPN      8
D1           613   614               D1_GDS      156
D2           699   617               D9_GSD      4700
XR1          606   605   605   605   RMOS        WR=6U       RES=1K
XR2          607   606   606   606   RMOS        WR=4U       RES=3K
XR3          614   605   605   605   RMOS        WR=6U       RES=1K
R4           616   617                           10
XR10         619   618   618   618   RMOS        WR=3U       RES=20K
XPVREF       670   603   699   699   PM          WP=50U      LP=0.8U
XNVREF       671   671   600   600   NM          WN=30U      LN=0.8U
XRVREF1      604   670   670   670   RMOS        WR=3U       RES=20K
XRVREF2      671   604   604   604   RMOS        WR=3U       RES=1.5K
XNCLAMP      673   612   674   600   NM          WN=250U     LN=0.8U
DCLAMP1      608   673               D6_GSD      800
DCLAMP2      674   602               D6_GSD      800
XPNOR1       675   609   699   699   PM          WP=30U      LP=0.8U
XPNOR2       612   611   675   699   PM          WP=30U      LP=0.8U
XNNOR1       612   611   600   600   NM          WN=6U       LN=0.8U
XNNOR2       612   609   600   600   NM          WN=6U       LN=0.8U
XP_INV1      609   601   699   699   PM          WP=20U      LP=0.8U
XN_INV1      609   601   600   600   NM          WN=10U      LN=0.8U
XP_INV2      622   603   699   699   PM          WP=15U      LP=0.8U
XN_INV2      622   603   600   600   NM          WN=5U       LN=0.8U
XP_INV3      610   603   699   699   PM          WP=4U       LP=0.8U
XN_INV3      610   603   600   600   NM          WN=4U       LN=0.8U
XP_INV4      611   610   699   699   PM          WP=4U       LP=0.8U
XN_INV4      611   610   600   600   NM          WN=4U       LN=0.8U
CBP          602   600                           0.3P
.ENDS ABT16240__OUT
*
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