

SN74CBT3251 8-BIT TO 1-BIT FET MULTIPLEXER/DEMULTIPLEXER

SCDS019C – MAY 1995 – REVISED AUGUST 1996

- Functionally Equivalent to QS3251
- 5- Ω Switch Connection Between Two Ports
- TTL-Compatible Control Input Levels
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

description

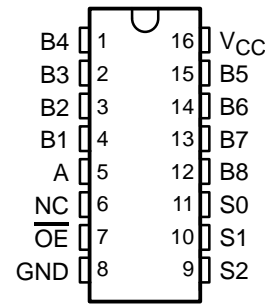
The SN74CBT3251 is an 8-bit to 1-bit high-speed TTL-compatible FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

When output enable (\overline{OE}) is low, the SN74CBT3251 is enabled. S0, S1, and S2 select one of the B outputs for the A-input data.

The SN74CBT3251 is available in TI's shrink small-outline (DB) and thin shrink small-outline (PW) packages, which provide the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74CBT3251 is characterized for operation from -40°C to 85°C .

D, DB, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

S2	S1	S0	\overline{OE}	FUNCTION
X	X	X	H	Disconnect
L	L	L	L	A = B1
L	L	H	L	A = B2
L	H	L	L	A = B3
L	H	H	L	A = B4
H	L	L	L	A = B5
H	L	H	L	A = B6
H	H	L	L	A = B7
H	H	H	L	A = B8



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**TEXAS
INSTRUMENTS**

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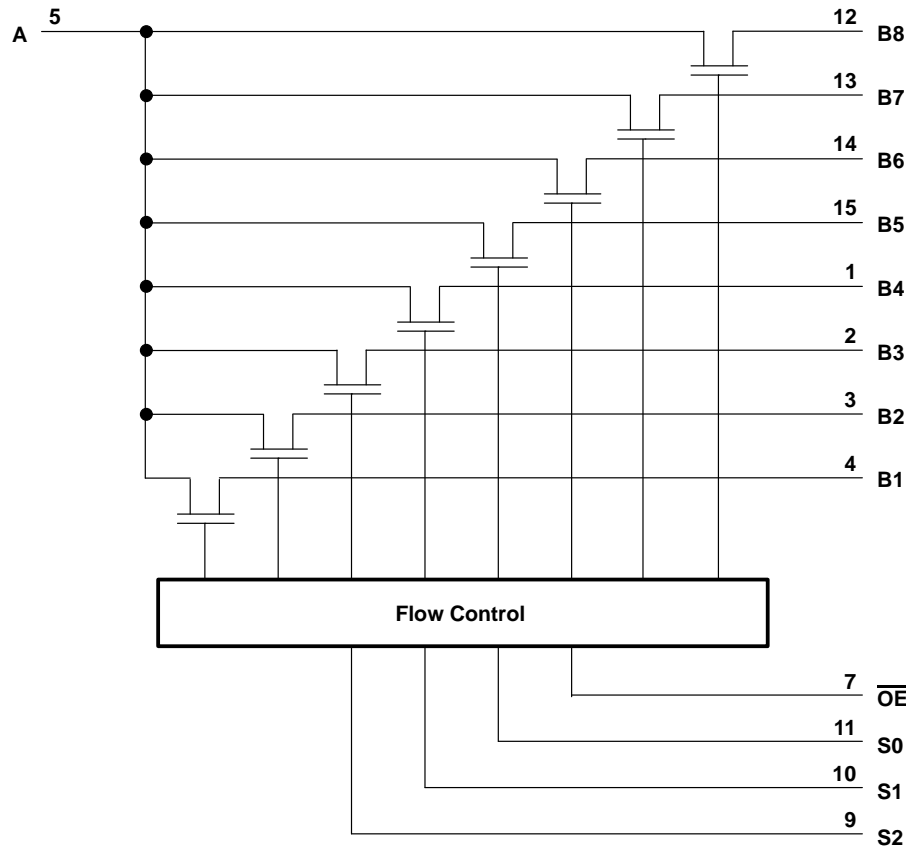
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PRODUCT PREVIEW

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logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_K ($V_{I/O} < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
D package	1.3 W
DB package	0.55 W
PW package	0.5 W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

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recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA			–1.2	V
I_I	$V_{CC} = 5.5$ V, $V_I = 5.5$ V or GND			± 1	μ A
I_{CC}	$V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND			3	μ A
ΔI_{CC}^\ddagger	Control pins $V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND			2.5	mA
C_i	Control pins $V_I = 3$ V or 0			3	pF
$C_{io(OFF)}$	A port				pF
	B port			6	
r_{on}^\S	$V_{CC} = 4$ V, $V_I = 2.4$ V, $I_I = 15$ mA				Ω
	$V_{CC} = 4.5$ V	$V_I = 0$, $I_I = 64$ mA		5	
		$V_I = 0$, $I_I = 30$ mA		5	
		$V_I = 2.4$ V, $I_I = 15$ mA		10	

† All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V ± 0.5 V		$V_{CC} = 4$ V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}^\parallel	A or B	B or A		0.25		0.25	ns
t_{en}	\overline{OE}	A or B					ns
t_{dis}	\overline{OE}	A or B					ns

¶ This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

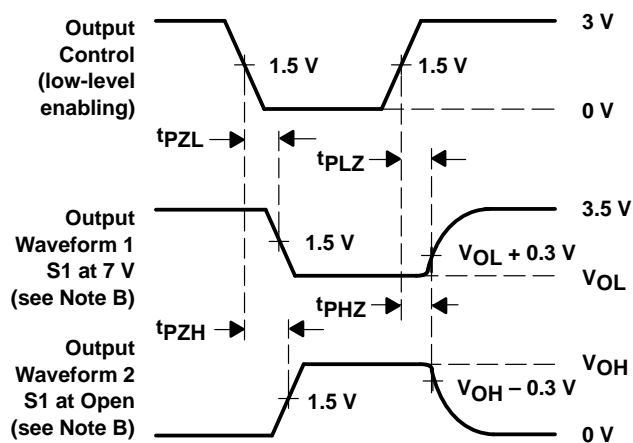
PRODUCT PREVIEW





VOLTAGE WAVEFORMS

PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

- ### Figure 1. Load Circuit and Voltage Waveforms

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