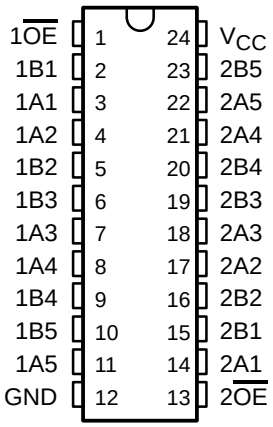
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Designed to Be Used in Level-Shifting Applications**
- **Package Options Include Plastic Shrink Small-Outline (DB), Small-Outline (DW), Thin Shrink Small-Outline (PW), Ceramic DIP (JT), and Ceramic Flat (W) Packages**

SN54CBTD3384 . . . JT OR W PACKAGE
SN74CBTD3384 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



description

The ’CBTD3384 provide ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switches allows connections to be made without adding propagation delay. A diode to V_{CC} is integrated on the die to allow for level shifting between 5-V inputs and 3.3-V outputs.

These devices are organized as two 5-bit switches with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the switch is on and port A is connected to port B. When $\overline{OE}$ is high, the switch is open and a high-impedance state exists between the two ports.

The SN74CBTD3384 is available in TI’s shrink small-outline (DB) and thin shrink small-outline (PW) packages, which provide the same I/O pin count and functionality of standard small-outline packages in less than half the printed circuit board area.

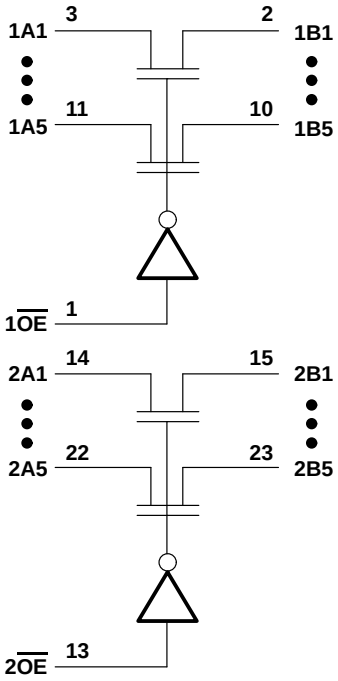
The SN54CBTD3384 is characterized for operation over the full military temperature range from –55°C to 125°C. The SN74CBTD3384 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

$1\overline{OE}$	$2\overline{OE}$	1B1 – 1B5	2B1 – 2B5
L	L	1A1–1A5	2A1–2A5
L	H	1A1–1A5	Z
H	L	Z	2A1–2A5
H	H	Z	Z

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Continuous channel current . . . . . 128 mA
Input clamp current, I_{IK} ($V_{I/O}$ < 0) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package . . . . . 0.65 W
DW package . . . . . 1.7 W
PW package . . . . . 0.7 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions

		SN54CBTD3384		SN74CBTD3384		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level control input voltage	2		2		V
V_{IL}	Low-level control input voltage		0.8		0.8	V
T_A	Operating free-air temperature	–55	125	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

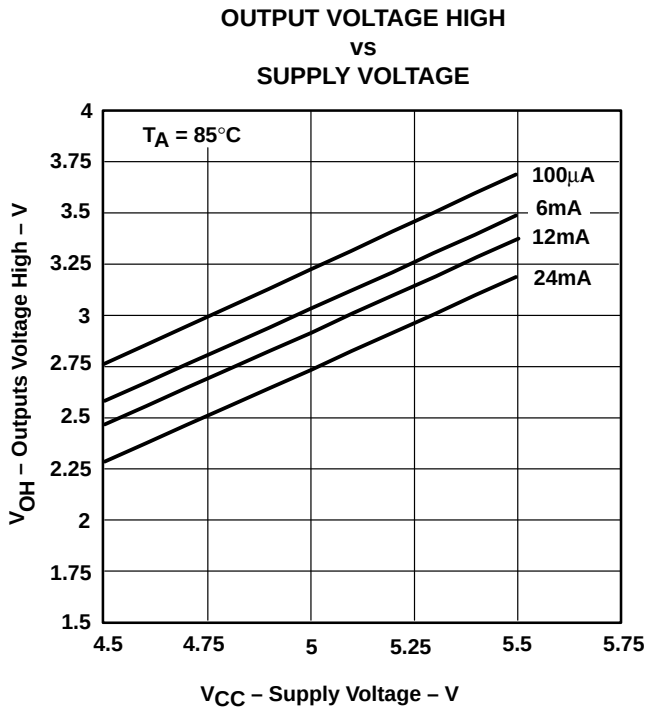
PARAMETER		TEST CONDITIONS			SN54CBTD3384			SN74CBTD3384			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}		See Figure 1									
I_I		V_{CC} = 5.5 V,		V_I = 5.5 V or GND			±1			±1	µA
I_{CC}		V_{CC} = 5.5 V, V_I = V_{CC} or GND		I_O = 0,			1.5			1.5	mA
ΔI_{CC}‡	Control pins	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND		One input at 3.4 V,			2.5			2.5	mA
C_i	Control pins	V_I = 3 V or 0				3			3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,		$\overline{OE}$ = V_{CC}		3.5			3.5		pF
r_{on}§		V_{CC} = 4.5 V	V_I = 0,	I_I = 64 mA		5			5	7	Ω
			V_I = 0,	I_I = 30 mA		5			5	7	
			V_I = 2.4 V,	I_I = 15 mA		35			35	50	

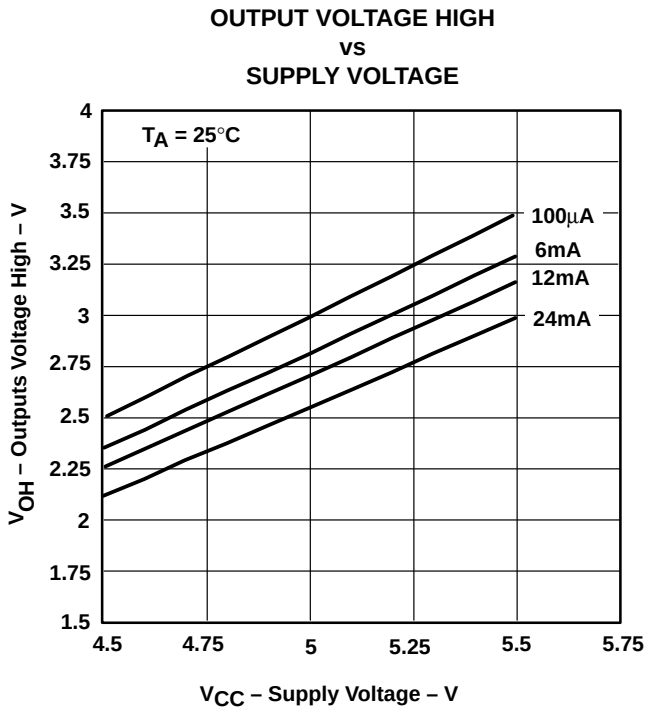
† Typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54CBTD3384		SN74CBTD3384		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A		0.25		0.25	ns
t_{en}	$\overline{OE}$	A or B	2.2	7.2	2.3	7	ns
t_{dis}	$\overline{OE}$	A or B	1.6	5.5	1.7	5.3	ns

¶ This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).





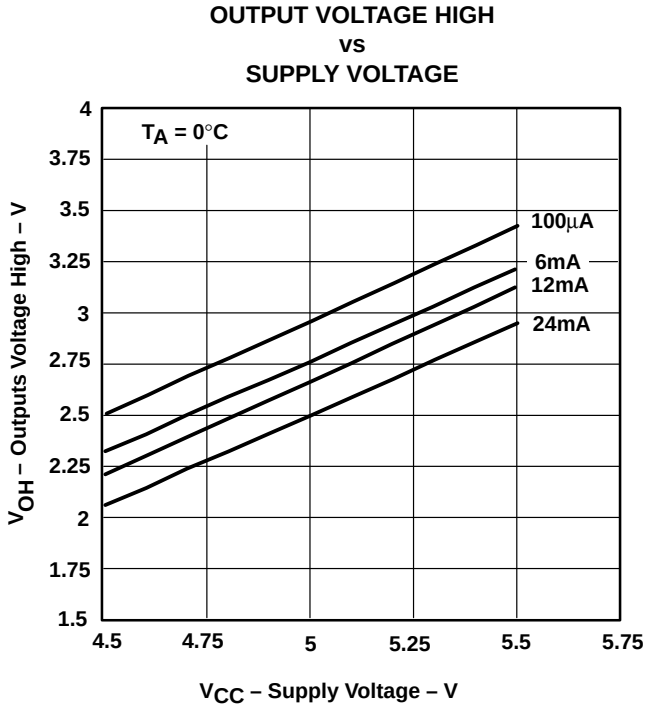
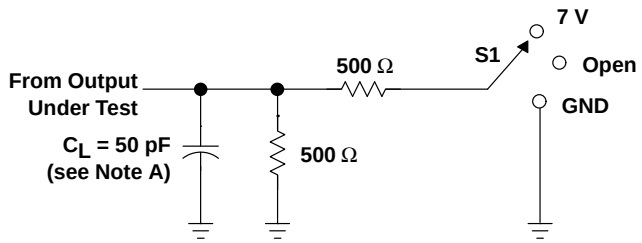


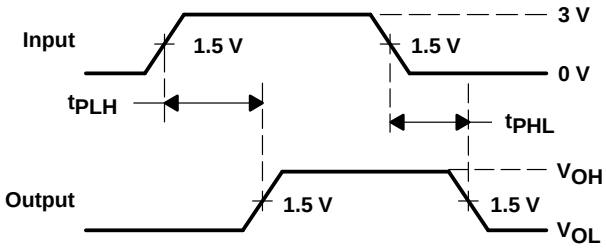
Figure 1. V_{OH} Values

PARAMETER MEASUREMENT INFORMATION

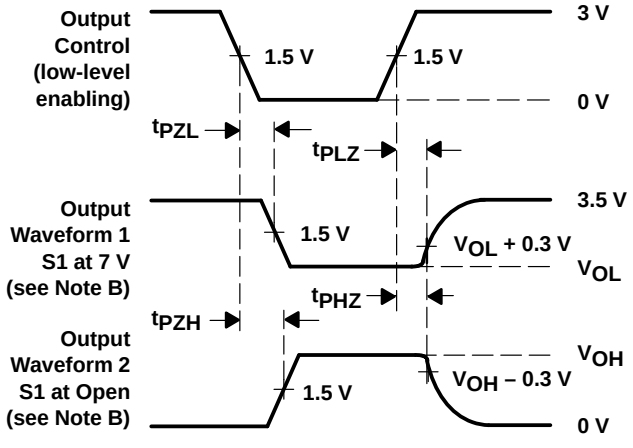


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

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