

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input and Output Levels
- Package Options Include Plastic Thin Shrink Small-Outline (DGG) and 300-mil Shrink Small-Outline (DL) Packages

description

The SN74CBT16211 provides 24 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device operates as a 12- or 24-bit bus switch. When $\overline{1OE}$ is low, 1A is connected to 1B. When $\overline{2OE}$ is low, 2A is connected to 2B.

The SN74CBT16211 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

| INPUTS | | INPUTS/OUTPUTS | |
|------------------|------------------|----------------|---------|
| $\overline{1OE}$ | $\overline{2OE}$ | 1A, 1B | 2A, 2B |
| L | L | 1A = 1B | 2A = 2B |
| L | H | 1A = 1B | Z |
| H | L | Z | 2A = 2B |
| H | H | Z | Z |

DGG OR DL PACKAGE
(TOP VIEW)

| | | | |
|-----------------|----|----|------------------|
| NC | 1 | 56 | $\overline{1OE}$ |
| 1A1 | 2 | 55 | $\overline{2OE}$ |
| 1A2 | 3 | 54 | 1B1 |
| 1A3 | 4 | 53 | 1B2 |
| 1A4 | 5 | 52 | 1B3 |
| 1A5 | 6 | 51 | 1B4 |
| 1A6 | 7 | 50 | 1B5 |
| GND | 8 | 49 | GND |
| 1A7 | 9 | 48 | 1B6 |
| 1A8 | 10 | 47 | 1B7 |
| 1A9 | 11 | 46 | 1B8 |
| 1A10 | 12 | 45 | 1B9 |
| 1A11 | 13 | 44 | 1B10 |
| 1A12 | 14 | 43 | 1B11 |
| 2A1 | 15 | 42 | 1B12 |
| 2A2 | 16 | 41 | 2B1 |
| V _{CC} | 17 | 40 | 2B2 |
| 2A3 | 18 | 39 | 2B3 |
| GND | 19 | 38 | GND |
| 2A4 | 20 | 37 | 2B4 |
| 2A5 | 21 | 36 | 2B5 |
| 2A6 | 22 | 35 | 2B6 |
| 2A7 | 23 | 34 | 2B7 |
| 2A8 | 24 | 33 | 2B8 |
| 2A9 | 25 | 32 | 2B9 |
| 2A10 | 26 | 31 | 2B10 |
| 2A11 | 27 | 30 | 2B11 |
| 2A12 | 28 | 29 | 2B12 |

NC – No internal connection



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**TEXAS
INSTRUMENTS**

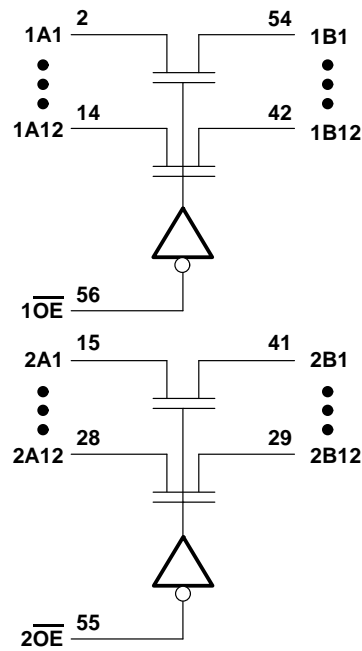
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SN74CBT16211
24-BIT BUS SWITCH

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logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to 7 V |
| Continuous channel current | 128 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | –50 mA |
| Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DGG package | 1 W |
| DL package | 1.4 W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions

| | MIN | MAX | UNIT |
|---|-----|-----|------|
| V_{CC} Supply voltage | 4 | 5.5 | V |
| V_{IH} High-level control input voltage | 2 | | V |
| V_{IL} Low-level control input voltage | | 0.8 | V |
| T_A Operating free-air temperature | –40 | 85 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT | |
|-----------------------|--------------|----------------------------|-----------------------------------|---|------|------|------|---|
| V _{IK} | | V _{CC} = 4.5 V, | I _I = −18 mA | | | −1.2 | V | |
| I _I | | V _{CC} = 0 V, | V _I = 5.5 V | | | 10 | μA | |
| | | V _{CC} = 5.5 V, | V _I = 5.5 V or GND | | | ±1 | | |
| I _{CC} ‡ | | V _{CC} = 5.5 V, | I _O = 0, | V _I = V _{CC} or GND | | 3 | μA | |
| ΔI _{CC} | Control pins | V _{CC} = 5.5 V, | One input at 3.4 V, | Other inputs at V _{CC} or GND | | 2.5 | mA | |
| C _i | Control pins | V _I = 3 V or 0 | | | | 4.5 | pF | |
| C _{io} (OFF) | | V _O = 3 V or 0, | \overline{OE} = V _{CC} | | | 5.5 | pF | |
| r _{on} § | | V _{CC} = 4 V, | V _I = 2.4 V, | I _I = 15 mA | | 14 | 20 | Ω |
| | | V _{CC} = 4.5 V | V _I = 0, | I _I = 64 mA | | 5 | 7 | |
| | | | V _I = 0, | I _I = 30 mA | | 5 | 7 | |
| | | | V _I = 2.4 V, | I _I = 15 mA | | 8 | 12 | |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ | | $V_{CC} = 4\text{ V}$ | | UNIT |
|--------------------|-----------------|-------------|--|------|-----------------------|------|------|
| | | | MIN | MAX | MIN | MAX | |
| t_{pd}^\parallel | A or B | B or A | | 0.25 | | 0.25 | ns |
| t_{en} | \overline{OE} | A or B | 3.9 | 9.3 | | 10.1 | ns |
| t_{dis} | \overline{OE} | A or B | 3.3 | 8.5 | | 7.1 | ns |

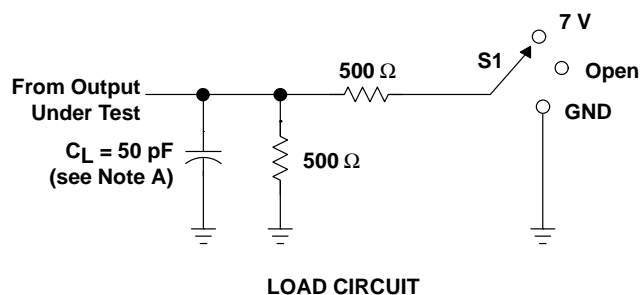
¶ This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

SN74CBT16211

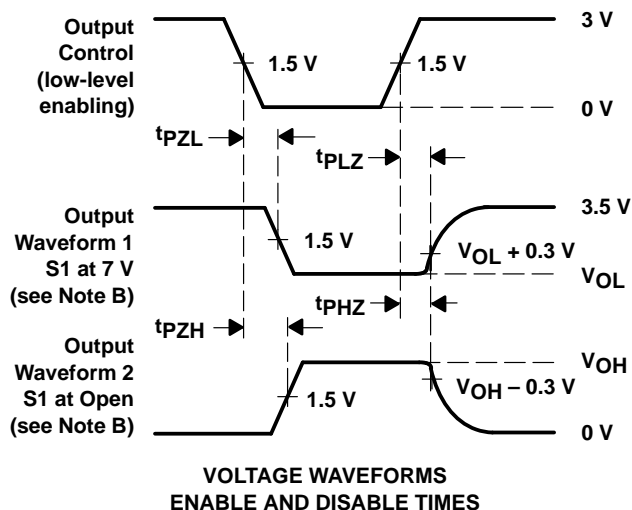
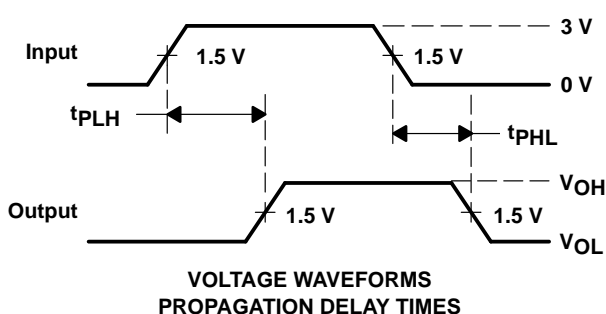
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PARAMETER MEASUREMENT INFORMATION



| TEST | S1 |
|-------------------|------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | 7 V |
| t_{PHZ}/t_{PZH} | Open |



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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