

SN74ALVCH16271 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES017 – JULY 1995

- Member of the Texas Instruments **Widebus™** Family
- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 12-bit to 24-bit bus exchanger is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16271 is intended for applications where two separate datapaths must be multiplexed onto, or demultiplexed from, a single datapath. This device is particularly suitable as an interface between conventional DRAMs and high-speed microprocessors.

A data is stored in the internal A-to-B registers on the low-to-high transition of the clock (CLK) input, provided that the \overline{CLKENA} inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port.

Transparent latches in the B-to-A path allow asynchronous operation in order to maximize memory access throughput. These latches transfer data when the latch-enable (\overline{LE}) inputs are low. The select (\overline{SEL}) line selects 1B or 2B data for the A outputs. Data flow is controlled by the active-low output enables ($\overline{OE_A}$, $\overline{OE_B}$).

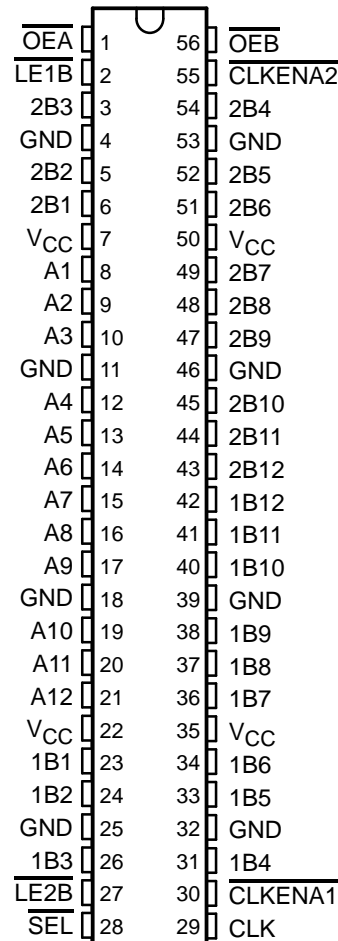
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16271 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16271 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW



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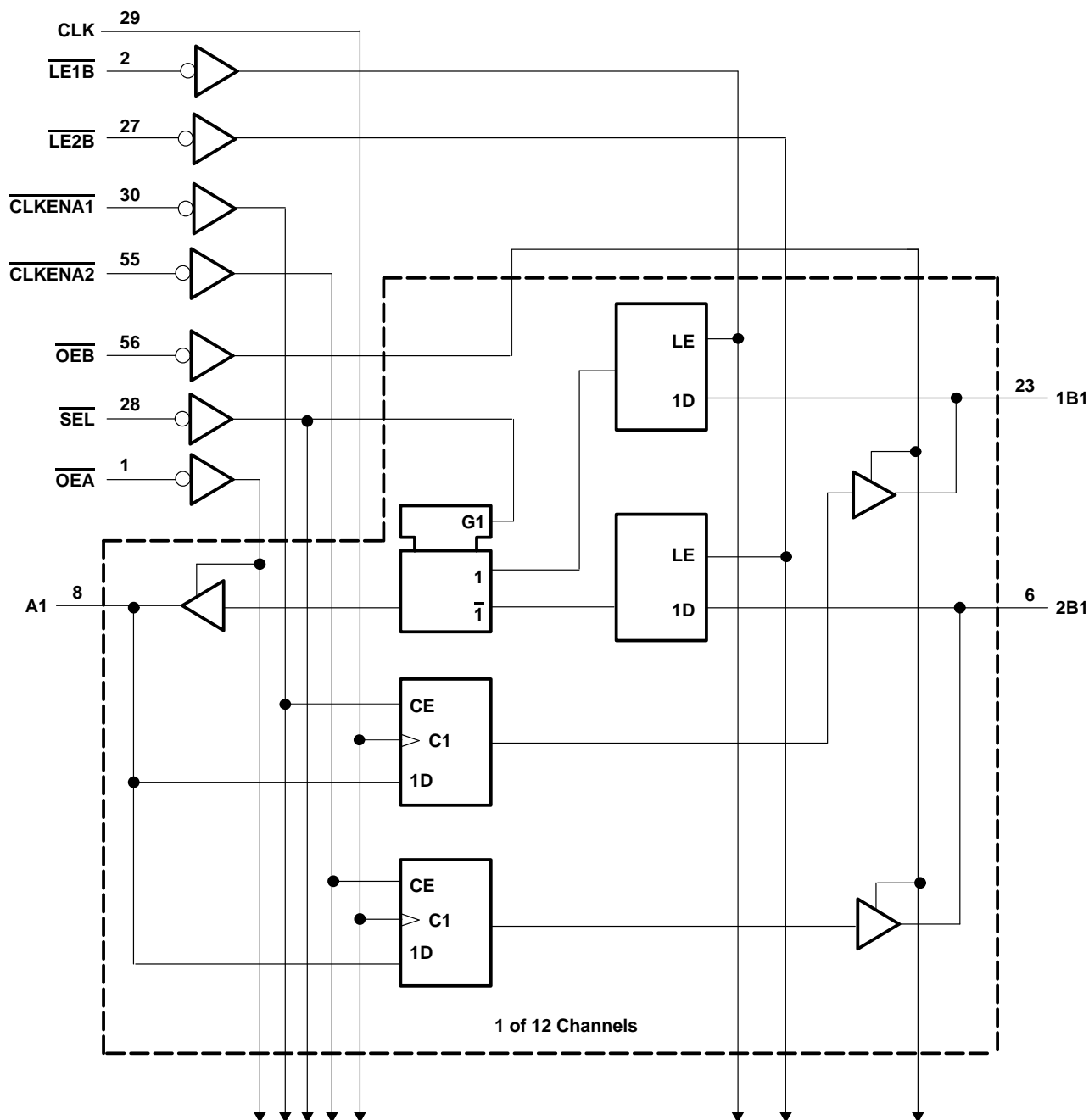
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logic diagram (positive logic)



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Function Tables

OUTPUT ENABLE

INPUTS		OUTPUTS	
$\overline{OE}A$	$\overline{OE}B$	A	1B, 2B
H	H	Z	Z
H	L	Z	Active
L	H	Active	Z
L	L	Active	Active

A-TO-B STORAGE ($\overline{OE}B = L$)

INPUTS				OUTPUTS	
$\overline{CLKENA}1$	$\overline{CLKENA}2$	CLK	A	1B	2B
H	H	X	X	1B ₀ [†]	2B ₀ [†]
L	X	↑	L	L	X
L	X	↑	H	H	X
X	L	↑	L	X	L
X	L	↑	H	A ₀	H

B-TO-A STORAGE ($\overline{OE}A = L$)

INPUTS				OUTPUT
\overline{LE}	\overline{SEL}	1B	2B	A
H	X	X	X	A ₀ [†]
H	X	X	X	A ₀ [†]
L	H	L	X	L
L	H	H	X	H
L	L	X	L	L
L	L	X	H	H

[†] Output level before the indicated steady-state input conditions were established

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I : Except I/O ports (see Note 1)	–0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, T_{stg}	–65°C to 150°C

[‡] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.



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recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2.3	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7		V
		V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7	V
		V _{CC} = 2.7 V to 3.6 V		0.8	
V _I	Input voltage		0	V _{CC}	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.3 V		−12	mA
		V _{CC} = 2.7 V		−12	
		V _{CC} = 3 V		−24	
I _{OL}	Low-level output current	V _{CC} = 2.3 V		12	mA
		V _{CC} = 2.7 V		12	
		V _{CC} = 3 V		24	
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
T _A	Operating free-air temperature		−40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC} [†]	MIN	TYP [‡]	MAX	UNIT
V _{OH}	I _{OH} = −100 μA		MIN to MAX	V _{CC} − 0.2		V	
	I _{OH} = −6 mA, V _{IH} = 1.7 V		2.3 V	2			
	I _{OH} = −12 mA	V _{IH} = 1.7 V	2.3 V	1.7			
		V _{IH} = 2 V	2.7 V	2.2			
		V _{IH} = 2 V	3 V	2.4			
	I _{OH} = −24 mA, V _{IH} = 2 V		3 V	2			
V _{OL}	I _{OL} = 100 μA		MIN to MAX	0.2		V	
	I _{OL} = 6 mA, V _{IL} = 0.7 V		2.3 V	0.4			
	I _{OL} = 12 mA	V _{IL} = 0.7 V	2.3 V	0.7			
		V _{IL} = 0.8 V	2.7 V	0.4			
	I _{OL} = 24 mA, V _{IL} = 0.8 V		3 V	0.55			
I _I	V _I = V _{CC} or GND		3.6 V	±5		μA	
I _I (hold)	V _I = 0.7 V		2.3 V	45		μA	
	V _I = 1.7 V			−45			
	V _I = 0.8 V		3 V	75			
	V _I = 2 V			−75			
	V _I = 0 to 3.6 V		3.6 V	±500			
I _{OZ} [§]		V _O = V _{CC} or GND		3.6 V	±10		μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0		3.6 V	40		μA
ΔI _{CC}		One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		3 V to 3.6 V	750		μA
C _i	Control inputs	V _I = V _{CC} or GND		3.3 V			pF
C _{io}	A or B ports	V _O = V _{CC} or GND		3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

[§] For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW



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