

SN74ALVCH16501

18-BIT UNIVERSAL BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

SCES024 – JULY 1995

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- *UBT™* (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit universal bus transceiver is designed for 2.3-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable (OEAB and \overline{OEBA}), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OEBA} should be tied to V_{CC} through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

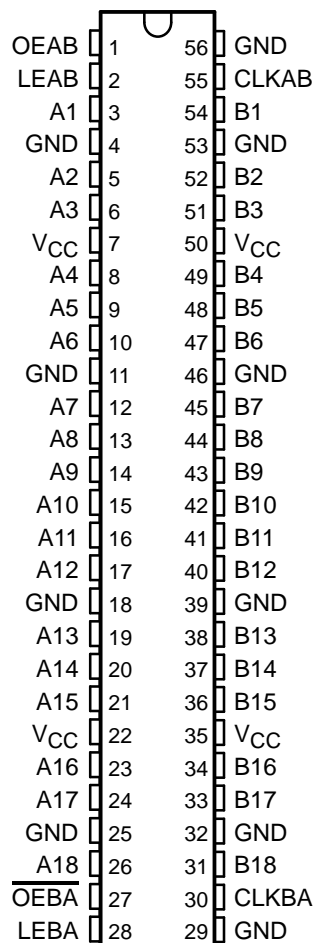
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Data flow for B to A is similar to that of A to B but uses \overline{OEBA} , LEBA, and CLKBA. The output enables are complementary (OEAB is active high and \overline{OEBA} is active low).

The SN74ALVCH16501 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16501 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



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FUNCTION TABLE†

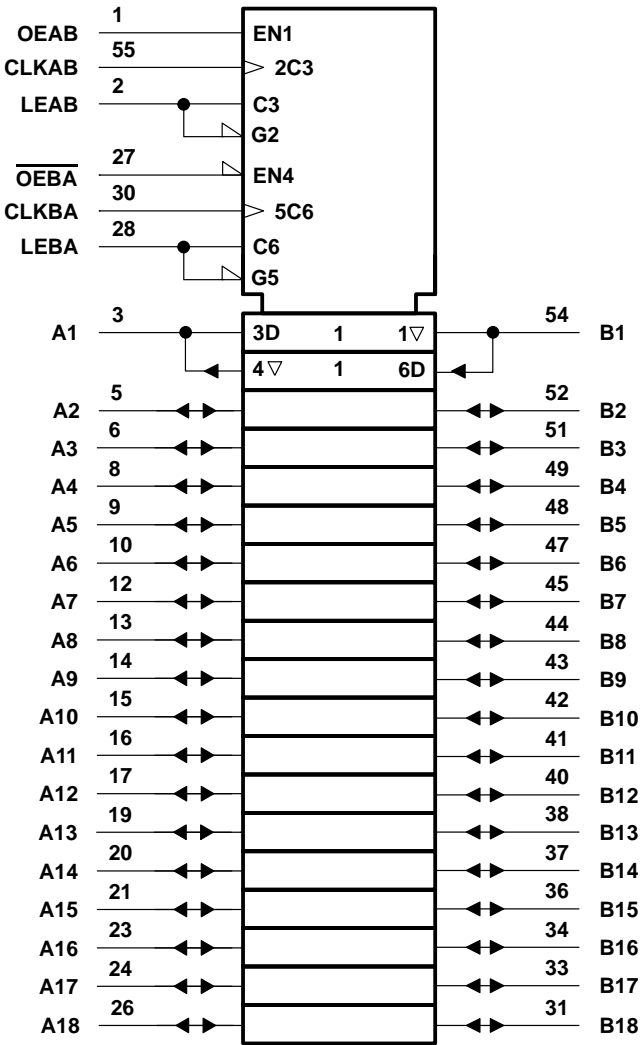
INPUTS				OUTPUT B
OEAB	LEAB	CLKAB	A	
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B ₀ ‡
H	L	L	X	B ₀ §

† A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB is high before LEAB goes low

§ Output level before the indicated steady-state input conditions were established

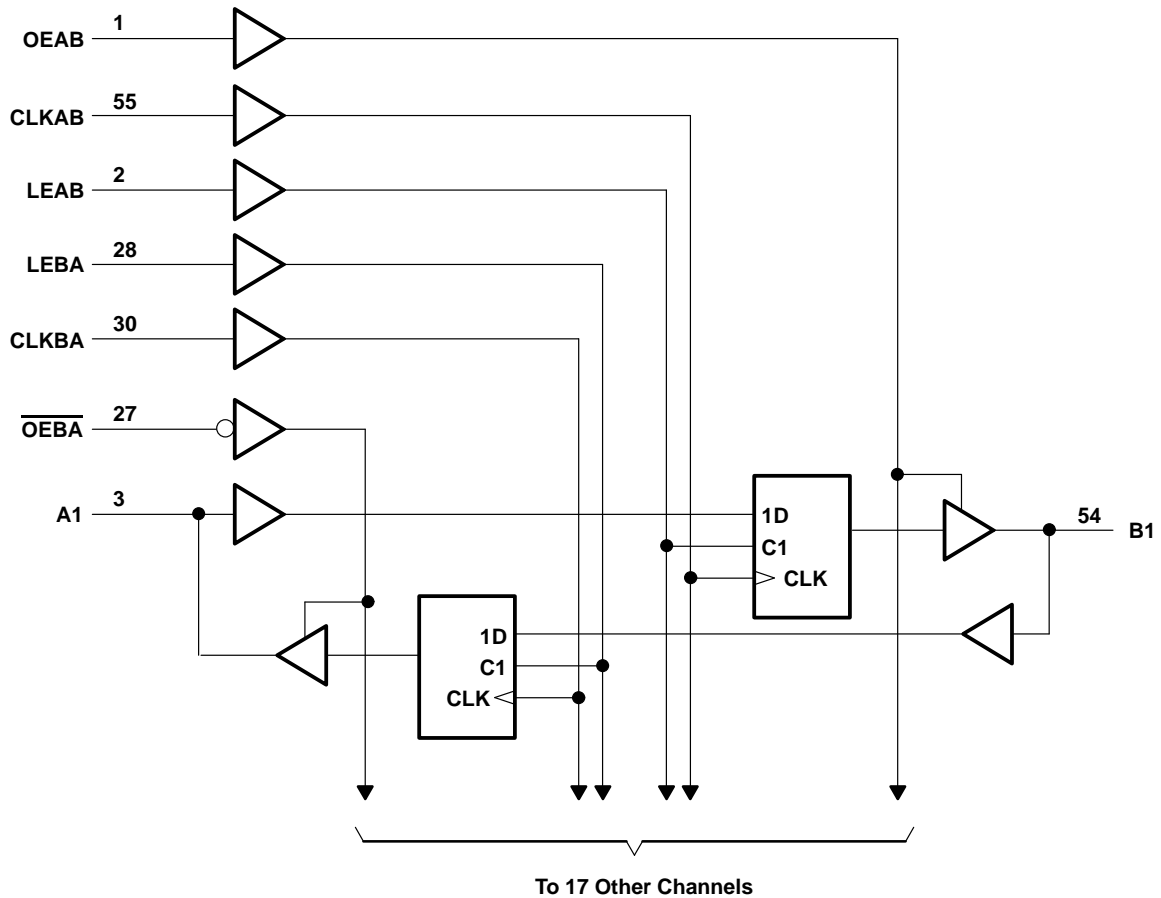
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I : Except I/O ports (see Note 1)	–0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

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recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2.3	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7		V
		V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7	V
		V _{CC} = 2.7 V to 3.6 V		0.8	
V _I	Input voltage		0	V _{CC}	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.3 V		−12	mA
		V _{CC} = 2.7 V		−12	
		V _{CC} = 3 V		−24	
I _{OL}	Low-level output current	V _{CC} = 2.3 V		12	mA
		V _{CC} = 2.7 V		12	
		V _{CC} = 3 V		24	
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
T _A	Operating free-air temperature		−40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC} [†]	MIN	TYP [‡]	MAX	UNIT
V _{OH}	I _{OH} = −100 μA		MIN to MAX	V _{CC} − 0.2			V
	I _{OH} = −6 mA, V _{IH} = 1.7 V		2.3 V	2			
	I _{OH} = −12 mA	V _{IH} = 1.7 V	2.3 V	1.7			
		V _{IH} = 2 V	2.7 V	2.2			
		V _{IH} = 2 V	3 V	2.4			
I _{OH} = −24 mA, V _{IH} = 2 V		3 V	2				
V _{OL}	I _{OL} = 100 μA		MIN to MAX			0.2	V
	I _{OL} = 6 mA, V _{IL} = 0.7 V		2.3 V			0.4	
	I _{OL} = 12 mA	V _{IL} = 0.7 V	2.3 V			0.7	
		V _{IL} = 0.8 V	2.7 V			0.4	
	I _{OL} = 24 mA, V _{IL} = 0.8 V		3 V			0.55	
I _I	V _I = V _{CC} or GND		3.6 V			±5	μA
I _I (hold)	V _I = 0.7 V		2.3 V	45			μA
	V _I = 1.7 V			−45			
	V _I = 0.8 V		3 V	75			
	V _I = 2 V			−75			
	V _I = 0 to 3.6 V		3.6 V			±500	
I _{OZ} [§]	V _O = V _{CC} or GND		3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0		3.6 V			40	μA
ΔI _{CC}	One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		3 V to 3.6 V			750	μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	4			pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V	8			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[§] For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		0	150	0	150	0	150	MHz
t _w	Pulse duration	LE high	3.3		3.3		3.3		ns
		CLK high or low	3.3		3.3		3.3		
t _{su}	Setup time	Data before CLK [↑]	2.2		2.1		1.7		ns
		Data before LE [↓] , CLK high	1.9		1.6		1.5		
		Data before LE [↓] , CLK low	1.3		1.1		1		
t _h	Hold time	Data after CLK [↑]	0.6		0.6		0.7		ns
		Data after LE [↓] , CLK high or low	1.4		1.7		1.4		



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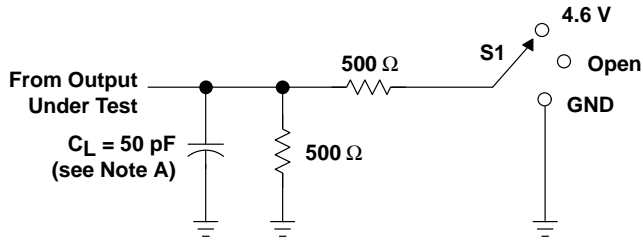
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{\max}			150		150		150		MHz
t_{pd}	A or B	B or A	1.2	5.4	4.5		1	3.9	ns
	LE	A or B	1.6	6.3	5.3		1.3	4.6	
	CLK	A or B	1.7	6.7	5.6		1.4	4.9	
t_{en}	OEAB	B	1.1	6.3	5.3		1	4.6	ns
t_{dis}	OEAB	B	2.2	6.4	5.7		1.4	5	ns
t_{en}	$\overline{\text{OEBA}}$	A	1.4	6.8	6		1.1	5	ns
t_{dis}	$\overline{\text{OEBA}}$	A	2	5.5	4.6		1.3	4.2	ns

operating characteristics, $T_A = 25^\circ\text{C}$

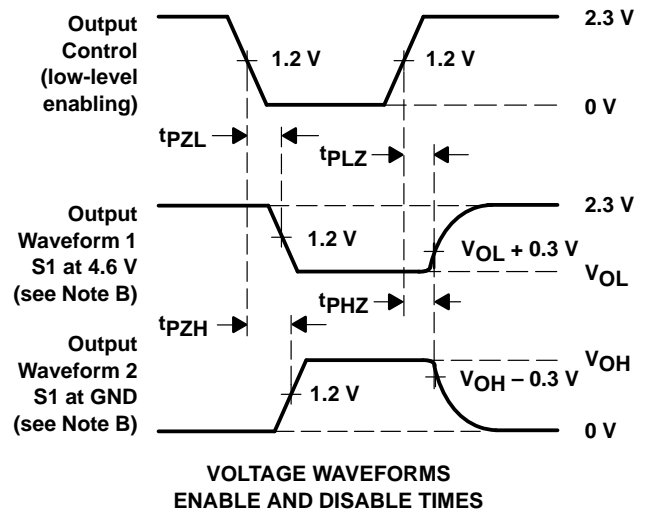
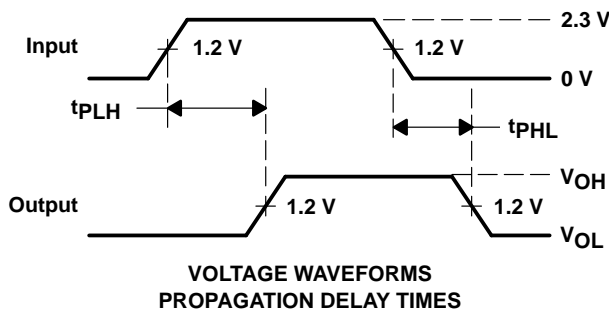
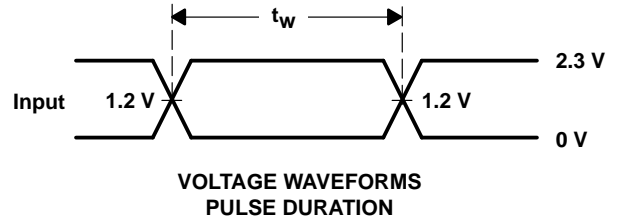
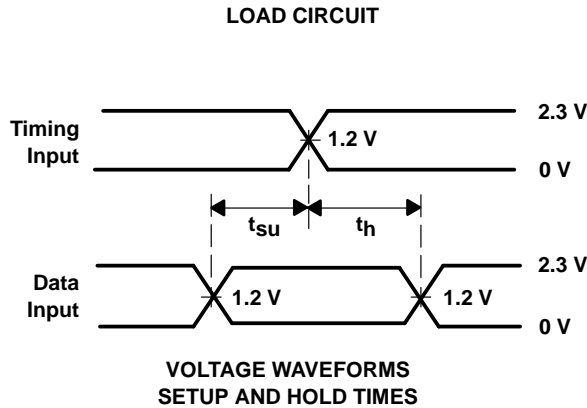
PARAMETER			TEST CONDITIONS	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}, f = 10\text{ MHz}$	44	54	pF
		Outputs disabled		6	6	

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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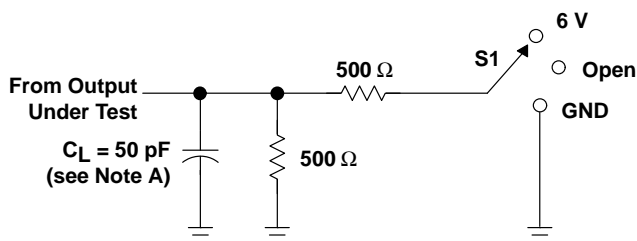
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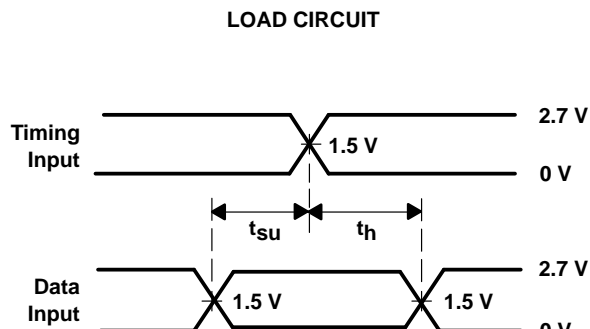
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

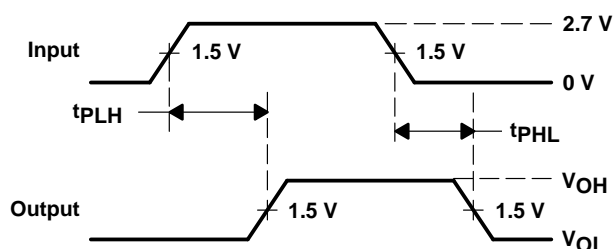


LOAD CIRCUIT

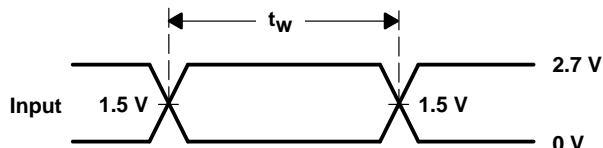
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



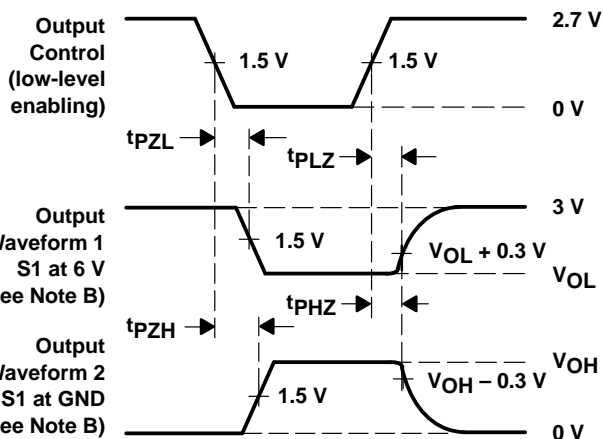
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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