

SN74ALVCH16841

20-BIT BUS-INTERFACE D-TYPE LATCH

WITH 3-STATE OUTPUTS

SCES043 – JULY 1995

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 20-bit bus-interface D-type latch is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16841 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, unidirectional bus drivers, and working registers.

The SN74ALVCH16841 can be used as two 10-bit latches or one 20-bit latch. The 20 latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the D inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($\overline{1OE}$ or $\overline{2OE}$) input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

The output-enable (\overline{OE}) input does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

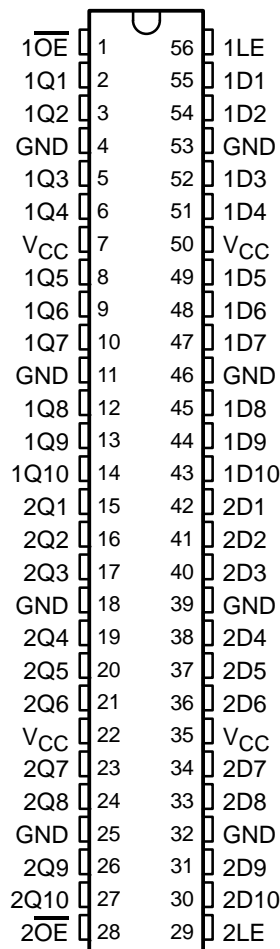
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN74ALVCH16841 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16841 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



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INSTRUMENTS**

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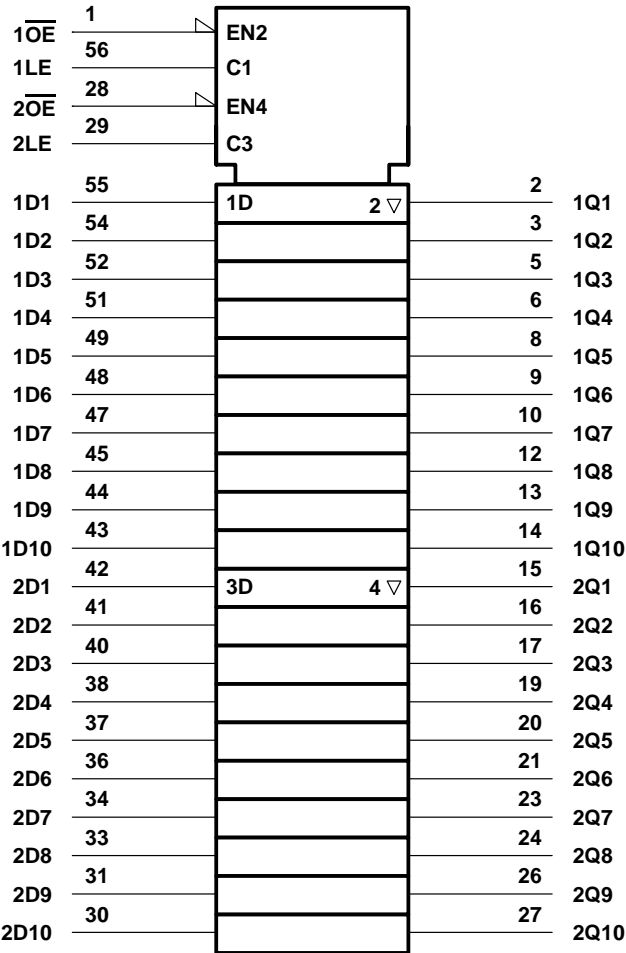
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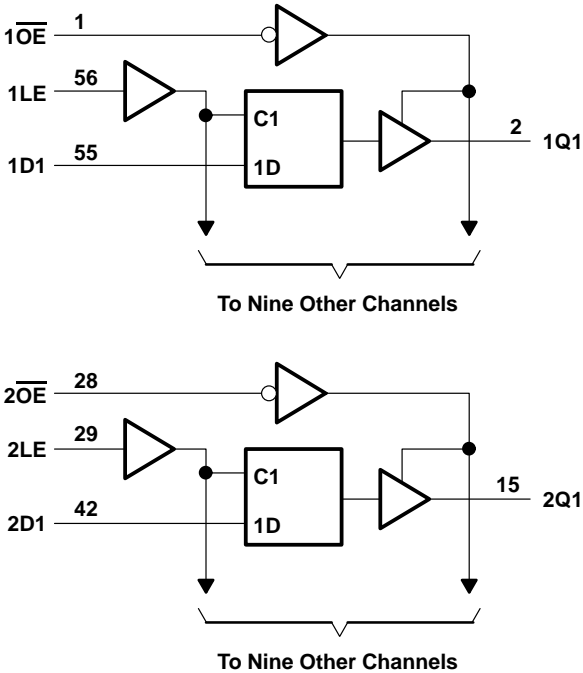
FUNCTION TABLE
(each 10-bit latch)

INPUTS			OUTPUT Q
\overline{OE}	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.3$ V to 2.7 V	1.7		V
		$V_{CC} = 2.7$ V to 3.6 V	2		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3$ V to 2.7 V		0.7	V
		$V_{CC} = 2.7$ V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.3$ V		–12	mA
		$V_{CC} = 2.7$ V		–12	
		$V_{CC} = 3$ V		–24	
I_{OL}	Low-level output current	$V_{CC} = 2.3$ V		12	mA
		$V_{CC} = 2.7$ V		12	
		$V_{CC} = 3$ V		24	
$\Delta t / \Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V _{CC} [†]	MIN	TYP [‡]	MAX	UNIT	
V _{OH}	I _{OH} = −100 μA		MIN to MAX		V _{CC} − 0.2			V	
	I _{OH} = −6 mA, V _{IH} = 1.7 V		2.3 V		2				
	I _{OH} = −12 mA	V _{IH} = 1.7 V	2.3 V		1.7				
		V _{IH} = 2 V	2.7 V		2.2				
		V _{IH} = 2 V	3 V		2.4				
	I _{OH} = −24 mA, V _{IH} = 2 V		3 V		2				
V _{OL}	I _{OL} = 100 μA		MIN to MAX				0.2	V	
	I _{OL} = 6 mA, V _{IL} = 0.7 V		2.3 V				0.4		
	I _{OL} = 12 mA	V _{IL} = 0.7 V	2.3 V				0.7		
		V _{IL} = 0.8 V	2.7 V				0.4		
	I _{OL} = 24 mA, V _{IL} = 0.8 V		3 V				0.55		
I _I	V _I = V _{CC} or GND		3.6 V				±5	μA	
I _I (hold)	V _I = 0.7 V		2.3 V		45			μA	
	V _I = 1.7 V				−45				
	V _I = 0.8 V		3 V		75				
	V _I = 2 V				−75				
	V _I = 0 to 3.6 V		3.6 V				±500		
I _{OZ}	V _O = V _{CC} or GND		3.6 V				±10	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0		3.6 V				40	μA	
ΔI _{CC}		One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		3 V to 3.6 V				750	μA
C _i	Control inputs	V _I = V _{CC} or GND		3.3 V		3		pF	
	Data inputs					6			
C _O	Outputs	V _O = V _{CC} or GND		3.3 V		7		pF	

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

‡ Typical values are measured at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, (unless otherwise noted) (see Figures 1 and 2)

PARAMETER		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high or low	3.3		3.3		3.3		ns
t_{su}	Setup time, data before LE \uparrow	0.9		0.7		1.1		ns
t_h	Hold time, data after LE \uparrow	1.2		1.5		1.1		ns

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	1.1	5.6	4.7		1.2	3.9	ns
	LE	Q	1	6.2	5.1		1	4.3	
t_{en}	\overline{OE}	Q	1	6.7	6		1	4.9	ns
t_{dis}	\overline{OE}	Q	1.8	5.5	4.3		1.3	4.1	ns



operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
			TYP	TYP	
C_{pd} Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}, \quad f = 10\text{ MHz}$	12	20	pF
	Outputs disabled		1	3	

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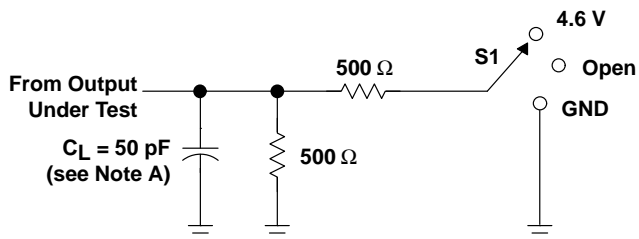
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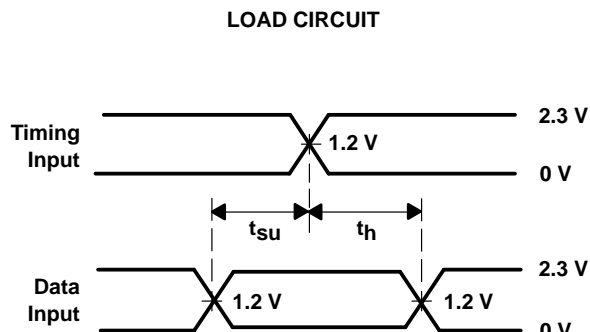
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

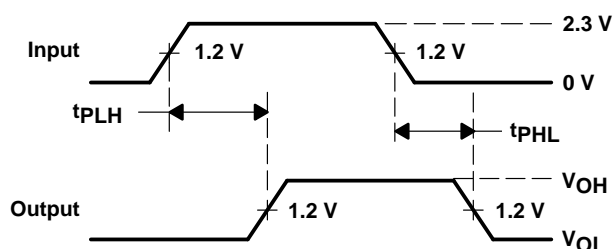


LOAD CIRCUIT

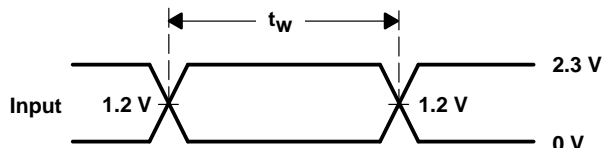
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND



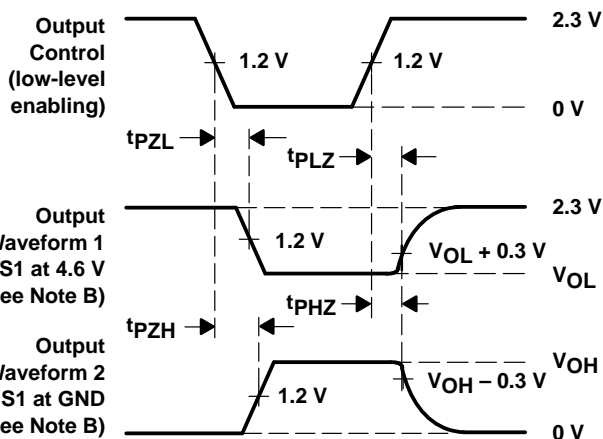
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

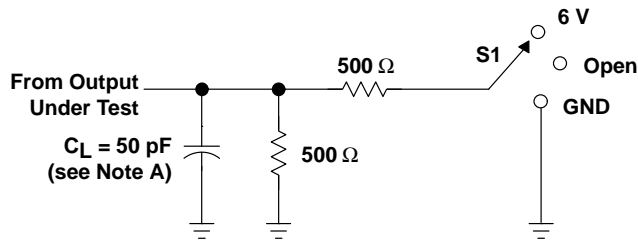


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

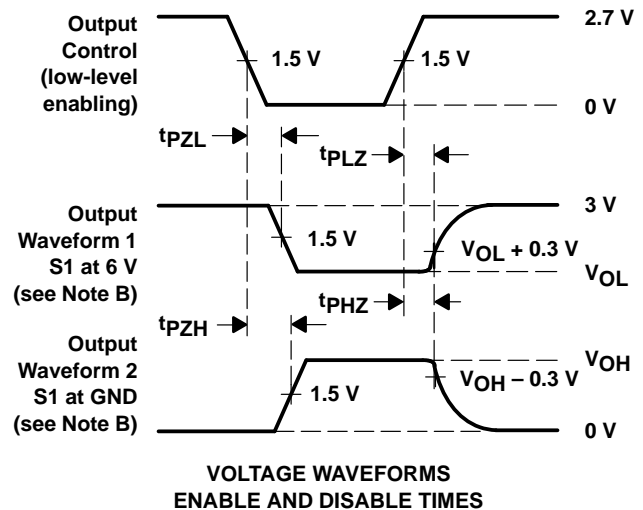
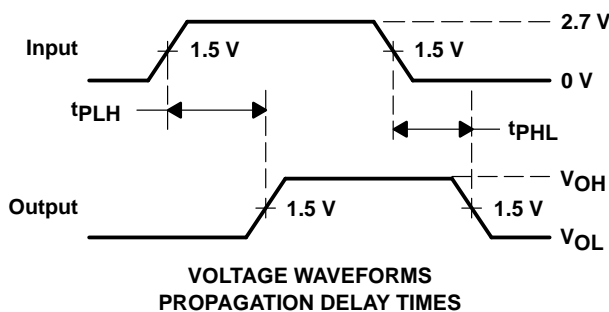
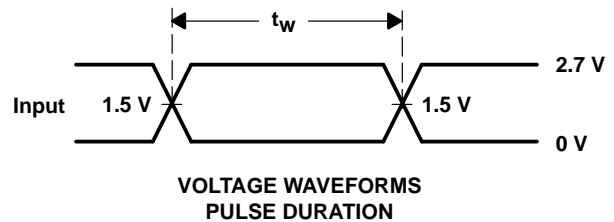
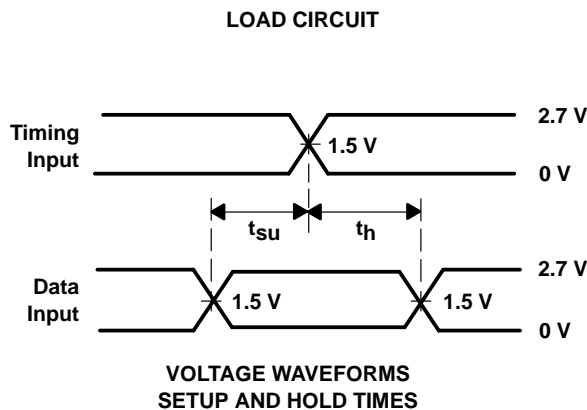
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.7\text{ V}$ AND $3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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