

SN74ALVCH162525

18-BIT REGISTERED BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

SCES058 – NOVEMBER 1995

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- B-Port Outputs Have Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Option Includes Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit universal bus transceiver is designed for 2.3-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}), and clock enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For the A-to-B data flow, the data flows through a single register. The B-to-A data can flow through a four-stage pipeline register path, or through a single register path, depending on the state of \overline{SEL} .

Data is stored in the internal registers on the low-to-high transition of the CLK input, provided that the appropriate \overline{CLKEN} inputs are low. The A-to-B data transfer is synchronized to the CLKAB input, and B-to-A data transfer is synchronized with the CLK1BA and CLK2BA inputs.

The B outputs, which are designed to sink up to 12 mA, include 26- Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162525 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)

$\overline{CLKENAB}$	1	56	\overline{SEL}
\overline{OEAB}	2	55	CLKAB
A1	3	54	B1
GND	4	53	GND
A2	5	52	B2
A3	6	51	B3
V_{CC}	7	50	V_{CC}
A4	8	49	B4
A5	9	48	B5
A6	10	47	B6
GND	11	46	GND
A7	12	45	B7
A8	13	44	B8
A9	14	43	B9
A10	15	42	B10
A11	16	41	B11
A12	17	40	B12
GND	18	39	GND
A13	19	38	B13
A14	20	37	B14
A15	21	36	B15
V_{CC}	22	35	V_{CC}
A16	23	34	B16
A17	24	33	B17
GND	25	32	GND
A18	26	31	B18
\overline{OEBA}	27	30	CLK1BA
$\overline{CLKENBA}$	28	29	CLK2BA



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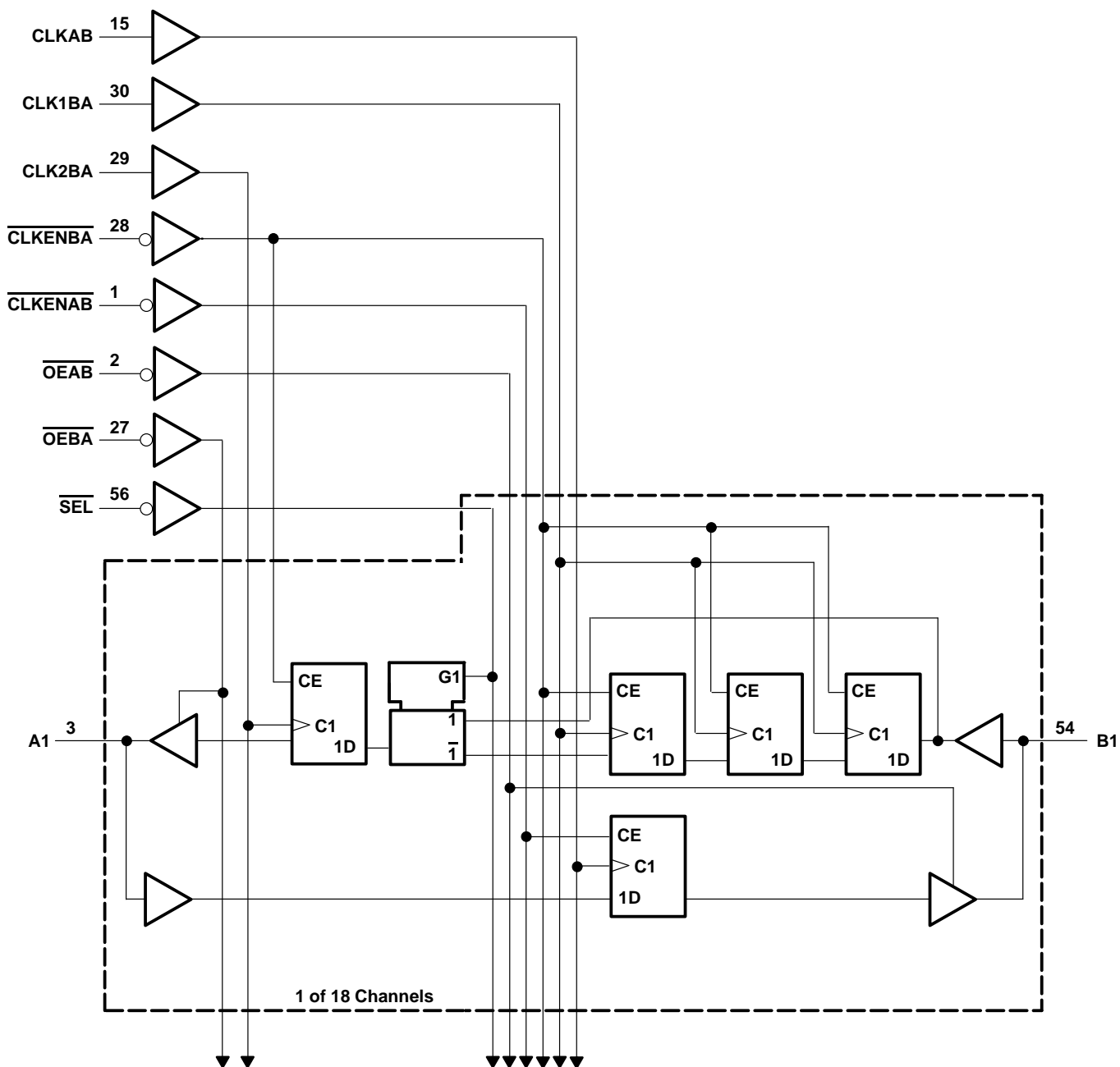
SN74ALVCH162525

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SCES058 – NOVEMBER 1995

logic diagram (positive logic)



Function Tables

A-TO-B STORAGE ($\overline{OEAB} = L$)

INPUTS			OUTPUT
CLKENAB	CLKAB	A	B
H	X	X	B ₀ [†]
L	↑	L	L
L	↑	H	H

B-TO-A STORAGE ($\overline{OEBA} = L$)

INPUTS					OUTPUT
CLKENBA	CLK2BA	CLK1BA	\overline{SEL}	B	A
H	X	X	X	X	A ₀ [†]
L	↑	X	H	L	L
L	↑	X	H	H	H
L	↑	↑	L	L	L [‡]
L	↑	↑	L	H	H [‡]

[†] Output level before the indicated steady-state input conditions were established

[‡] Three CLK1BA edges and one CLK2BA edge are needed to propagate data from B-to-A when \overline{SEL} is low.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[§]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3):	
DGG package	1 W
DL package	1.4 W
Storage temperature range, T_{stg}	–65°C to 150°C

[§] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

SN74ALVCH162525

18-BIT REGISTERED BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

SCES058 – NOVEMBER 1995

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2.3	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
		V _{CC} = 2.3 V to 2.7 V		0.7	
V _I	Input voltage		0	V _{CC}	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current (A port)	V _{CC} = 2.3 V		–12	mA
		V _{CC} = 2.7 V		–12	
		V _{CC} = 3 V		–24	
I _{OL}	Low-level output current (A port)	V _{CC} = 2.3 V		12	mA
		V _{CC} = 2.7 V		12	
		V _{CC} = 3 V		24	
I _{OH}	High-level output current (B port)	V _{CC} = 2.3 V		–6	mA
		V _{CC} = 2.7 V		–8	
		V _{CC} = 3 V		–12	
I _{OL}	Low-level output current (B port)	V _{CC} = 2.3 V		6	mA
		V _{CC} = 2.7 V		8	
		V _{CC} = 3 V		12	
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
T _A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [†]	MIN	TYP [‡]	MAX	UNIT
V _{OH} (A port)	I _{OH} = –100 µA	MIN to MAX	V _{CC} – 0.2			V
	I _{OH} = –6 mA, V _{IH} = 1.7 V	2.3 V	2			
	I _{OH} = –12 mA	V _{IH} = 1.7 V	2.3 V		1.7	
		V _{IH} = 2 V	2.7 V		2.2	
		V _{IH} = 2 V	3 V		2.4	
	I _{OH} = –24 mA, V _{IH} = 2 V	3 V	2			
V _{OH} (B port)	I _{OH} = –100 µA	MIN to MAX	V _{CC} – 0.2			V
	I _{OH} = –4 mA, V _{IH} = 1.7 V	2.3 V	1.9			
	I _{OH} = –6 mA	V _{IH} = 1.7 V	2.3 V		1.7	
		V _{IH} = 2 V	3 V		2.4	
	I _{OH} = –8 mA, V _{IH} = 2 V	2.7 V	2			
	I _{OH} = –12 mA, V _{IH} = 2 V	3 V	2			
V _{OL} (A port)	I _{OL} = 100 µA	MIN to MAX	0.2			V
	I _{OL} = 6 mA, V _{IL} = 0.7 V	2.3 V	0.4			
	I _{OL} = 12 mA	V _{IL} = 0.7 V	2.3 V		0.7	
		V _{IL} = 0.8 V	2.7 V		0.4	
	I _{OL} = 24 mA, V _{IL} = 0.8 V	3 V	0.55			
V _{OL} (B port)	I _{OL} = 100 µA	MIN to MAX	0.2			V
	I _{OL} = 4 mA, V _{IL} = 0.7 V	2.3 V	0.4			
	I _{OL} = 6 mA	V _{IL} = 0.7 V	2.3 V		0.55	
		V _{IL} = 0.8 V	3 V		0.55	
	I _{OL} = 8 mA, V _{IL} = 0.8 V	2.7 V	0.6			
	I _{OL} = 12 mA, V _{IL} = 0.8 V	3 V	0.8			
I _I	V _I = V _{CC} or GND	3.6 V	±5			µA
I _{hold}	V _I = 0.7 V	2.3 V	45			µA
	V _I = 1.7 V		–45			
	V _I = 0.8 V	3 V	75			
	V _I = 2 V		–75			
	V _I = 0 to 3.6 V	3.6 V	±500			
I _{OZ} [§]	V _O = V _{CC} or GND	3.6 V	±10			µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	40			µA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V	750			µA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	3		pF
C _O	A or B ports	V _O = V _{CC} or GND	3.3 V	7		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[§] For I/O ports, the parameter I_{OZ} includes the input leakage current.

SN74ALVCH162525
18-BIT REGISTERED BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

SCES058 – NOVEMBER 1995

timing requirements over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V _{CC} = 2.5 V ±0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	0	120	0	125	0	150	MHz
t _w	Pulse duration, CLK high or low	3.2		3.2		3		ns
t _{su}	A data before CLKAB↑	1.3		1.3		1.3		ns
	B data before CLK2BA↑	2.1		1.8		1.7		
	B data before CLK1BA↑	1.3		1.2		1.1		
	SEL before CLK2BA↑	3.3		3.3		3.3		
	CLKENAB before CLKAB↑	2.1		1.9		1.6		
	CLKENBA before CLK1BA↑	2.7		2.5		2.1		
	CLKENBA before CLK2BA↑	2.7		2.5		2.2		
t _h	A data after CLKAB↑	0.7		0.4		0.9		ns
	B data after CLK2BA↑	0.4		0		0.6		
	B data after CLK1BA↑	0.8		0.4		1		
	SEL after CLK2BA↑	0		0		0.1		
	CLKENAB after CLKAB↑	0.1		0.3		0.3		
	CLKENBA after CLK1BA↑	0		0		0.1		
	CLKENBA after CLK2BA↑	0		0		0		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

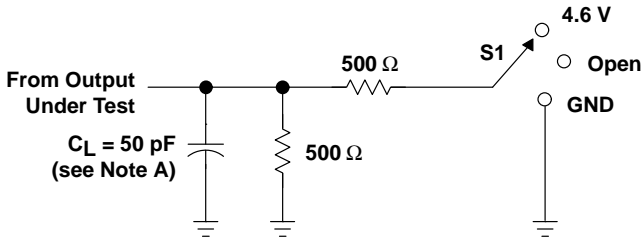
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			120		125		150		MHz
t _{pd}	CLKAB	B	1	6.1		5.4	1	4.7	ns
	CLK2BA	A	1	5.1		4.4	1	4.2	
t _{en}	OEBA	A	1	6.6		6.1	1	5.1	ns
	OEAB	B	1	7.2		6.8	1	5.7	
t _{dis}	OEBA	A	1	6.5		5.4	1	4.9	ns
	OEAB	B	1	6.5		5.4	1	4.9	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
			TYP	TYP	
C _{pd}	Power dissipation capacitance	C _L = 50 pF, f = 10 MHz	160	160	pF
	Outputs enabled				
	Outputs disabled				

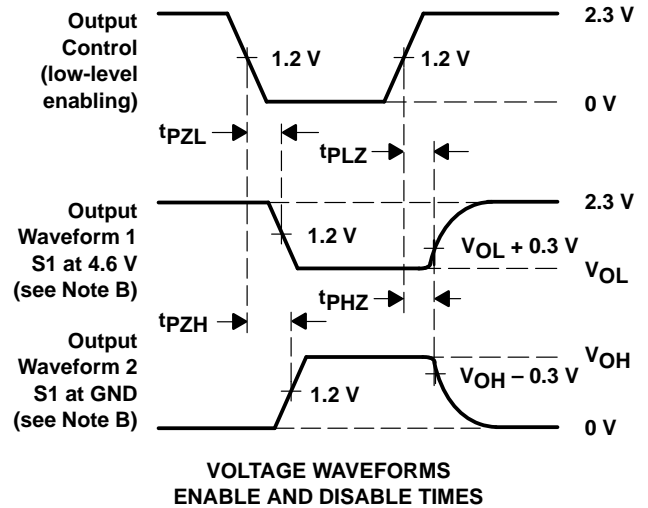
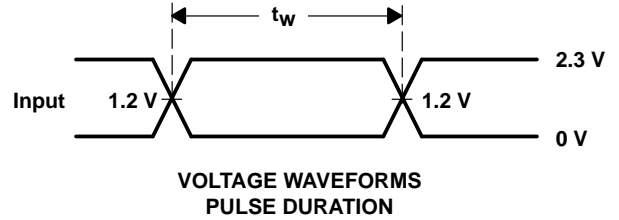
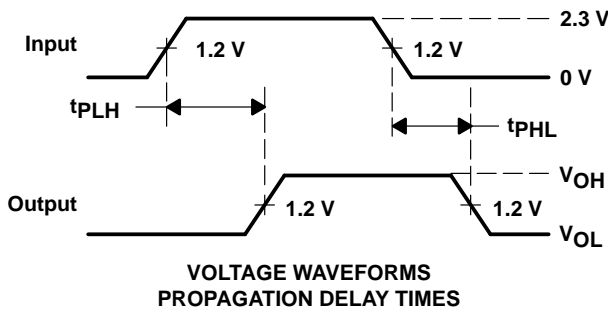
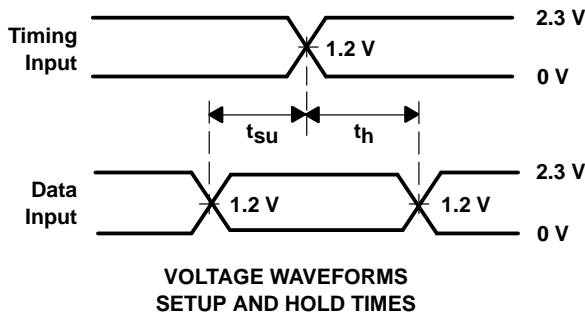


PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74ALVCH162525

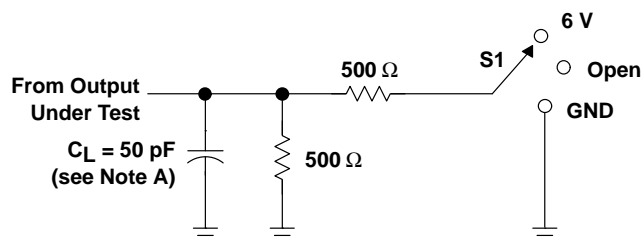
18-BIT REGISTERED BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

SCES058 – NOVEMBER 1995

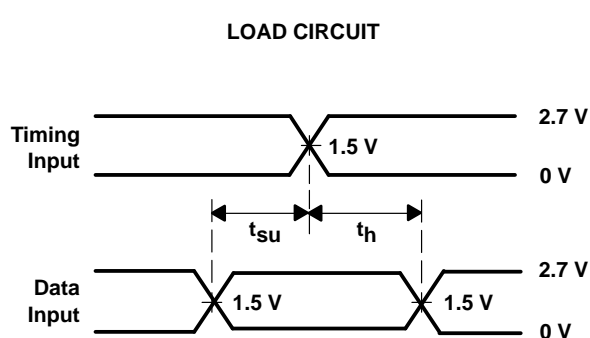
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

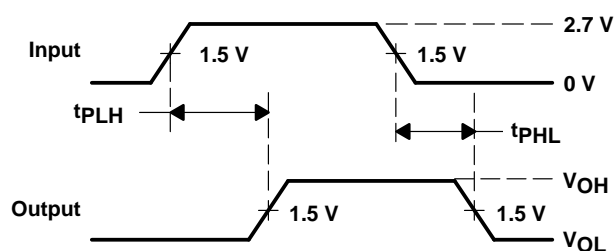


LOAD CIRCUIT

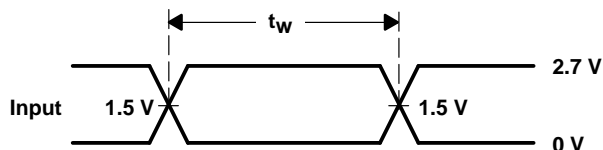
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



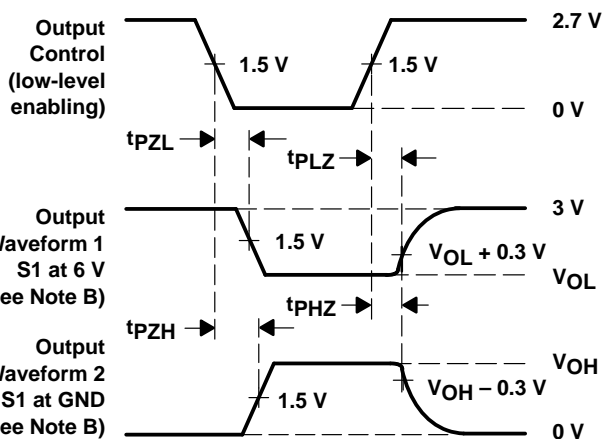
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
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 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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