

# SN74LVC16245A

## 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES062A – DECEMBER 1995 – REVISED JUNE 1996

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8\text{ V}$  at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $> 2\text{ V}$  at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200\text{ pF}$ ,  $R = 0$ )
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

### description

This 16-bit (dual-octal) noninverting bus transceiver is designed for 2.7-V to 3.6-V  $V_{CC}$  operation; it can interface to a 5-V system environment.

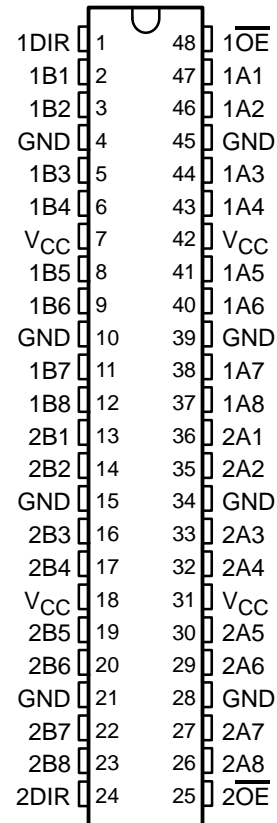
The SN74LVC16245A is designed for asynchronous communication between data buses. The control function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC16245A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

DGG OR DL PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation



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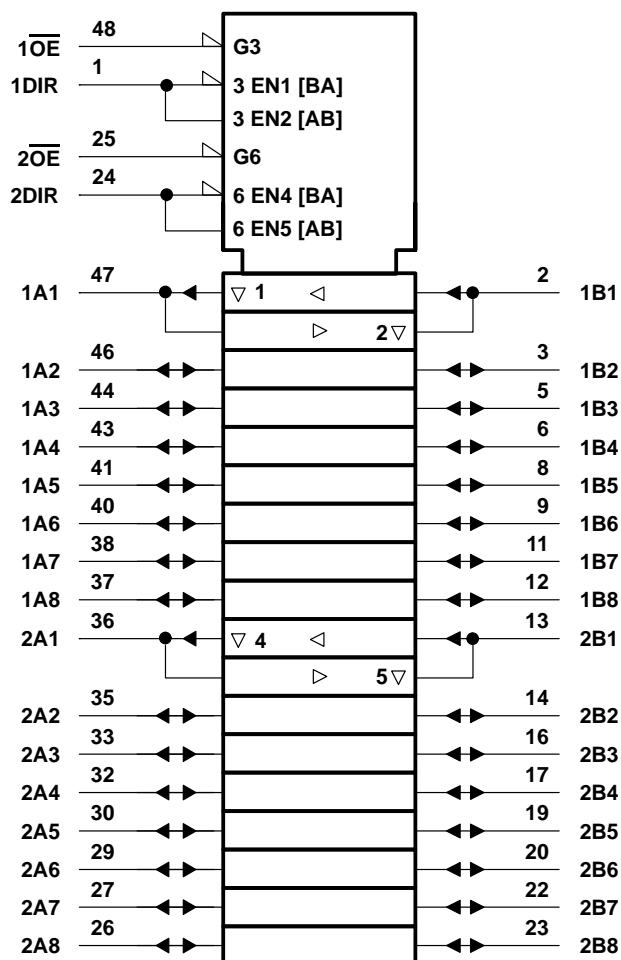


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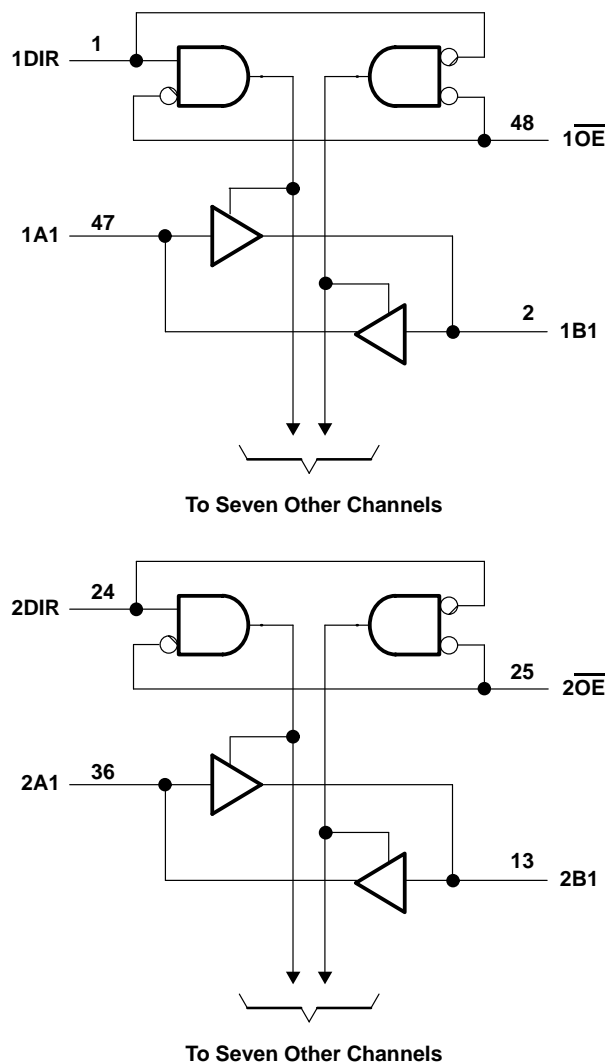
**SN74LVC16245A**  
**16-BIT BUS TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**  
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**logic symbol†**



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**logic diagram (positive logic)**



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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$	–0.5 V to 6.5 V
Input voltage range, $V_I$ : Except I/O ports (see Note 1)	–0.5 V to 6.5 V
I/O ports (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Voltage applied to any output in the high-impedance state or power-off state, $V_O$ (see Note 1)	–0.5 V to 6.5 V
Voltage applied to any output in the high or low state, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through each $V_{CC}$ or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package	0.85 W
DL package	1.2 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. This value is limited to 4.6 V maximum.  
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

**recommended operating conditions (see Note 4)**

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
$V_{IH}$	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V	2		V
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.8	V
$V_I$	Input voltage		0	5.5	V
$V_O$	Output voltage	High or low state	0	$V_{CC}$	V
		3 state	0	5.5	
$I_{OH}$	High-level output current	$V_{CC} = 2.7$ V		–12	mA
		$V_{CC} = 3$ V		–24	
$I_{OL}$	Low-level output current	$V_{CC} = 2.7$ V		12	mA
		$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	5	ns/V
$T_A$	Operating free-air temperature		–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> <sup>†</sup>	MIN	TYP <sup>‡</sup>	MAX	UNIT
V <sub>OH</sub>		I <sub>OH</sub> = −100 μA	MIN to MAX	V <sub>CC</sub> − 0.2		V	
		I <sub>OH</sub> = −12 mA	2.7 V	2			
		I <sub>OH</sub> = −12 mA	3 V	2.2			
		I <sub>OH</sub> = −24 mA	3 V	2			
V <sub>OL</sub>		I <sub>OL</sub> = 100 μA	MIN to MAX	0.2		V	
		I <sub>OL</sub> = 12 mA	2.7 V	0.4			
		I <sub>OL</sub> = 24 mA	3 V	0.55			
I <sub>I</sub>		V <sub>I</sub> = 5.5 V or GND	3.6 V	±5		μA	
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0	50		μA	
I <sub>OZ</sub> <sup>§</sup>		V <sub>O</sub> = 0 or 5.5 V	3.6 V	±20		μA	
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V	20		μA	
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> − 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V	500		μA	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	5.4		pF	
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	9		pF	

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

<sup>‡</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

<sup>§</sup> For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)**

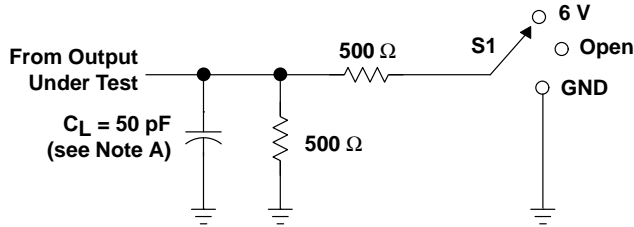
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	B or A	1	5.2	5.8		ns
t <sub>en</sub>	$\overline{\text{OE}}$	A or B	1.5	7.2	8		ns
t <sub>dis</sub>	$\overline{\text{OE}}$	A or B	1.5	7.2	8		ns
t <sub>sk(o)</sub> <sup>¶</sup>			1				ns

<sup>¶</sup> Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

**operating characteristics, V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C**

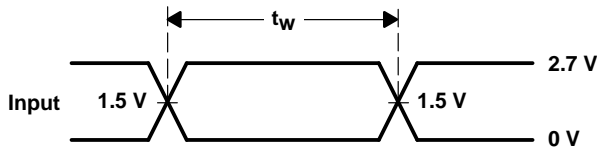
PARAMETER		TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per transceiver	Outputs enabled	24	pF
		Outputs disabled	3.7	

## PARAMETER MEASUREMENT INFORMATION

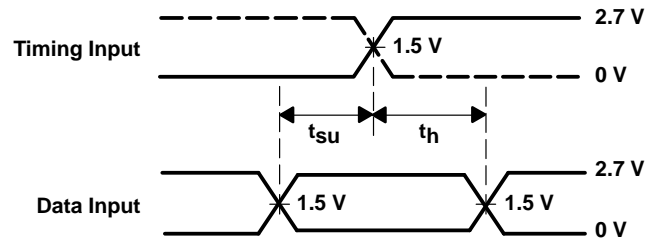


**LOAD CIRCUIT FOR OUTPUTS**

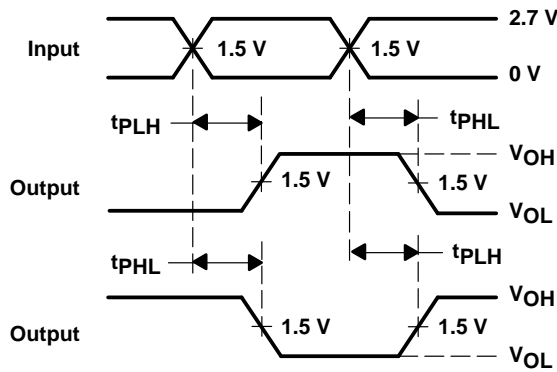
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



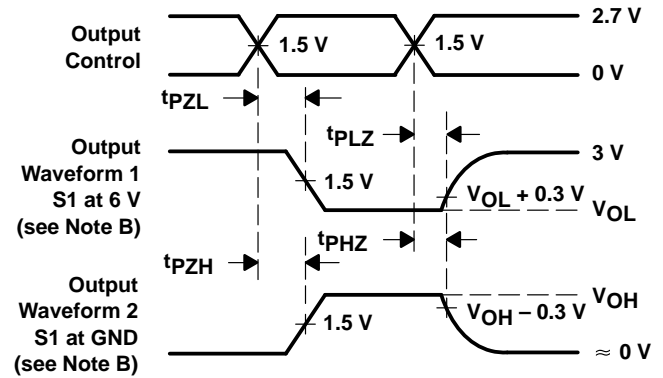
**VOLTAGE WAVEFORMS  
PULSE DURATION**



**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING**

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - F.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

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