

# SN74ALVCH16524

## 18-BIT REGISTERED BUS TRANSCEIVER

### WITH 3-STATE OUTPUTS

SCES080 – JULY 1996

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

#### description

This 18-bit universal bus transceiver is designed for 2.3-V to 3.6-V  $V_{CC}$  operation.

Data flow in each direction is controlled by output-enable ( $\overline{OEAB}$  and  $\overline{OEBA}$ ) and clock enable ( $\overline{CLKENBA}$ ) inputs. For the A-to-B data flow, the data flows through a single register. The B-to-A data can flow through a four-stage pipeline register path, or through a single register path, depending on the state of  $\overline{SEL}$ .

Data is stored in the internal registers on the low-to-high transition of the CLK input, provided that the appropriate  $\overline{CLKENBA}$  input is low. The B-to-A data transfer is synchronized with the CLK input.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16524 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16524 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

DGG OR DL PACKAGE  
(TOP VIEW)

GND	1	56	GND
$\overline{OEAB}$	2	55	$\overline{SEL}$
A1	3	54	B1
GND	4	53	GND
A2	5	52	B2
A3	6	51	B3
$V_{CC}$	7	50	$V_{CC}$
A4	8	49	B4
A5	9	48	B5
A6	10	47	B6
GND	11	46	GND
A7	12	45	B7
A8	13	44	B8
A9	14	43	B9
A10	15	42	B10
A11	16	41	B11
A12	17	40	B12
GND	18	39	GND
A13	19	38	B13
A14	20	37	B14
A15	21	36	B15
$V_{CC}$	22	35	$V_{CC}$
A16	23	34	B16
A17	24	33	B17
GND	25	32	GND
A18	26	31	B18
$\overline{OEBA}$	27	30	CLK
$\overline{CLKENBA}$	28	29	GND



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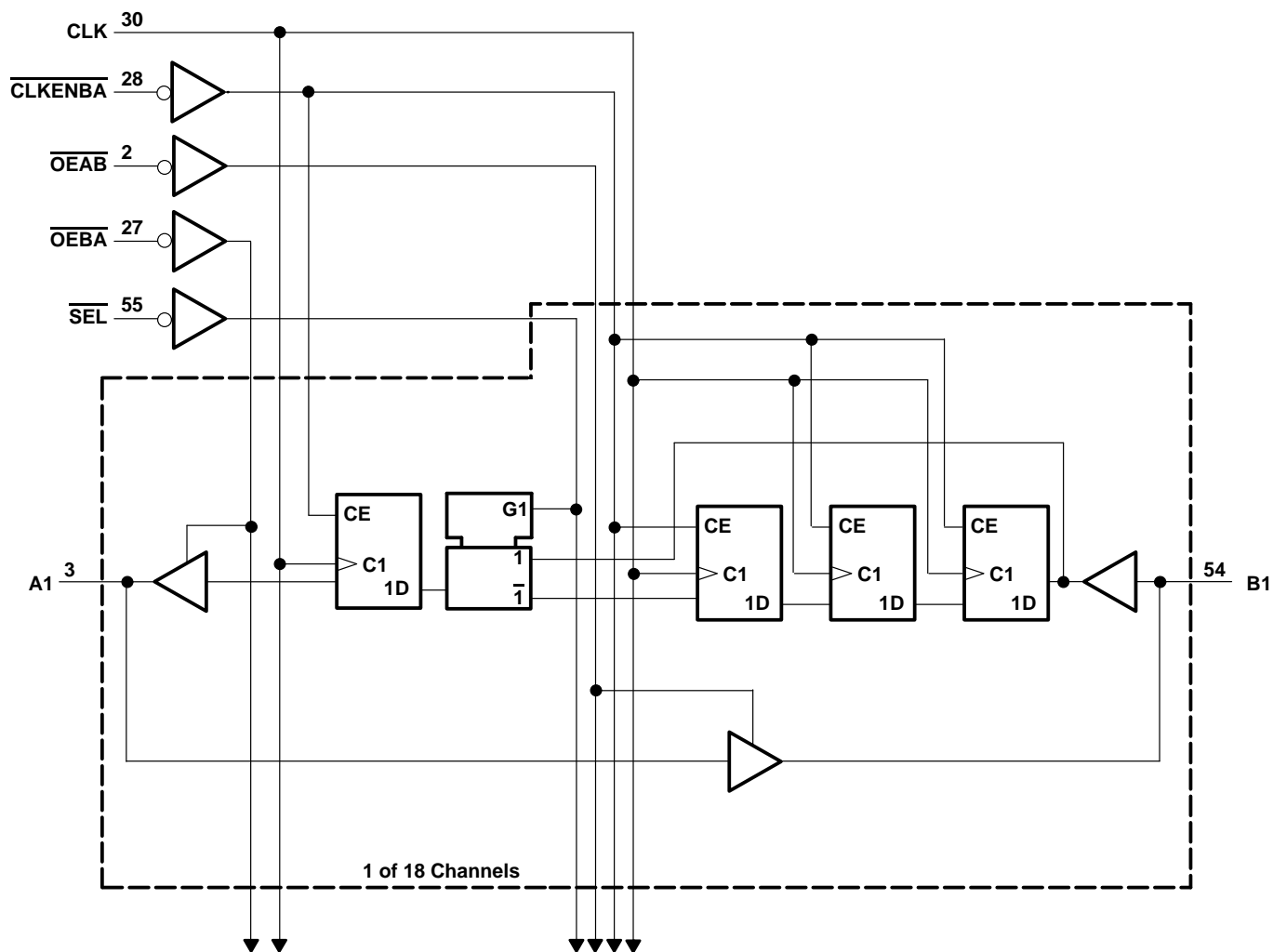
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SCES080 – JULY 1996

#### logic diagram (positive logic)



**FUNCTION TABLE**  
**B-TO-A STORAGE ( $\overline{OEBA} = L$ )**

INPUTS				OUTPUT A
$\overline{CLKENBA}$	CLK	$\overline{SEL}$	B	
H	X	X	X	$A_0^\dagger$
L	$\uparrow$	H	L	L
L	$\uparrow$	H	H	H
L	$\uparrow$	L	L	$L^\ddagger$
L	$\uparrow$	L	H	$H^\ddagger$

$^\dagger$  Output level before the indicated steady-state input conditions were established

$^\ddagger$  Four positive CLK edges are needed to propagate data from B to A when  $\overline{SEL}$  is low.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§**

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 4.6 V
Output voltage range, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 50$ mA
Continuous current through each $V_{CC}$ or GND	$\pm 100$ mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3):	
DGG package	1 W
DL package	1.4 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

§ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
  2. This value is limited to 4.6 V maximum.
  3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

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SCES080 – JULY 1996

#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2.3	3.6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V	2		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V		0.8	V
		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2.3 V		–12	mA
		V <sub>CC</sub> = 2.7 V		–12	
		V <sub>CC</sub> = 3 V		–24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.3 V		12	mA
		V <sub>CC</sub> = 2.7 V		12	
		V <sub>CC</sub> = 3 V		24	
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
T <sub>A</sub>	Operating free-air temperature		–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

**SN74ALVCH16524**  
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SCES080 – JULY 1996

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> <sup>†</sup>	MIN	TYP <sup>‡</sup>	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = −100 μA		MIN to MAX	V <sub>CC</sub> −0.2			V
	I <sub>OH</sub> = −6 mA, V <sub>IH</sub> = 1.7 V		2.3 V	2			
	I <sub>OH</sub> = −12 mA	V <sub>IH</sub> = 1.7 V	2.3 V	1.7			
		V <sub>IH</sub> = 2 V	2.7 V	2.2			
		V <sub>IH</sub> = 2 V	3 V	2.4			
	I <sub>OH</sub> = −24 mA, V <sub>IH</sub> = 2 V		3 V	2			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA		MIN to MAX	0.2			V
	I <sub>OL</sub> = 6 mA, V <sub>IL</sub> = 0.7 V		2.3 V	0.4			
	I <sub>OL</sub> = 12 mA	V <sub>IL</sub> = 0.7 V	2.3 V	0.7			
		V <sub>IL</sub> = 0.8 V	2.7 V	0.4			
	I <sub>OL</sub> = 24 mA, V <sub>IL</sub> = 0.8 V		3 V	0.55			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		3.6 V	±5			μA
I <sub>hold</sub>	V <sub>I</sub> = 0.7 V		2.3 V	45			μA
	V <sub>I</sub> = 1.7 V			−45			
	V <sub>I</sub> = 0.8 V		3 V	75			
	V <sub>I</sub> = 2 V			−75			
	V <sub>I</sub> = 0 to 3.6 V <sup>§</sup>		3.6 V	±500			
I <sub>OZ</sub> <sup>¶</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND		3.6 V	±10			μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0		3.6 V	40			μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> − 0.6 V, Other inputs at V <sub>CC</sub> or GND		3 V to 3.6 V	750			μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	3			pF
C <sub>O</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	7			pF

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

<sup>‡</sup> All typical values are at V<sub>CC</sub> = 3.3, T<sub>A</sub> = 25°C.

<sup>§</sup> This is the bus-hold maximum dynamic current required to switch the input from one state to another.

<sup>¶</sup> For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)**

			VCC = 2.5 V ±0.2 V		VCC = 2.7 V		VCC = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency		0	120	0	125	0	150	MHz
t <sub>w</sub>	Pulse duration, CLK high or low		3.2		3.2		3		ns
t <sub>su</sub>	Setup time	B data before CLK↑	1.5		1.2		1.1		ns
		SEL before CLK↑	2.7		2.4		2.1		
		CLKENBA before CLK↑	2.7		2.6		2		
t <sub>h</sub>	Hold time	B data after CLK↑	1		0.6		1.2		ns
		SEL after CLK↑	0.5		0.2		0.8		
		CLKENBA after CLK↑	0.1		0.1		0.3		



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SCES080 – JULY 1996

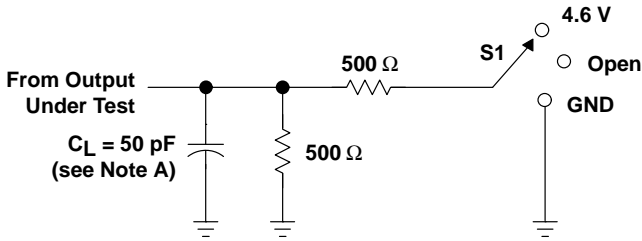
switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			120		125		150		MHz
$t_{pd}$	A	B	1	4.5	3.8		1	3.2	ns
	CLK	A	1	6.7	6.2		1	5.2	
$t_{en}$	$\overline{OEAB}$ or $\overline{OEBA}$	A or B	1	6.6	6.1		1	5.1	ns
$t_{dis}$	$\overline{OEAB}$ or $\overline{OEBA}$	A or B	1	6.5	5.4		1	4.9	ns

operating characteristics,  $T_A = 25^\circ\text{C}$

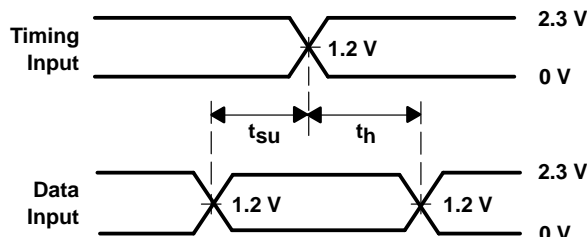
PARAMETER			TEST CONDITIONS	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
				TYP	TYP	
$C_{pd}$	Power dissipation capacitance	Outputs enabled	$C_L = 50$ pF, $f = 10$ MHz	160	160	pF
		Outputs disabled				

**PARAMETER MEASUREMENT INFORMATION**  
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

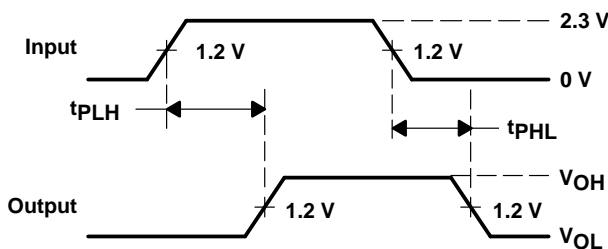


**LOAD CIRCUIT**

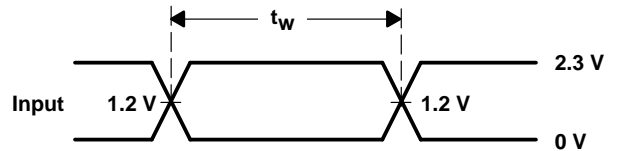
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	4.6 V
$t_{PHZ}/t_{PZH}$	GND



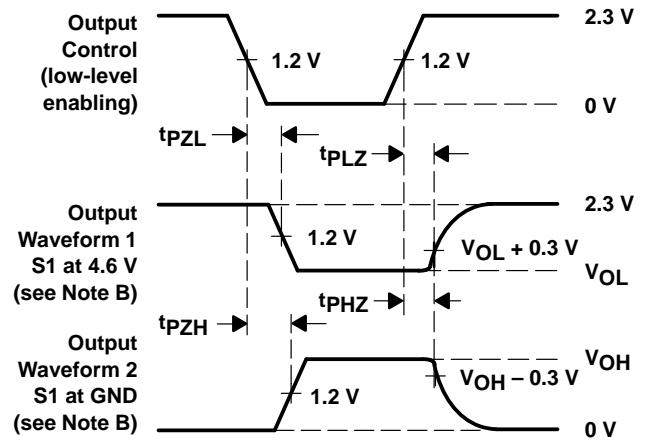
**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS  
PULSE DURATION**



**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES**

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

# SN74ALVCH16524

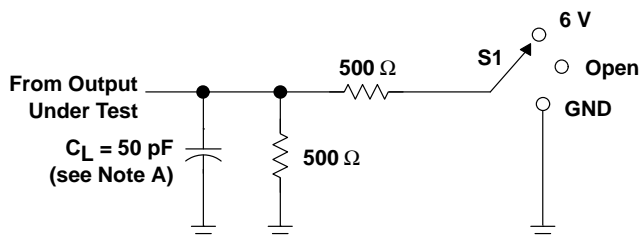
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SCES080 – JULY 1996

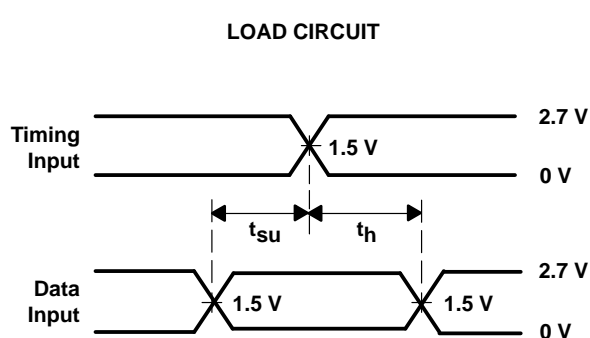
#### PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

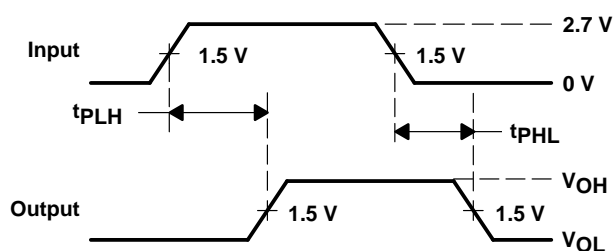


LOAD CIRCUIT

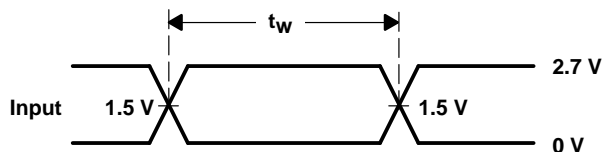
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



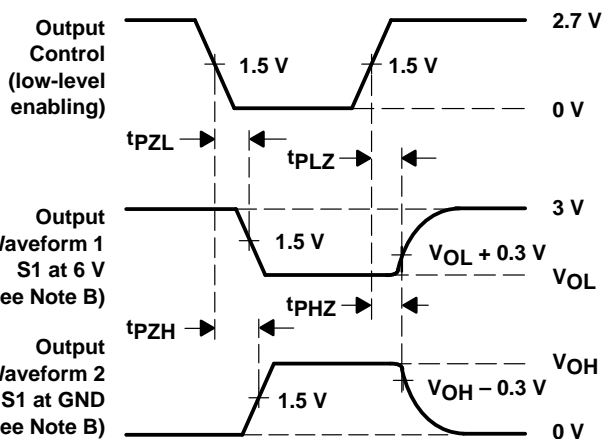
VOLTAGE WAVEFORMS  
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  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Load Circuit and Voltage Waveforms



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