- **Multiplexed I/O Ports Provide Improved Bit Density**
- **Four Modes of Operation: Hold (Store), Shift Right, Shift Left, and Load Data**
- **High Current 3-State Outputs Drive Bus Lines Directly or Up to 15 LSTTL Loads**
- **Can Be Cascaded for N-Bit Word Lengths**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

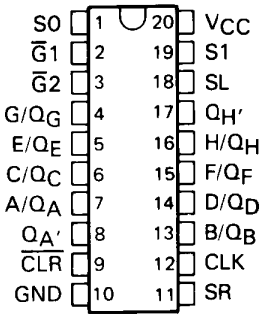
These eight-bit universal registers feature multiplexed I/O ports to achieve full eight-bit handling in a single 20-pin package. 'HC299 applications are as stacked or push-down registers, buffer storage, and accumulator registers.

Two function-select inputs and two output control inputs can be used to choose the modes of operation listed in the function table.

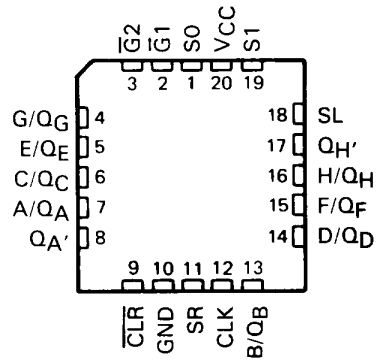
Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the I/O ports to be clocked into the register. Reading out of this register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off. Taking either of the output controls, $\overline{G}1$ or $\overline{G}2$, high disables the outputs but does not affect the shifting or storage of data.

The SN54HC299 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC299 is characterized for operation from −40°C to 85°C.

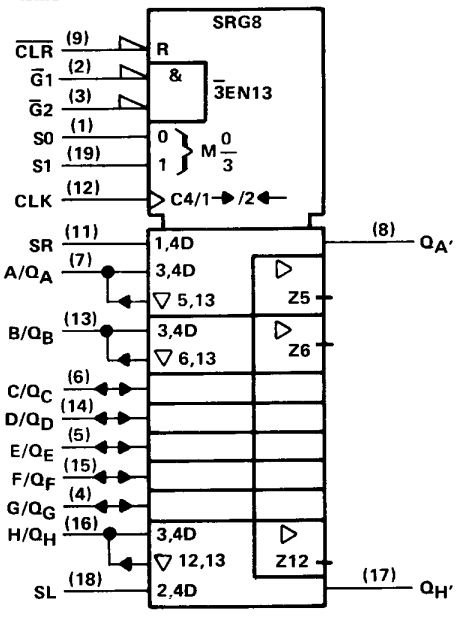
SN54HC299 . . . J PACKAGE
SN74HC299 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC299 . . . FK PACKAGE
(TOP VIEW)

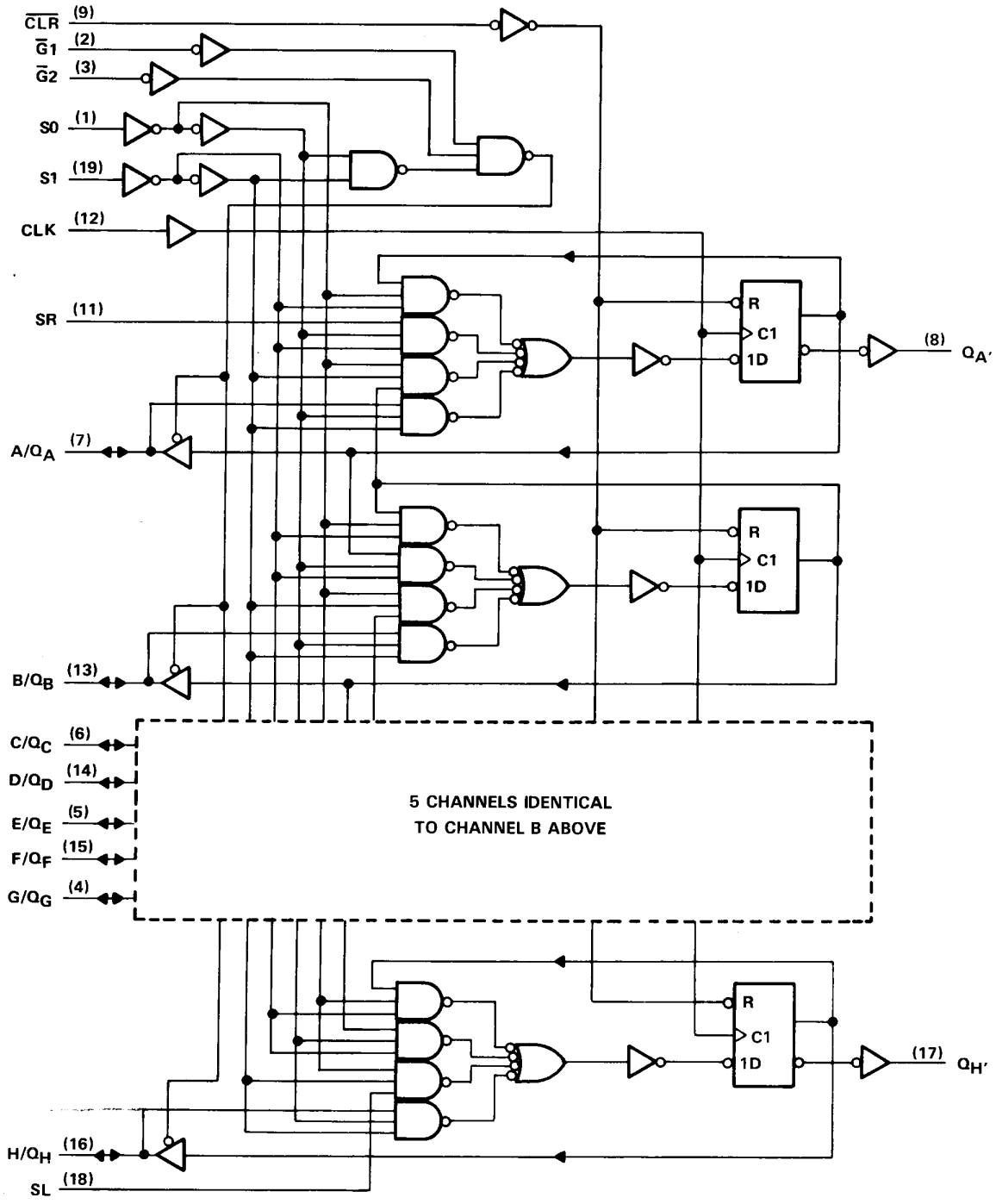


logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



FUNCTION TABLE

MODE	INPUTS								INPUTS/OUTPUTS								OUTPUTS	
	CLEAR	FUNCTION SELECT		OUTPUT CONTROL		CLOCK	SERIAL		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
		S1	S0	$\overline{G1}$†	$\overline{G2}$†		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a . . . h = the level of the steady-state input at inputs through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC299			SN74HC299			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC299		SN74HC299		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA		2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}	$Q_{A'}$ and $Q_{H'}$ I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
		A/Q_n thru H/Q_n I_{OH} = −6 mA									
	V_I = V_{IH} or V_{IL}	$Q_{A'}$ and $Q_{H'}$ I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
		A/Q_n thru H/Q_n I_{OH} = −7.8 mA									
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA		2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}	$Q_{A'}$ and $Q_{H'}$ I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		A/Q_n thru H/Q_n I_{OL} = 6 mA									
	V_I = V_{IH} or V_{IL}	$Q_{A'}$ and Q_H I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
		A/Q_n thru H/Q_H I_{OL} = 7.8 mA									
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}†	V_O = V_{CC} or 0, V_I = V_{IH} or V_{IL}		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0		6 V			8		160		80	μA
C_i‡			2 to 6 V		3	10		10		10	pF

†For I/O ports (Q_A through Q_H), the parameter I_I is included in the off-state output current.
‡This parameter, C_I, does not apply to transceiver I/O ports.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC299		SN74HC299		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	CLK high, CLK low, or $\overline{CLR}$ low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time before CLK↑	S0 or S1	2 V	175		263		219		ns
			4.5 V	35		53		44		
			6 V	30		45		37		
		SL or SR	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		26		21		
		Data or $\overline{CLR}$ inactive	2 V	65		98		81		ns
			4.5 V	13		20		16		
			6 V	11		17		14		
t_h	Hold time after CLK↑	Select or data	2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC299		SN74HC299		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6			4.2		5		MHz
			4.5 V	31			21		25		
			6 V	36			25		29		
t_{pd}	CLK	$Q_{A'}$ or $Q_{H'}$	2 V		45	170		285		210	ns
			4.5 V		16	38		57		48	
			6 V		13	32		48		40	
		Q_A thru Q_H	2 V		42	170		285		210	ns
			4.5 V		16	38		57		48	
			6 V		12	32		48		40	
t_{en}	$\overline{G}1$ or $\overline{G}2$	Q_A thru Q_H	2 V		60	160		240		200	ns
			4.5 V		24	32		48		40	
			6 V		23	27		41		34	
	S0 or S1		2 V		115	300		450		375	ns
			4.5 V		44	60		90		75	
			6 V		39	51		77		64	
t_{dis}	$\overline{G}1$, or $\overline{G}2$	Q_A thru Q_H	2 V		60	160		240		200	ns
			4.5 V		24	32		48		40	
			6 V		23	27		41		34	
	S0 or S1		2 V		115	300		450		375	ns
			4.5 V		44	60		90		75	
			6 V		39	51		77		64	
t_{PHL}	$\overline{CLR}$	$Q_{A'}$ or $Q_{H'}$	2 V		41	210		315		250	ns
			4.5 V		17	42		63		53	
			6 V		13	36		54		45	
		Q_A thru Q_H	2 V		50	200		315		250	ns
			4.5 V		17	42		63		53	
			6 V		13	36		54		45	
t_t		$Q_{A'}$ or $Q_{H'}$	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	
		Q_A thru Q_H	2 V		38	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	100 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC299		SN74HC299		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	CLK	Q_A thru Q_H	2 V		56	230		345		288	ns
			4.5 V		21	46		69		58	
			6 V		16	39		59		49	
t_{en}	$\overline{G}1$ or $\overline{G}2$	Q_A thru Q_H	2 V		94	220		330		275	ns
			4.5 V		38	44		66		55	
			6 V		33	37		56		47	
	S0 or S1		2 V		130	450		675		563	ns
			4.5 V		59	90		135		113	
			6 V		49	77		115		96	
t_{PHL}	$\overline{CLR}$	Q_A thru Q_H	2 V		63	260		390		325	ns
			4.5 V		21	52		78		65	
			6 V		17	44		66		55	
t_t		Q_A thru Q_H	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.