

SN54LV164, SN74LV164 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

SCLS191B – FEBRUARY 1993 – REVISED APRIL 1996

- **EPIC™ (Enhanced-Performance Implanted CMOS) 2-μ Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} , $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Chip Carriers (FK), and (J) 300-mil DIPs**

description

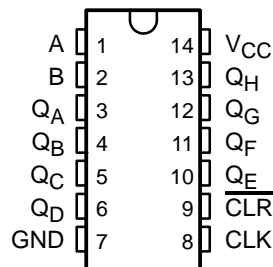
These 8-bit parallel-out serial shift registers are designed for 2.7-V to 5.5-V V_{CC} operation.

The 'LV164 feature AND-gated serial (A and B) inputs and an asynchronous clear ($\overline{\text{CLR}}$) input. The gated serial inputs permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs can be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock (CLK) input.

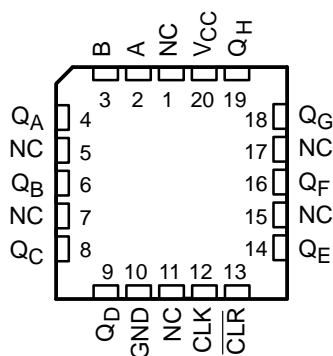
The SN74LV164 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LV164 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV164 is characterized for operation from -40°C to 85°C .

SN54LV164 . . . J OR W PACKAGE
SN74LV164 . . . D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LV164 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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**TEXAS
INSTRUMENTS**

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SN54LV164, SN74LV164 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

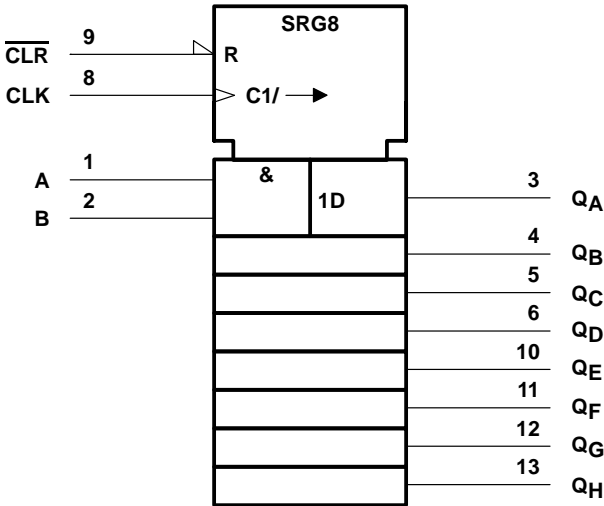
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| FUNCTION TABLE | | | | |
|----------------|-----|---|---|--|
| INPUTS | | | | OUTPUTS |
| CLR | CLK | A | B | Q _A Q _B . . . Q _H |
| L | X | X | X | L L L |
| H | L | X | X | Q _{A0} Q _{B0} Q _{H0} |
| H | ↑ | H | H | H Q _{An} Q _{Gn} |
| H | ↑ | L | X | L Q _{An} Q _{Gn} |
| H | ↑ | X | L | L Q _{An} Q _{Gn} |

Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state inputs conditions were established

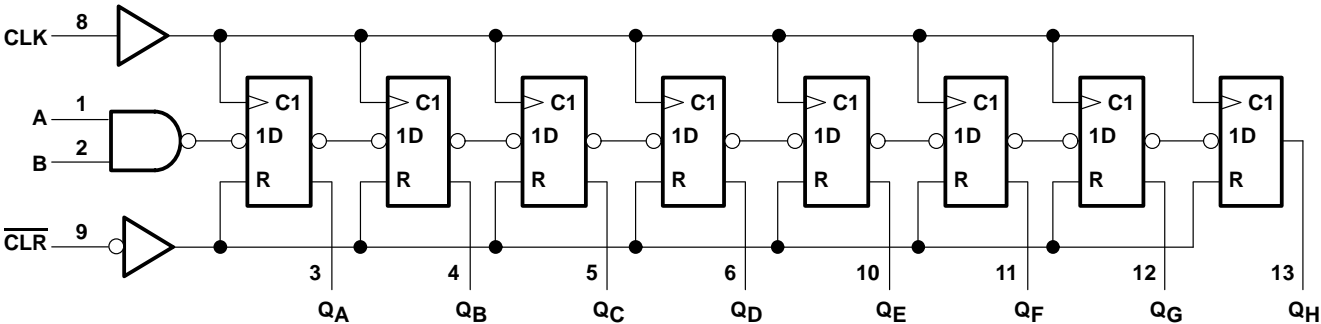
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of the clock: indicates a 1-bit shift

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, DB, J, PW, and W packages.

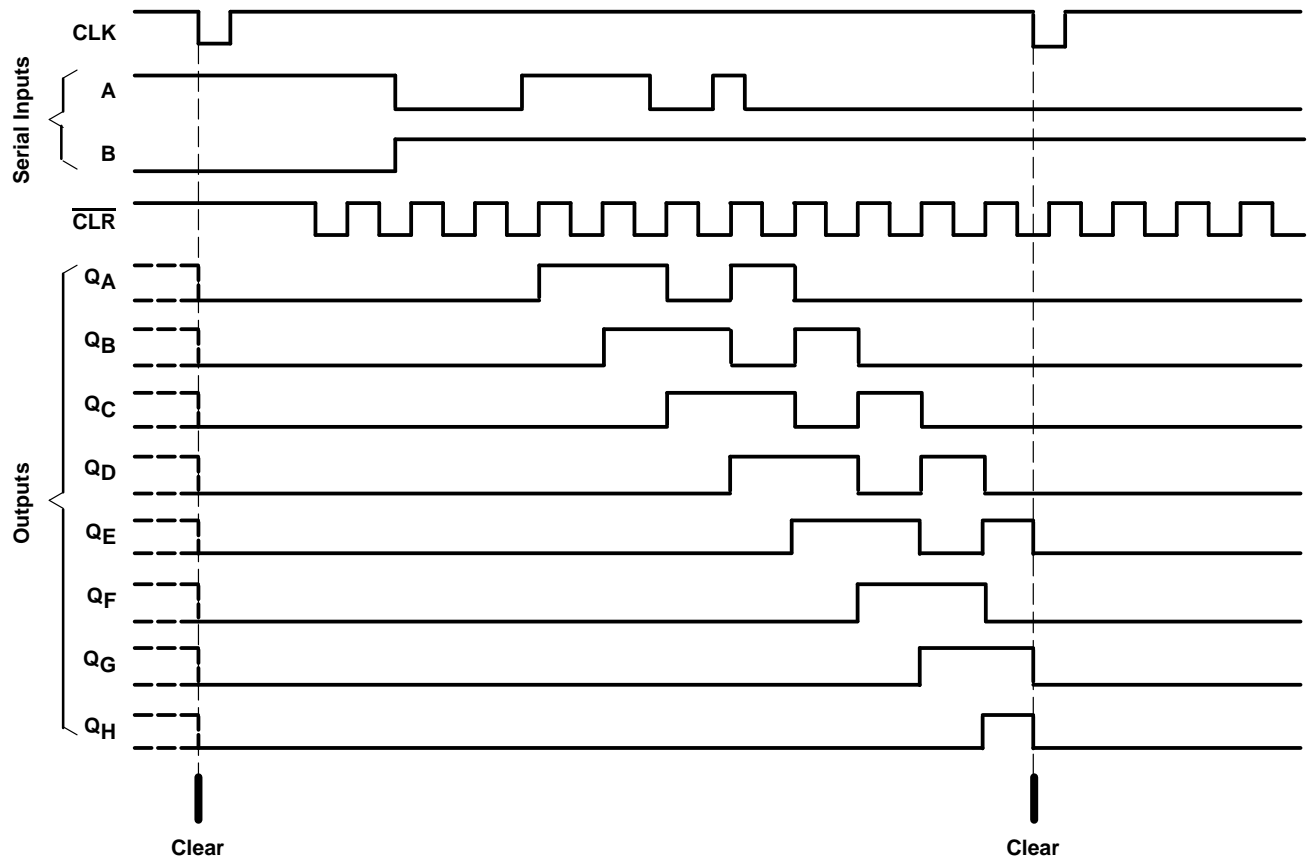
logic diagram (positive logic)



SN54LV164, SN74LV164 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

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typical clear, shift, and clear sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|--|--|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Output voltage range, V_O (see Notes 1 and 2) | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) | ± 20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | ± 50 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ± 25 mA |
| Continuous current through V_{CC} or GND | ± 50 mA |
| Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): D package | 1.25 W |
| DB or PW package | 0.5 W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

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recommended operating conditions (see Note 4)

| | | | SN54LV164 | | SN74LV164 | | UNIT |
|-----------------|------------------------------------|----------------------------------|-----------|-----------------|-----------|-----------------|------|
| | | | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | | 2.7 | 5.5 | 2.7 | 5.5 | V |
| V _{IH} | High-level input voltage | V _{CC} = 2.7 V to 3.6 V | 2 | | 2 | | V |
| | | V _{CC} = 4.5 V to 5.5 V | 3.15 | | 3.15 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 2.7 V to 3.6 V | 0.8 | | 0.8 | | V |
| | | V _{CC} = 4.5 V to 5.5 V | 1.65 | | 1.65 | | |
| V _I | Input voltage | | 0 | V _{CC} | 0 | V _{CC} | V |
| V _O | Output voltage | | 0 | V _{CC} | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 2.7 V to 3.6 V | −6 | | −6 | | mA |
| | | V _{CC} = 4.5 V to 5.5 V | −12 | | −12 | | |
| I _{OL} | Low-level output current | V _{CC} = 2.7 V to 3.6 V | 6 | | 6 | | mA |
| | | V _{CC} = 4.5 V to 5.5 V | 12 | | 12 | | |
| Δt/Δv | Input transition rise or fall rate | | 0 | 100 | 0 | 100 | ns/V |
| T _A | Operating free-air temperature | | −55 | 125 | −40 | 85 | °C |

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} [†] | SN54LV164 | | | SN74LV164 | | | UNIT |
|------------------|---|------------------------------|-----------------------|-----|-----|-----------------------|-----|-----|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V _{OH} | I _{OH} = –100 μA | MIN to MAX | V _{CC} – 0.2 | | | V _{CC} – 0.2 | | | V |
| | I _{OH} = –6 mA | 3 V | 2.4 | | | 2.4 | | | |
| | I _{OH} = –12 mA | 4.5 V | 3.6 | | | 3.6 | | | |
| V _{OL} | I _{OL} = 100 μA | MIN to MAX | 0.2 | | | 0.2 | | | V |
| | I _{OL} = 6 mA | 3 V | 0.4 | | | 0.4 | | | |
| | I _{OL} = 12 mA | 4.5 V | 0.55 | | | 0.55 | | | |
| I _I | V _I = V _{CC} or GND | 3.6 V | ±1 | | | ±1 | | | μA |
| | | 5.5 V | ±1 | | | ±1 | | | |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 3.6 V | 20 | | | 20 | | | μA |
| | | 5.5 V | 20 | | | 20 | | | |
| ΔI _{CC} | One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND | 3 V to 3.6 V | 500 | | | 500 | | | μA |
| C _i | V _I = V _{CC} or GND | 3.3 V | 2.5 | | | 2.5 | | | pF |
| | | 5 V | 3 | | | 3 | | | |

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | | SN54LV164 | | | | | | UNIT |
|--------------------|------------------------------|-----------------|---|-----|---|-----|-------------------------|-----|------|
| | | | $V_{CC} = 5.5\text{ V}$ $\pm 0.5\text{ V}$ | | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | | 0 | 40 | 0 | 35 | 0 | 30 | MHz |
| t _w | Pulse duration | CLR low | 14 | | 16 | | 18 | | ns |
| | | CLK high or low | 14 | | 16 | | 18 | | |
| t _{su} | Setup time, data before CLK↑ | Data | 8 | | 10 | | 12 | | ns |
| | | CLR inactive | 5 | | 6 | | 7 | | |
| t _h | Hold time, data after CLK↑ | | 3 | | 3 | | 3 | | ns |

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | | SN74LV164 | | | | | | UNIT | |
|--------------------|------------------------------|--|------------------------------------|-----|------------------------------------|-----|-------------------------|-----|------|----|
| | | | V _{CC} = 5.5 V ± 0.5 V | | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 2.7 V | | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| f _{clock} | Clock frequency | | 0 | 40 | 0 | 35 | 0 | 30 | MHz | |
| t _w | Pulse duration | | CLR low | | 14 | | 16 | | 18 | ns |
| | | | CLK high or low | | 14 | | 16 | | 18 | |
| t _{su} | Setup time, data before CLK↑ | | Data | | 8 | | 10 | | 12 | ns |
| | | | CLR inactive | | 5 | | 6 | | 7 | |
| t _h | Hold time, data after CLK↑ | | 3 | | 3 | | 3 | | ns | |

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LV164 | | | | | | | | UNIT |
|------------------|-----------------|----------------|---------------------------------|-----|-----|---------------------------------|-----|-----|-------------------------|-----|------|
| | | | V _{CC} = 5.5 V ± 0.5 V | | | V _{CC} = 3.3 V ± 0.3 V | | | V _{CC} = 2.7 V | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | MAX | |
| f _{max} | | | 40 | 90 | | 35 | 75 | | 30 | | MHz |
| t _{pd} | CLK | Q | | 10 | 20 | | 14 | 26 | | 32 | ns |
| t _{PHL} | CLR | Q | | 12 | 20 | | 16 | 26 | | 32 | ns |

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74LV164 | | | | | | | | UNIT |
|------------------|-----------------|----------------|---------------------------------|-----|-----|---------------------------------|-----|-----|-------------------------|-----|------|
| | | | V _{CC} = 5.5 V ± 0.5 V | | | V _{CC} = 3.3 V ± 0.3 V | | | V _{CC} = 2.7 V | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | MAX | |
| f _{max} | | | 40 | 90 | | 35 | 75 | | 30 | | MHz |
| t _{pd} | CLK | Q | | 10 | 20 | | 14 | 26 | | 32 | ns |
| t _{PHL} | <u>CLR</u> | Q | | 12 | 20 | | 16 | 26 | | 32 | ns |

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SN54LV164, SN74LV164

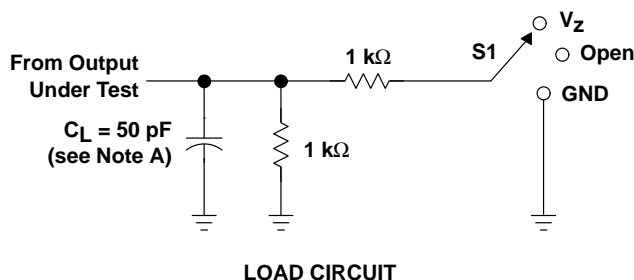
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operating characteristics, $T_A = 25^\circ\text{C}$

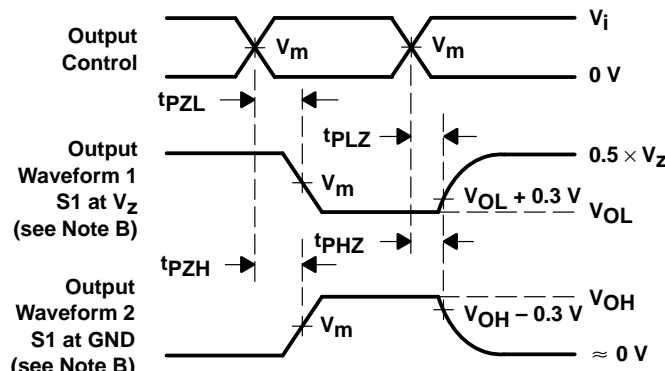
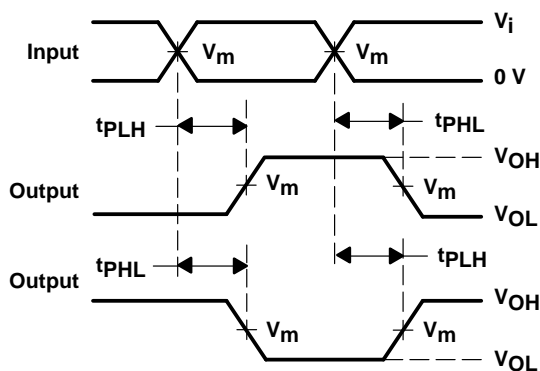
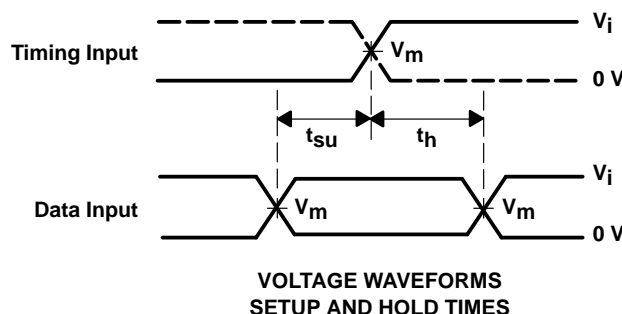
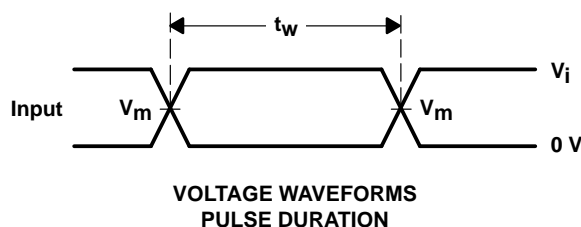
| PARAMETER | TEST CONDITIONS | TYP | TYP | UNIT |
|--|--|-------|-----|------|
| C_{pd} Power dissipation capacitance | $C_L = 50\text{ pF}$, $f = 10\text{ MHz}$ | 3.3 V | 74 | pF |
| | | 5 V | 75 | |

PARAMETER MEASUREMENT INFORMATION



| TEST | S1 |
|------------------------------------|----------------|
| t _{PLH} /t _{PHL} | Open |
| t _{PLZ} /t _{PZL} | V _Z |
| t _{PHZ} /t _{PZH} | GND |

| WAVEFORM CONDITION | V _{CC} = 4.5 V to 5.5 V | V _{CC} = 2.7 V to 3.6 V |
|--------------------|----------------------------------|----------------------------------|
| V _m | 0.5 × V _{CC} | 1.5 V |
| V _i | V _{CC} | 2.7 V |
| V _Z | 2 × V _{CC} | 6 V |



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $\text{PRR} \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - t_{PZL} and t_{PZH} are the same as t_{en}.
 - t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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