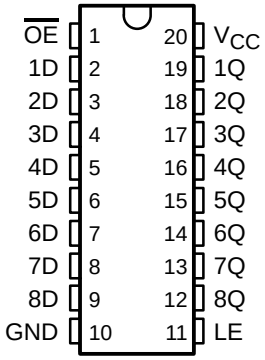
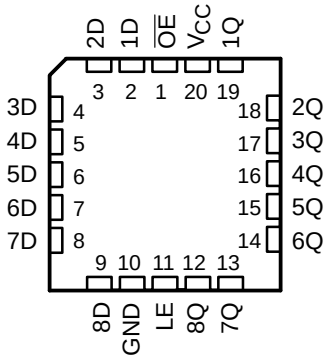
- **Inputs Are TTL-Voltage Compatible**
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54AHCT573 . . . J OR W PACKAGE**
**SN74AHCT573 . . . DB, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHCT573 . . . FK PACKAGE**
**(TOP VIEW)**




## description

The ’AHCT573 are octal-transparent D-type latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AHCT573 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT573 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each latch)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

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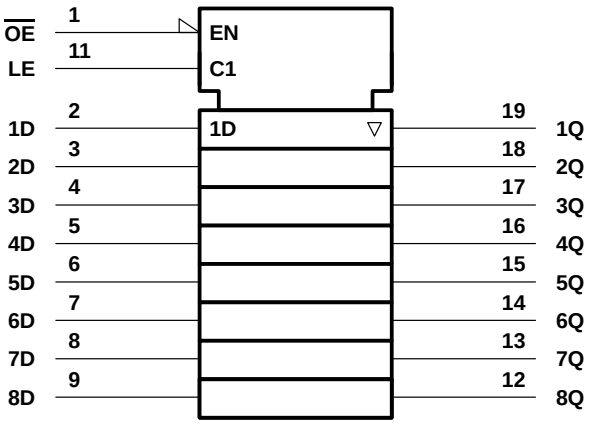
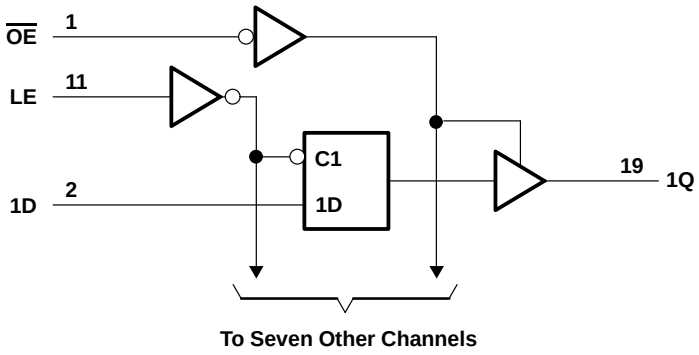
### logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)




### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{CC}$) . . . . . –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . –20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through $V_{CC}$ or GND . . . . . ±75 mA
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 2): DB package . . . . . 0.6 W
DW package . . . . . 1.6 W
N package . . . . . 1.3 W
PW package . . . . . 0.7 W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

## recommended operating conditions (see Note 3)

| | | SN54AHCT573 | | SN74AHCT573 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –8 | | –8 | mA |
| $I_{OL}$ | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHCT573 | | SN74AHCT573 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | $I_{OH}$ = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | $I_{OL}$ = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | |
| $I_{OZ}$ | $V_O = V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $\Delta I_{CC}$† | One input at 3.4 V, Other inputs at GND or $V_{CC}$ | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 2.5 | 10 | | | | 10 | pF |
| $C_o$ | $V_O = V_{CC}$ or GND | 5 V | | 3 | | | | | | pF |

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| | | $T_A$ = 25°C | | SN54AHCT573 | | SN74AHCT573 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high | 5 | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time, data before LE↓ | 3.5 | | 3.5 | | 3.5 | | ns |
| $t_h$ | Hold time, data after LE↓ | 1.5 | | 1.5 | | 1.5 | | ns |

ADVANCE INFORMATION

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN54AHCT573 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$* | D | Q | $C_L$ = 15 pF | | 4.2 | 6 | 1 | 6.5 | ns |
| $t_{PHL}$* | | | | | 5.1 | 7 | 1 | 9 | |
| $t_{PLH}$* | LE | Q | $C_L$ = 15 pF | | 4.7 | 6.5 | 1 | 7.5 | ns |
| $t_{PHL}$* | | | | | 5.6 | 7.5 | 1 | 9 | |
| $t_{PZH}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 4.1 | 6.5 | 1 | 7 | ns |
| $t_{PZL}$* | | | | | 5.5 | 7.5 | 1 | 10 | |
| $t_{PHZ}$* | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 5.5 | 8 | 1 | 11 | ns |
| $t_{PLZ}$* | | | | | 5.4 | 8 | 1 | 9.5 | |
| $t_{PLH}$ | D | Q | $C_L$ = 50 pF | | 5.2 | 7 | 1 | 7.5 | ns |
| $t_{PHL}$ | | | | | 6.1 | 8 | 1 | 10 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 50 pF | | 5.7 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 6.6 | 8.5 | 1 | 10 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 5.1 | 7.5 | 1 | 8 | ns |
| $t_{PZL}$ | | | | | 6.5 | 8.5 | 1 | 11 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 6.7 | 9 | 1 | 12 | ns |
| $t_{PLZ}$ | | | | | 6.4 | 9 | 1 | 10.5 | |

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | SN74AHCT573 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | MIN | MAX | |
| | | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | D | Q | $C_L$ = 15 pF | | 4.2 | 6 | 1 | 6.5 | ns |
| $t_{PHL}$ | | | | | 5.1 | 7 | 1 | 9 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 15 pF | | 4.7 | 6.5 | 1 | 7.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 7.5 | 1 | 9 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 4.1 | 6.5 | 1 | 7 | ns |
| $t_{PZL}$ | | | | | 5.5 | 7.5 | 1 | 10 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 5.5 | 8 | 1 | 11 | ns |
| $t_{PLZ}$ | | | | | 5.4 | 8 | 1 | 9.5 | |
| $t_{PLH}$ | D | Q | $C_L$ = 50 pF | | 5.2 | 7 | 1 | 7.5 | ns |
| $t_{PHL}$ | | | | | 6.1 | 8 | 1 | 10 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 50 pF | | 5.7 | 7.5 | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 6.6 | 8.5 | 1 | 10 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 5.1 | 7.5 | 1 | 8 | ns |
| $t_{PZL}$ | | | | | 6.5 | 8.5 | 1 | 11 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 6.7 | 9 | 1 | 12 | ns |
| $t_{PLZ}$ | | | | | 6.4 | 9 | 1 | 10.5 | |

### output-skew characteristics, $C_L$ = 50 pF (see Note 4)

| PARAMETER | | $V_{CC}$ | SN74AHCT573 | | UNIT |
|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | MIN MAX | |
| | | | MIN MAX | | |
| $t_{sk(o)}$ | Output skew | 5 V ± 0.5 V | 1 | 1 | ns |

NOTE 4: Characteristics are determined during product characterization and ensured by design.

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

| PARAMETER | | SN74AHCT573 | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 1.1 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.7 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 3.7 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 0.8 | V |

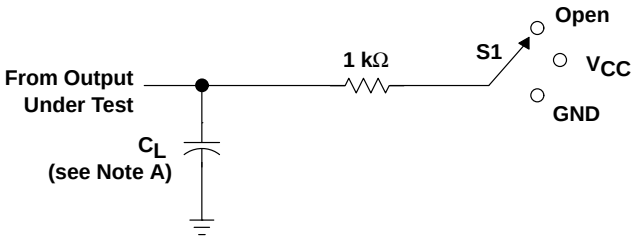
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 16 | pF |

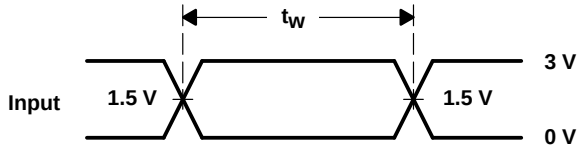
ADVANCE INFORMATION

## PARAMETER MEASUREMENT INFORMATION

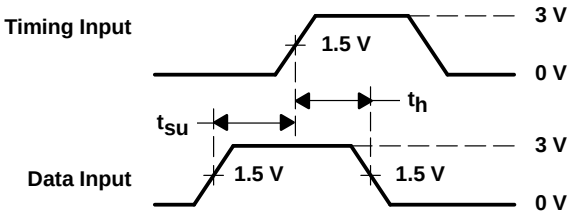



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

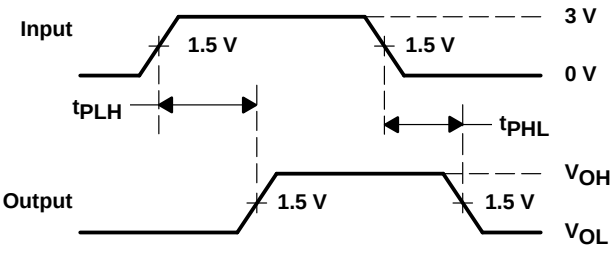
LOAD CIRCUIT



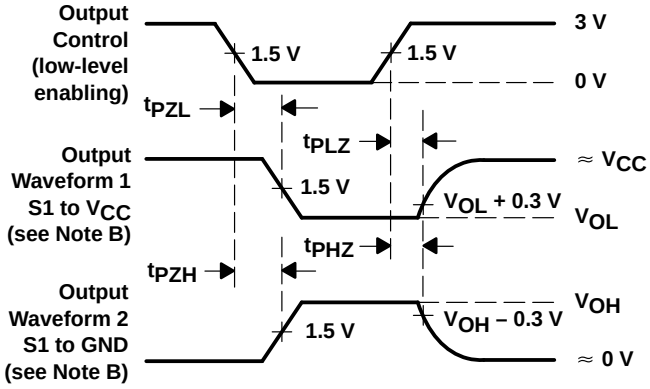

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

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