

SN54AHCT574, SN74AHCT574 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS245C – OCTOBER 1995 – REVISED NOVEMBER 1996

- Inputs Are TTL-Voltage Compatible
- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

The 'AHCT574 are octal edge-triggered D-type flip-flops that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

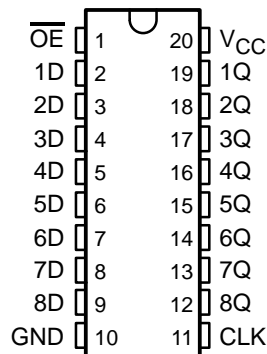
On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

A buffered output-enable (\overline{OE}) input places the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

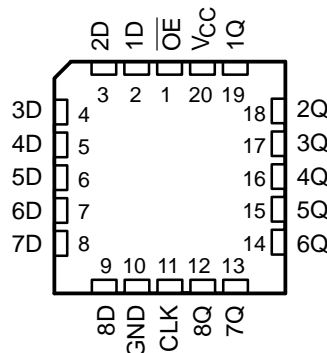
\overline{OE} does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AHCT574 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AHCT574 is characterized for operation from -40°C to 85°C .

SN54AHCT574 . . . J OR W PACKAGE
SN74AHCT574 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT574 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT Q
\overline{OE}	CLK	D	
L	\uparrow	H	H
L	\uparrow	L	L
L	L or H	X	Q_0
H	X	X	Z



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**TEXAS
INSTRUMENTS**

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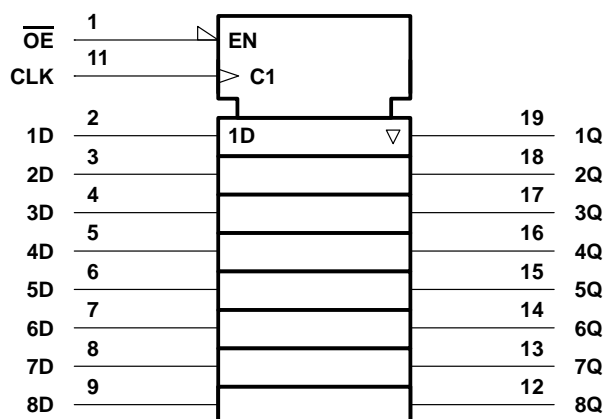
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OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

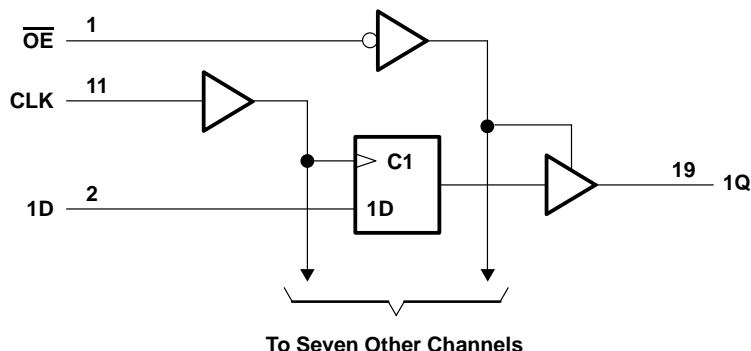
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	–20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±75 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package	0.6 W
DW package	1.6 W
N package	1.3 W
PW package	0.7 W

Storage temperature range, T_{stg} –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.



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recommended operating conditions (see Note 3)

		SN54AHCT574		SN74AHCT574		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		–8		–8	mA
I _{OL}	Low-level output current		8		8	mA
Δt/Δv	Input transition rise or fall rate		20		20	ns/V
T _A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHCT574		SN74AHCT574		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = –50 μA	4.5 V	4.4	4.5		4.4		4.4		V
	I _{OH} = –8 mA		3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I _{OL} = 8 mA				0.36		0.44		0.44	
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.25		±2.5		±2.5	μA
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40		40	μA
ΔI _{CC} [†]	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			1.35		1.5		1.5	mA
C _i	V _I = V _{CC} or GND	5 V		3	10				10	pF
C _o	V _O = V _{CC} or GND	5 V		3						pF

[†] This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54AHCT574		SN74AHCT574		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, CLK high or low	5		5.5		5.5		ns
t _{su}	Setup time, data before CLK↑	3		3.5		3.5		ns
t _h	Hold time, data after CLK↑	1.5		1.5		1.5		ns

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SN54AHCT574, SN74AHCT574

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WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT574					UNIT
				T _A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f _{max}			C _L = 15 pF	130	180	110		MHz	
			C _L = 50 pF	85	115	75			
t _{PLH} *	CLK	Q	C _L = 15 pF	5.5 8.6		1	10	ns	
t _{PHL} *				5.5 8.6		1	10		
t _{PZH} *	$\overline{\text{OE}}$	Q	C _L = 15 pF	5 9		1	10.5	ns	
t _{PZL} *				5 9		1	10.5		
t _{PHZ} *	$\overline{\text{OE}}$	Q	C _L = 15 pF	5.5 9		1	10.5	ns	
t _{PLZ} *				5.5 9		1	10.5		
t _{PLH}	CLK	Q	C _L = 50 pF	7	10.6	1	12	ns	
t _{PHL}				7	10.6	1	12		
t _{PZH}	$\overline{\text{OE}}$	Q	C _L = 50 pF	6	11	1	12.5	ns	
t _{PZL}				6	11	1	12.5		
t _{PHZ}	$\overline{\text{OE}}$	Q	C _L = 50 pF	7	10.1	1	11.5	ns	
t _{PLZ}				7	10.1	1	11.5		

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT574					UNIT
				T _A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f _{max}			C _L = 15 pF	130	180		110	MHz	
			C _L = 50 pF	85	115		75		
t _{PLH}	CLK	Q	C _L = 15 pF		5.5	8.6	1	10	ns
t _{PHL}					5.5	8.6	1	10	
t _{PZH}	$\overline{\text{OE}}$	Q	C _L = 15 pF		5	9	1	10.5	ns
t _{PZL}					5	9	1	10.5	
t _{PHZ}	$\overline{\text{OE}}$	Q	C _L = 15 pF		5.5	9	1	10.5	ns
t _{PLZ}					5.5	9	1	10.5	
t _{PLH}	CLK	Q	C _L = 50 pF		7	10.6	1	12	ns
t _{PHL}					7	10.6	1	12	
t _{PZH}	$\overline{\text{OE}}$	Q	C _L = 50 pF		6	11	1	12.5	ns
t _{PZL}					6	11	1	12.5	
t _{PHZ}	$\overline{\text{OE}}$	Q	C _L = 50 pF		7	10.1	1	11.5	ns
t _{PLZ}					7	10.1	1	11.5	

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output-skew characteristics, $C_L = 50 \text{ pF}$ (see Note 4)

PARAMETER		V _{CC}	SN74AHCT574				UNIT
			T _A = 25°C		MIN	MAX	
			MIN	MAX			
t _{sk(o)}	Output skew	5 V ± 0.5 V	1		1	ns	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, $V_{CC} = 5 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER	SN74AHCT574		UNIT
	MIN	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}		-0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}	3.9		V
$V_{IH(D)}$ High-level dynamic input voltage	2		V
$V_{IL(D)}$ Low-level dynamic input voltage		0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1 \text{ MHz}$	28	pF

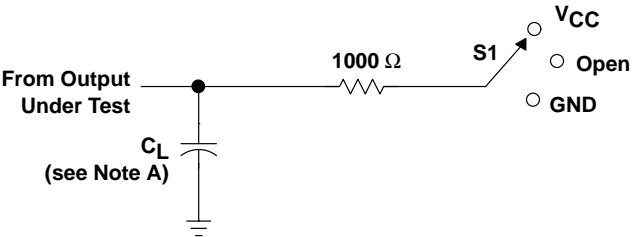
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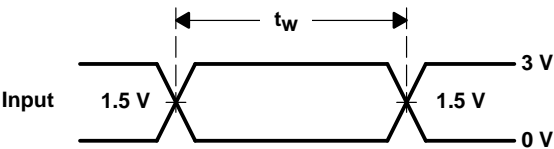
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PARAMETER MEASUREMENT INFORMATION

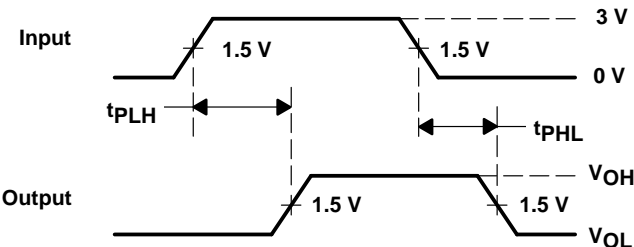


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

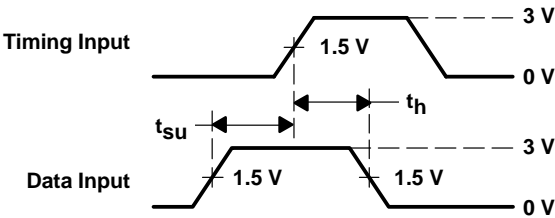
LOAD CIRCUIT



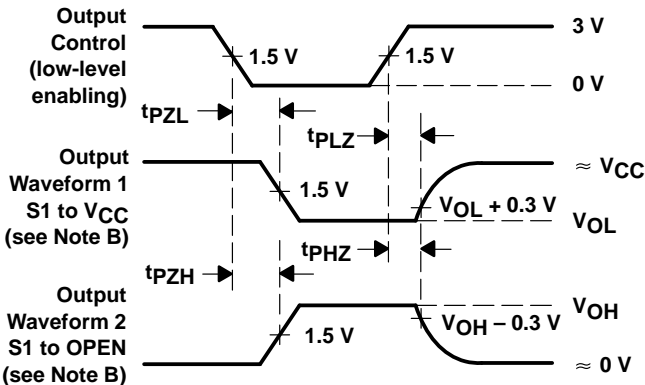
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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