

# SN54AHCT240, SN74AHCT240 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS252B – OCTOBER 1995 – NOVEMBER 1996

- Inputs Are TTL-Voltage Compatible
- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

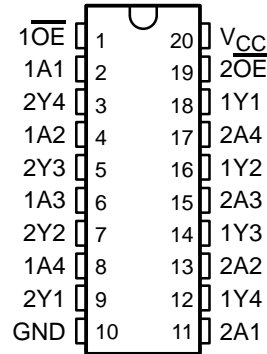
## description

These octal buffers/drivers are designed specifically to improve the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

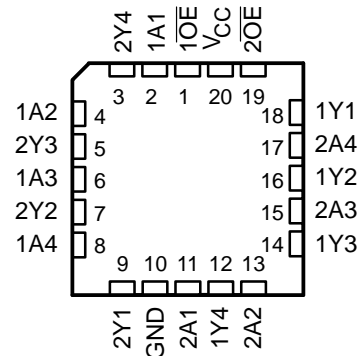
The 'AHCT240 are organized as two 4-bit buffers/line drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

The SN54AHCT240 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74AHCT240 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

SN54AHCT240 . . . J OR W PACKAGE  
SN74AHCT240 . . . DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



SN54AHCT240 . . . FK PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each buffer/driver)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z



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**TEXAS  
INSTRUMENTS**

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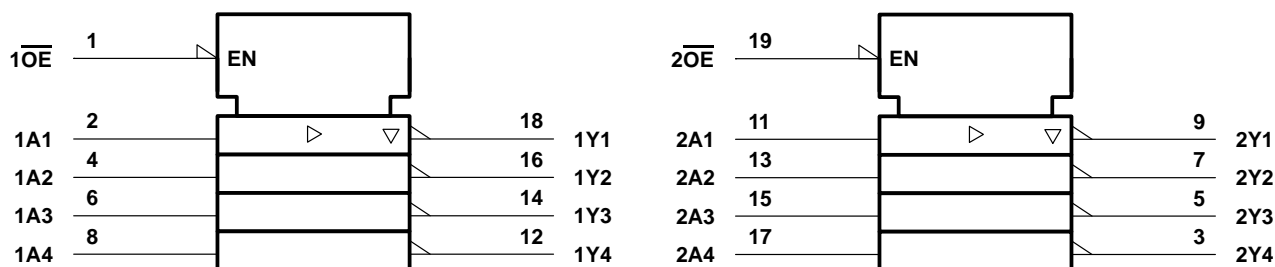
# SN54AHCT240, SN74AHCT240

## OCTAL BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

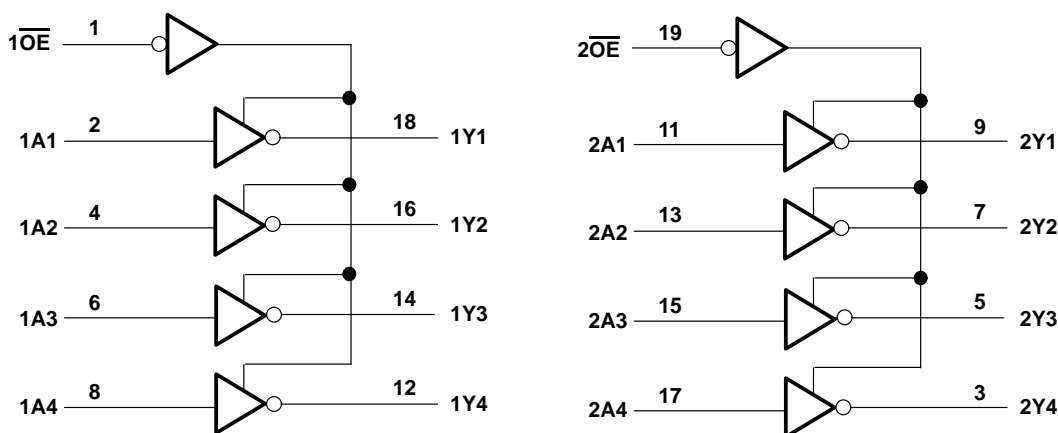
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#### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	–20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±75 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package	0.6 W
DW package	1.6 W
N package	1.3 W
PW package	0.7 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT240		SN74AHCT240		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		–8		–8	mA
I <sub>OL</sub>	Low-level output current		8		8	mA
Δt/Δv	Input transition rise or fall rate		20		20	ns/V
T <sub>A</sub>	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHCT240		SN74AHCT240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –50 μA	4.5 V	4.4	4.5		4.4		4.4		V
	I <sub>OH</sub> = –8 mA		3.94			3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V		.001	0.1		0.1		0.1	V
	I <sub>OL</sub> = 8 mA				0.36		0.44		0.44	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25		±2.5		±2.5	μA
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1		±1	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40		40	μA
ΔI <sub>CC</sub> <sup>†</sup>	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5		1.5	mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2.5	10				10	pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		3						pF

<sup>†</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

# SN54AHCT240, SN74AHCT240

## OCTAL BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT240				UNIT
				$T_A = 25^\circ\text{C}$			MIN	MAX
				MIN	TYP	MAX		
$t_{PLH}^*$	A	Y	$C_L = 15\text{ pF}$	5.4	7.4	1	8.5	ns
$t_{PHL}^*$				5.4	7.4	1	8.5	
$t_{PZH}^*$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	7.7	10.4	1	12	ns
$t_{PZL}^*$				7.7	10.4	1	12	
$t_{PHZ}^*$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	8.3	10.4	1	12	ns
$t_{PLZ}^*$				8.3	10.4	1	12	
$t_{PLH}$	A	Y	$C_L = 50\text{ pF}$	5.9	8.4	1	9.5	ns
$t_{PHL}$				5.9	8.4	1	9.5	
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	8.2	11.4	1	13	ns
$t_{PZL}$				8.2	11.4	1	13	
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	8.8	11.4	1	13	ns
$t_{PLZ}$				8.8	11.4	1	13	

\* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT240				UNIT
				$T_A = 25^\circ\text{C}$			MIN	MAX
				MIN	TYP	MAX		
$t_{PLH}$	A	Y	$C_L = 15\text{ pF}$	5.4	7.4	1	8.5	ns
$t_{PHL}$				5.4	7.4	1	8.5	
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	7.7	10.4	1	12	ns
$t_{PZL}$				7.7	10.4	1	12	
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	8.3	10.4	1	12	ns
$t_{PLZ}$				8.3	10.4	1	12	
$t_{PLH}$	A	Y	$C_L = 50\text{ pF}$	5.9	8.4	1	9.5	ns
$t_{PHL}$				5.9	8.4	1	9.5	
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	8.2	11.4	1	13	ns
$t_{PZL}$				8.2	11.4	1	13	
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	8.8	11.4	1	13	ns
$t_{PLZ}$				8.8	11.4	1	13	

output-skew characteristics,  $C_L = 50\text{ pF}$  (see Note 4)

PARAMETER	V <sub>CC</sub>	SN74AHCT240				UNIT
		T <sub>A</sub> = 25°C		MIN	MAX	
		MIN	MAX			
t <sub>sk(o)</sub> Output skew	5 V ± 0.5 V	1		1	ns	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

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noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

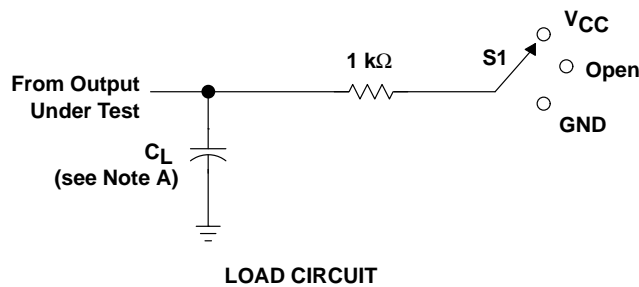
PARAMETER	SN74AHCT240			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic $V_{OL}$		0.6		V
$V_{OL(V)}$ Quiet output, minimum dynamic $V_{OL}$		-0.6		V
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$		4.1		V
$V_{IH(D)}$ High-level dynamic input voltage	2			V
$V_{IL(D)}$ Low-level dynamic input voltage			0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

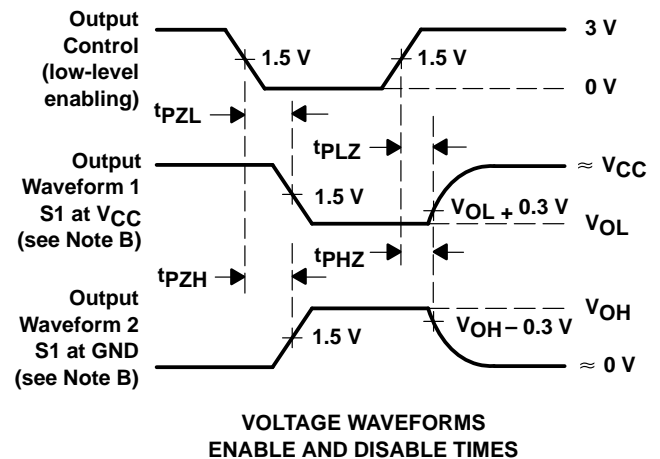
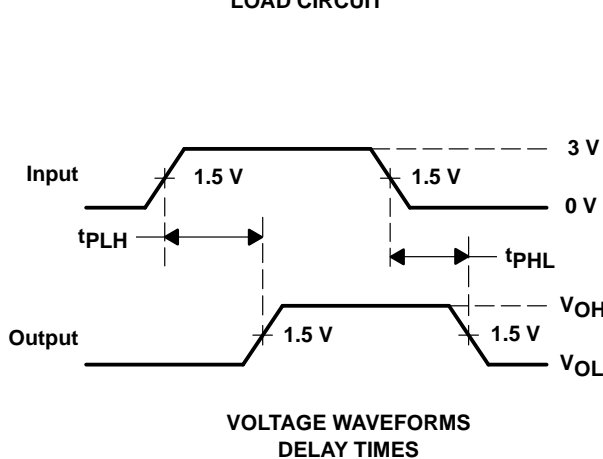
operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1\text{ MHz}$	10	pF

## PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .
  - D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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