

SN54AHCT257, SN74AHCT257 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

SCLS351A – MAY 1996 – REVISED NOVEMBER 1996

- Inputs Are TTL-Voltage Compatible
- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 4.5-V to 5.5-V V_{CC} operation.

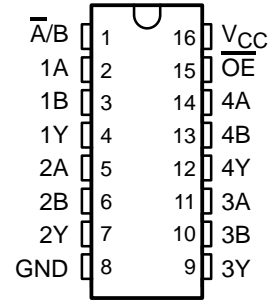
The 'AHCT257 are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable (\overline{OE}) input is at the high logic level.

The SN54AHCT257 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AHCT257 is characterized for operation from -40°C to 85°C .

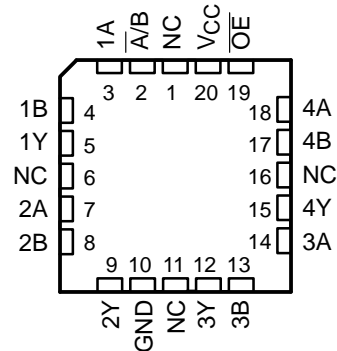
FUNCTION TABLE

INPUTS				OUTPUT Y
\overline{OE}	$\overline{A/B}$	A	B	
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

SN54AHCT257 . . . J OR W PACKAGE
SN74AHCT257 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT257 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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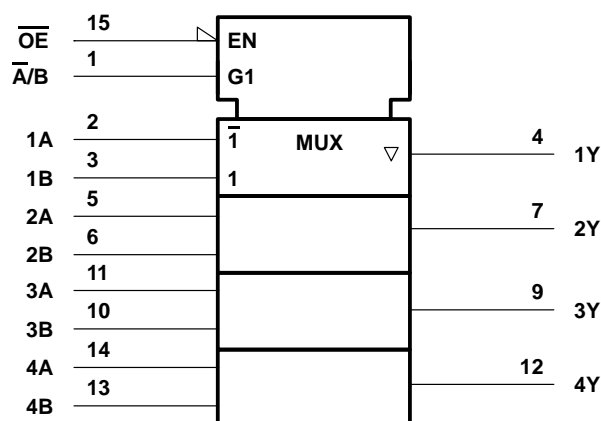
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WITH 3-STATE OUTPUTS

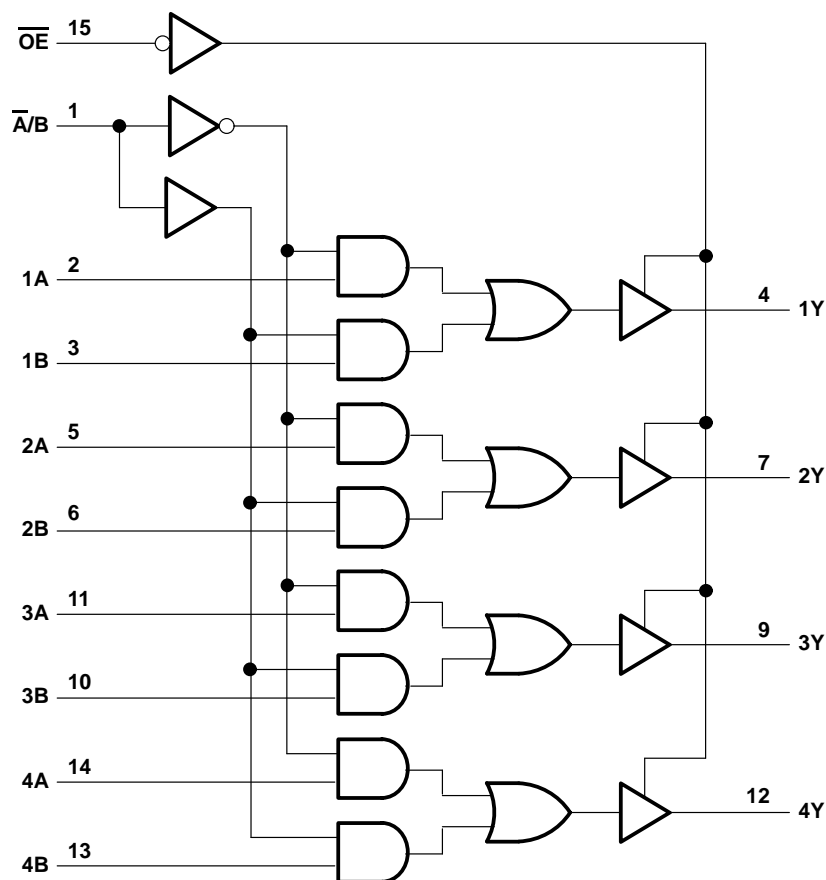
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	–20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
D package	1.3 W
DB package	0.55 W
N package	1.1 W
PW package	0.5 W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

	SN54AHCT257		SN74AHCT257		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage		0.8		0.8	V
V_I Input voltage	0	5.5	0	5.5	V
V_O Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH} High-level output current		–8		–8	mA
I_{OL} Low-level output current		8		8	mA
$\Delta t/\Delta v$ Input transition rise or fall time		20		20	ns/V
T_A Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHCT257		SN74AHCT257		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	4.5 V	4.4	4.5		4.4		4.4		V
	I _{OH} = -8 mA		3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
	I _{OL} = 8 mA				0.36		0.44		0.44	
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40		40	µA
ΔI _{CC} [†]	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			1.35		1.5		1.5	mA
I _{OZ}	V _I = V _{CC} or GND	5.5 V			±0.25		±2.5		±2.5	µA
C _i	V _I = V _{CC} or GND	5 V		2	10				10	pF

[†] This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT257					UNIT
				T _A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t _{PLH} *	A or B	Y	C _L = 15 pF					ns	
t _{PHL} *									
t _{PLH} *	\overline{A}/B	Y	C _L = 15 pF					ns	
t _{PHL} *									
t _{PZH} *	\overline{OE}	Y	C _L = 15 pF					ns	
t _{PZL} *									
t _{PHZ} *	\overline{OE}	Y	C _L = 15 pF					ns	
t _{PLZ} *									
t _{PLH}	A or B	Y	C _L = 50 pF					ns	
t _{PHL}									
t _{PLH}	\overline{A}/B	Y	C _L = 50 pF					ns	
t _{PLH}									
t _{PZH}	\overline{OE}	Y	C _L = 50 pF					ns	
t _{PZL}									
t _{PHZ}	\overline{OE}	Y	C _L = 50 pF					ns	
t _{PLZ}									

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT257					UNIT
				T _A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t _{PLH}	A or B	Y	C _L = 15 pF					ns	
t _{PHL}									
t _{PLH}	\overline{A}/B	Y	C _L = 15 pF					ns	
t _{PHL}									
t _{PZH}	\overline{OE}	Y	C _L = 15 pF					ns	
t _{PZL}									
t _{PHZ}	\overline{OE}	Y	C _L = 15 pF					ns	
t _{PLZ}									
t _{PLH}	A or B	Y	C _L = 50 pF					ns	
t _{PHL}									
t _{PLH}	\overline{A}/B	Y	C _L = 50 pF					ns	
t _{PLH}									
t _{PZH}	\overline{OE}	Y	C _L = 50 pF					ns	
t _{PZL}									
t _{PHZ}	\overline{OE}	Y	C _L = 50 pF					ns	
t _{PLZ}									

noise characteristics $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER		SN74AHCT257		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	-0.8		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}			V
$V_{IH(D)}$	High-level dynamic input voltage	2		V
$V_{IL(D)}$	Low-level dynamic input voltage		0.8	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

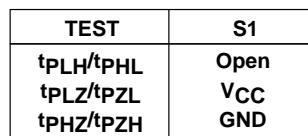
PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$		pF

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The diagram illustrates the timing relationships for a 1-bit D-type flip-flop. It features three signal traces: Input, In-Phase Output, and Out-of-Phase Output. The Input signal is a square wave with a high level of 1.5 V and a low level of 0 V. The In-Phase Output signal is a square wave that follows the Input signal, with a high level of V_{OH} and a low level of V_{OL} . The Out-of-Phase Output signal is a square wave that is the logical inverse of the In-Phase Output signal, with a high level of V_{OH} and a low level of V_{OL} . The propagation delay from the Input to the In-Phase Output is labeled t_{PLH} (low-to-high) and t_{PHL} (high-to-low). The propagation delay from the Input to the Out-of-Phase Output is labeled t_{PHL} (low-to-high) and t_{PLH} (high-to-low). The signal levels are indicated by dashed lines on the right side of the diagram.

The diagram shows three vertically aligned waveforms over a common time axis. The top waveform, labeled 'Output Control (low-level enabling)', is a square wave that transitions from 3 V to 0 V and back. The transition from 3 V to 0 V is marked with a time interval t_{PZL} , and the transition from 0 V to 3 V is marked with t_{PLZ} . The middle waveform, 'Output Waveform 1 S1 to V_{CC} (see Note B)', shows a signal that transitions from $\approx V_{CC}$ to $V_{OL} + 0.3$ V and back. The transition from $\approx V_{CC}$ to $V_{OL} + 0.3$ V is marked with t_{PLZ} , and the transition from $V_{OL} + 0.3$ V to $\approx V_{CC}$ is marked with t_{PHZ} . The bottom waveform, 'Output Waveform 2 S1 to GND (see Note B)', shows a signal that transitions from ≈ 0 V to $V_{OH} - 0.3$ V and back. The transition from ≈ 0 V to $V_{OH} - 0.3$ V is marked with t_{PZH} , and the transition from $V_{OH} - 0.3$ V to ≈ 0 V is marked with t_{PHZ} . All transitions are marked with a 1.5 V level on the signal lines.

NOTES:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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