

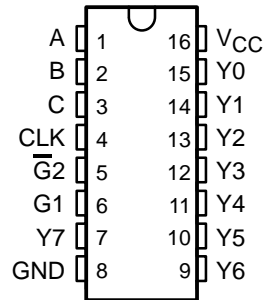
# SN74AS131A

## 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS REGISTERS

SDAS060C – APRIL 1982 – REVISED DECEMBER 1994

- Combines Decoder and 3-Bit Address Register
- Incorporates Two Enable Inputs to Simplify Cascading
- Package Options Include Plastic Small-Outline (D) Packages and Standard Plastic (N) 300-mil DIPs

D OR N PACKAGE  
(TOP VIEW)



### description

The SN74AS131A is a 3-line to 8-line decoder/demultiplexer with registers on the three address inputs. When the clock (CLK) input goes from low to high, the device acts as a decoder/demultiplexer and the address present at the select (A, B, and C) inputs is stored in the registers. Further address changes are ignored until the next rising transition of CLK. The output-enable (G1,  $\overline{G2}$ ) inputs control the state of the outputs independently of the select or CLK inputs. All of the outputs are high unless G1 is high and  $\overline{G2}$  is low. This device is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

The SN74AS131A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS						OUTPUTS							
CLK	ENABLE		SELECT										
	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
↑	H	L	L	L	L	L	H	H	H	H	H	H	H
↑	H	L	L	L	H	H	L	H	H	H	H	H	H
↑	H	L	L	H	L	H	H	L	H	H	H	H	H
↑	H	L	L	H	H	H	H	H	L	H	H	H	H
↑	H	L	H	L	H	H	H	H	H	L	H	H	H
↑	H	L	H	H	L	H	H	H	H	H	L	H	H
↑	H	L	H	H	H	H	H	H	H	H	H	L	H
L or H	H	L	X	X	X	Outputs corresponding to stored address = L; all others = H.							

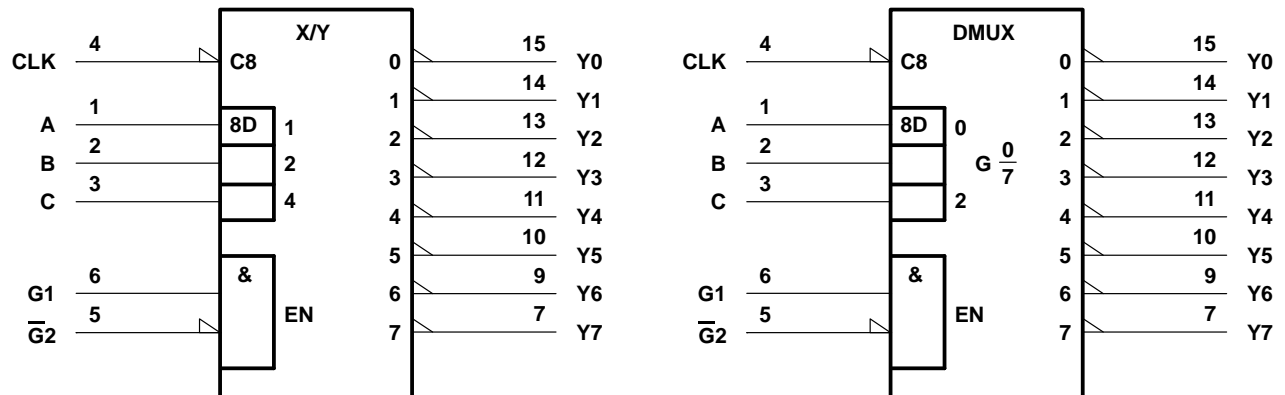
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## 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

### WITH ADDRESS REGISTERS

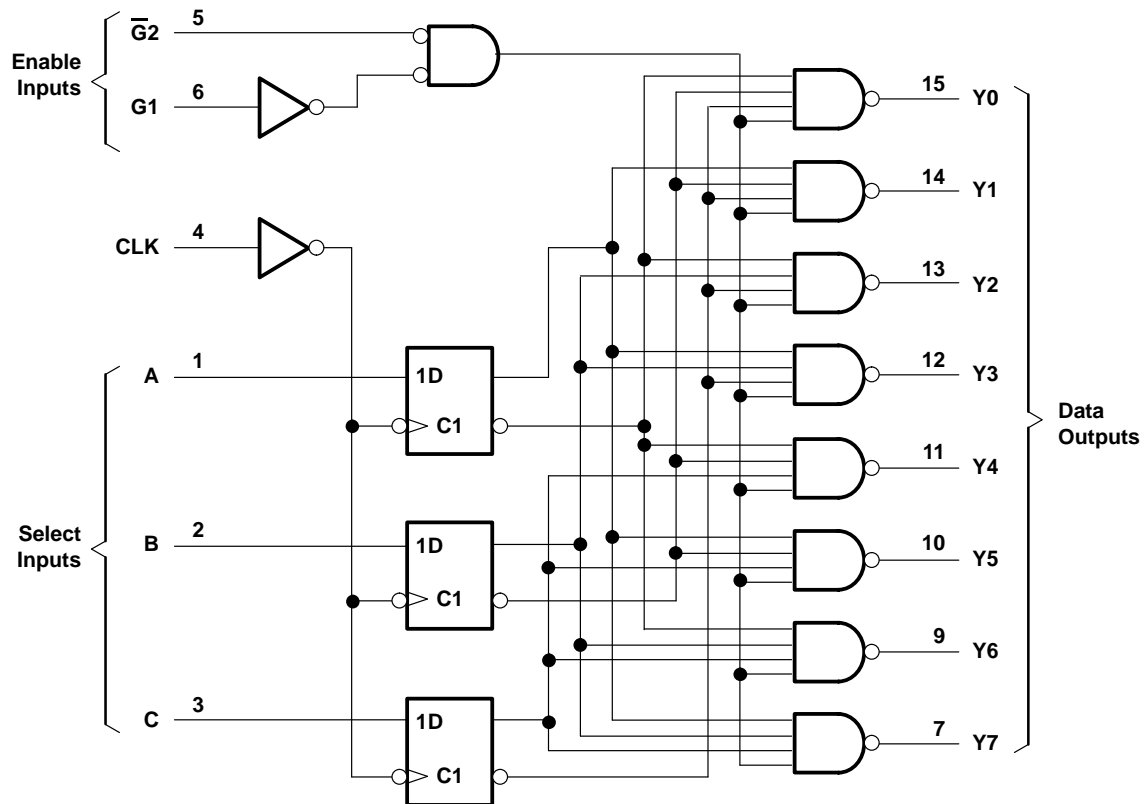
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#### logic symbols (alternatives)<sup>†</sup>



<sup>†</sup> These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)



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## 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS REGISTERS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{OH}$	High-level output current			–2	mA
$I_{OL}$	Low-level output current			20	mA
$f_{clock}$	Clock frequency	0		100	MHz
$t_w$	Pulse duration	CLK high		5	ns
		CLK low		5	
$t_{su}$	Setup time, A, B, and C before CLK <sup>↑</sup>	3.5			ns
$t_h$	Hold time, A, B, and C after CLK <sup>↑</sup>	0			ns
$T_A$	Operating free-air temperature	0		70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>‡</sup>	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.5$ V, $I_I = -18$ mA			–1.2	V
$V_{OH}$	$V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -2$ mA	$V_{CC} - 2$			V
$V_{OL}$	$V_{CC} = 4.5$ V, $I_{OL} = 20$ mA		0.35	0.5	V
$I_I$	$V_{CC} = 5.5$ V, $V_I = 7$ V			0.1	mA
$I_{IH}$	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20	μA
$I_{IL}$	$V_{CC} = 5.5$ V, $V_I = 0.4$ V			–0.5	mA
$I_{O}^{\S}$	$V_{CC} = 5.5$ V, $V_O = 2.25$ V	–30		–112	mA
$I_{CCH}$	$V_{CC} = 5.5$ V		15	29	mA
$I_{CCL}$	$V_{CC} = 5.5$ V		16	30	mA

<sup>‡</sup> All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

<sup>\S</sup> The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

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### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†		UNIT
			MIN	MAX	
f <sub>max</sub>			100		MHz
t <sub>PLH</sub>	CLK	Y	2	14.5	ns
t <sub>PHL</sub>			2	9.5	
t <sub>PLH</sub>	G1	Y	2	10	ns
t <sub>PHL</sub>			2	9	
t <sub>PLH</sub>	$\overline{G2}$	Y	2	7	ns
t <sub>PHL</sub>			2	8.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

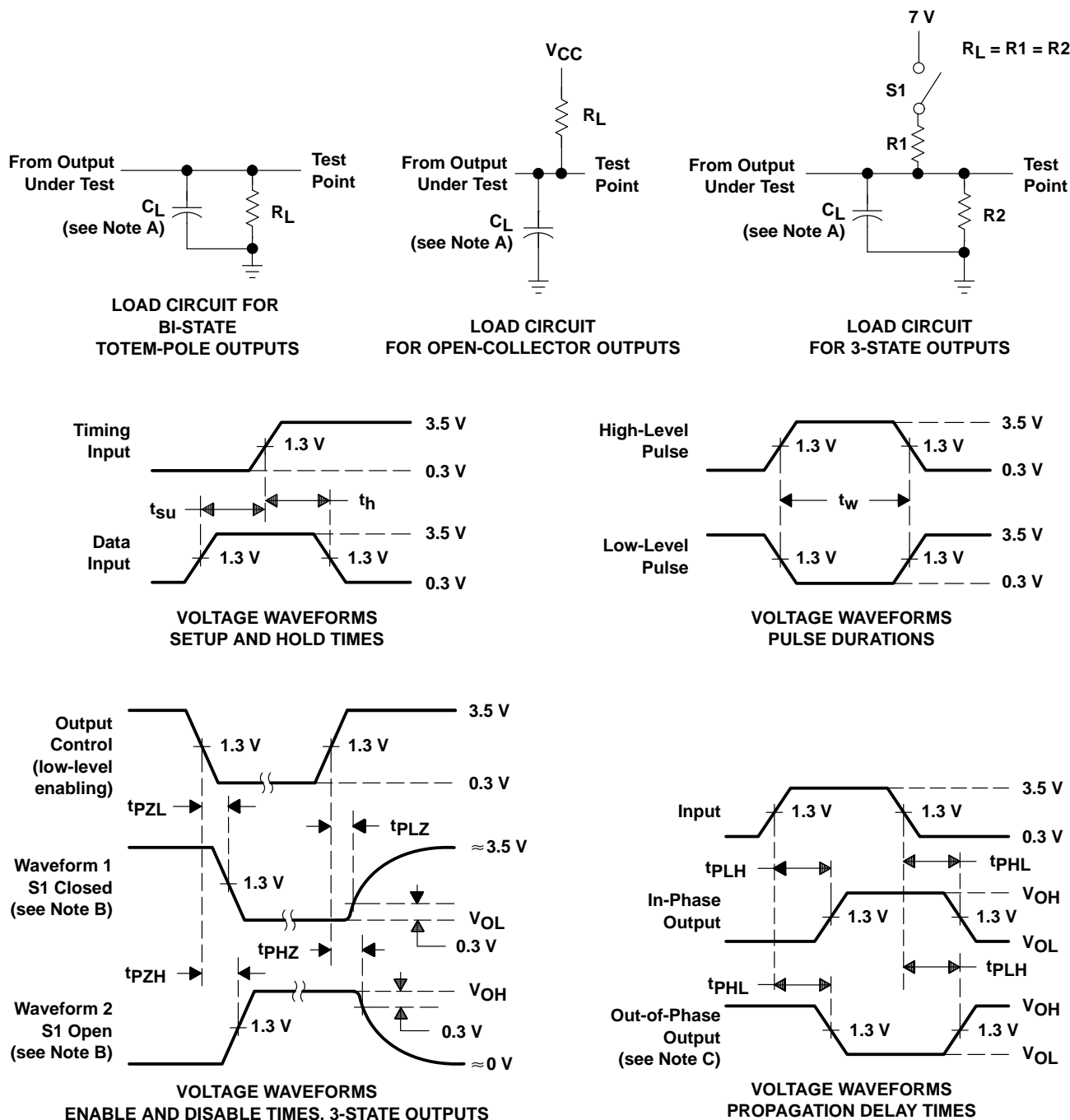


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## 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS REGISTERS

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### PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

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