

# SN54ALS857, SN74ALS857 HEX 2-TO-1 UNIVERSAL MULTIPLEXERS WITH 3-STATE OUTPUTS

SDAS170A – DECEMBER 1982 – REVISED JANUARY 1995

- Select True or Complementary Data
- Perform AND/NAND (Masking) of A or B Operand
- Cascadable to Expand Number of Operands
- Detect Zeros on A or B Operands
- 3-State Outputs Interface Directly With System Bus
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

## description

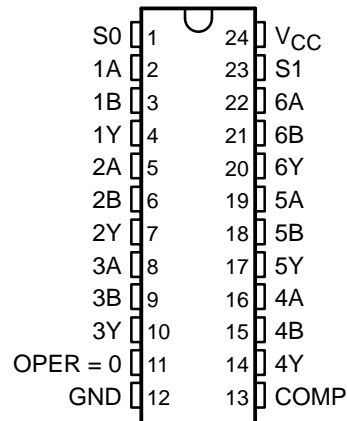
The 'ALS857 are hextuple 2-line to 1-line multiplexers with 3-state outputs. The devices can provide either true (COMP low) or inverted (COMP high) data at the Y outputs. In addition, the 'ALS857 perform the logical AND function ( $A \bullet B$ ) and the clear function as well. The four modes of operation are:

- Select A-data inputs
- Select B-data inputs
- AND A inputs with B inputs
- Clear

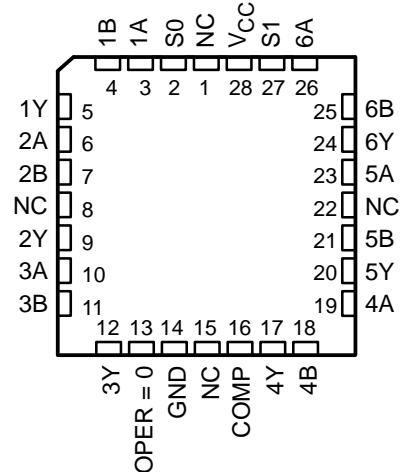
In either of the first two modes, OPER = 0 is high if all the selected A or B inputs are low. The six Y outputs and the OPER = 0 output are all 3-state and rated at 12-mA and 24-mA  $I_{OL}$  for the SN54ALS857 and SN74ALS857, respectively. All outputs can be placed in the high-impedance state by applying a high level to the COMP, S0, and S1 inputs simultaneously.

The SN54ALS857 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS857 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS857 . . . JT PACKAGE  
SN74ALS857 . . . DW OR NT PACKAGE  
(TOP VIEW)



SN54ALS857 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

# SN54ALS857, SN74ALS857

## HEX 2-TO-1 UNIVERSAL MULTIPLEXERS

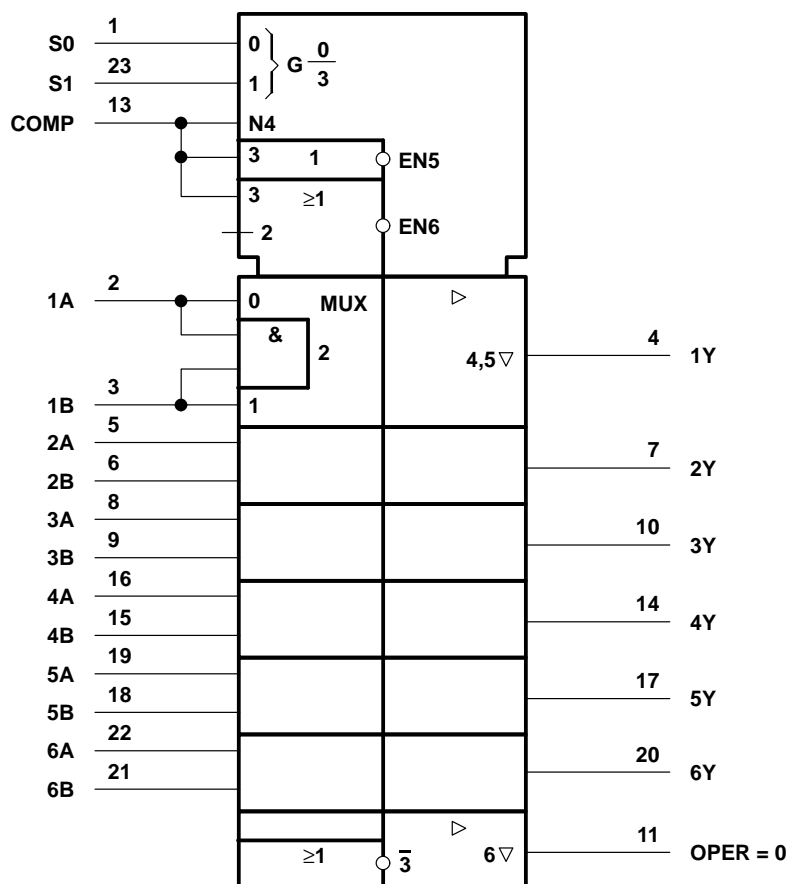
### WITH 3-STATE OUTPUTS

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FUNCTION TABLE

INPUTS			OUTPUTS	
COMP	S1	S0	Y	OPER = 0
L	L	L	A	H = all A inputs L
L	L	H	B	H = all B inputs L
L	H	L	$A \cdot B$	Z
L	H	H	L	L
H	L	L	$\bar{A}$	H = all A inputs L
H	L	H	$\bar{B}$	H = all B inputs L
H	H	L	$\overline{A \cdot B}$	Z
H	H	H	Z	Z

logic symbol†

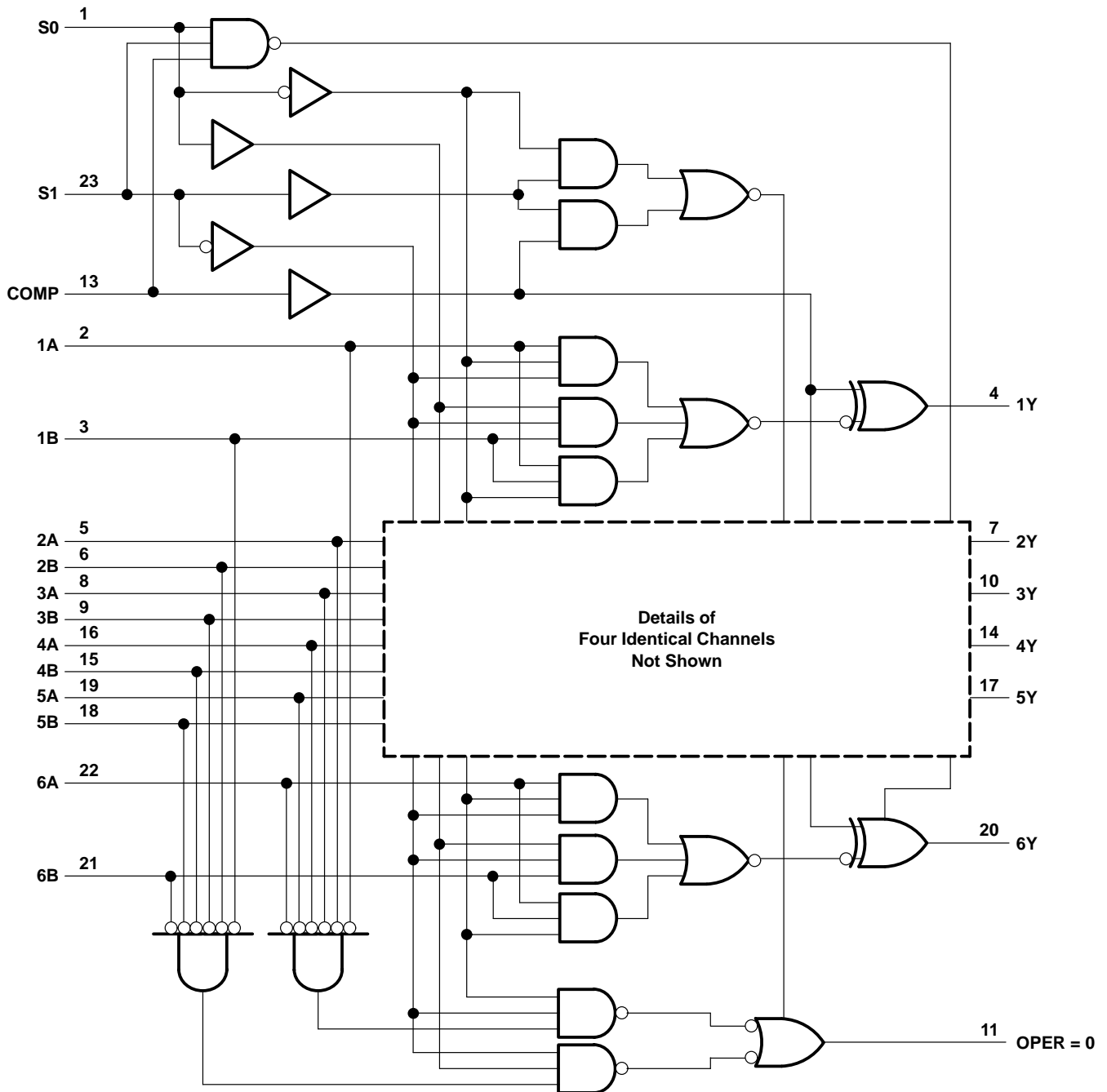


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the DW, JT, and NT packages.

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## logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, $T_A$ : SN54ALS857	–55°C to 125°C
SN74ALS857	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

		SN54ALS857			SN74ALS857			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			–1			–2.6	mA
$I_{OL}$	Low-level output current			12			24	mA
$T_A$	Operating free-air temperature	–55		125	0		70	°C

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS857			SN74ALS857			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$	$V_{CC} = 4.5$ V,	$I_I = -18$ mA			–1.5			–1.5	V
$V_{OH}$	$V_{CC} = 4.5$ V to 5.5 V,	$I_{OH} = -0.4$ mA	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5$ V	$I_{OH} = -1$ mA	2.4	3.3					
		$I_{OH} = -2.6$ mA				2.4	3.2		
$V_{OL}$	$V_{CC} = 4.5$ V	$I_{OL} = 12$ mA		0.25	0.4		0.25	0.4	V
		$I_{OL} = 24$ mA					0.35	0.5	
$I_{OZH}$	$V_{CC} = 5.5$ V,	$V_O = 2.7$ V			20			20	μA
$I_{OZL}$	$V_{CC} = 5.5$ V,	$V_O = 0.4$ V			–20			–20	μA
$I_I$	$V_{CC} = 5.5$ V,	$V_I = 7$ V			0.1			0.1	mA
$I_{IH}$	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			20			20	μA
$I_{IL}$	$V_{CC} = 5.5$ V,	$V_I = 0.4$ V			–0.2			–0.2	mA
$I_{O§}$	$V_{CC} = 5.5$ V,	$V_O = 2.25$ V	–15		–70	–15		–70	mA
$I_{CC}$	$V_{CC} = 5.5$ V, See Note 1	Outputs high		11	24		11	24	mA
		Outputs low		16	33		16	33	
		Outputs disabled		18	36		18	36	

‡ All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

NOTE 1:  $I_{CC}$  is measured with all possible inputs grounded while achieving the stated output conditions.



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## switching characteristics (see Figure 1)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX‡				UNIT
			SN54ALS857		SN74ALS857		
			MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B (COMP high)	Y (inverting)	2	35	4	25	ns
	A or B (COMP low)	Y (noninverting)	2	27	4	18	
	S0 or S1	Y	2	37	7	33	
	COMP		2	26	6	18	
	A or B	OPER = 0	2	45	5	37	
	S0 to S1		2	30	5	23	
t <sub>en</sub>	S0 to S1	Y	2	38	7	35	ns
t <sub>dis</sub>			2	43	2	23	
t <sub>en</sub>	COMP	Y	2	37	8	24	ns
t <sub>dis</sub>			2	45	6	21	
t <sub>en</sub>	S0	OPER = 0	2	29	6	20	ns
t <sub>dis</sub>			2	42	11	27	
t <sub>en</sub>	S1	OPER = 0	2	28	6	25	ns
t <sub>dis</sub>			2	37	3	19	
t <sub>en</sub>	COMP	OPER = 0	2	43	9	25	ns
t <sub>dis</sub>			2	36	6	20	

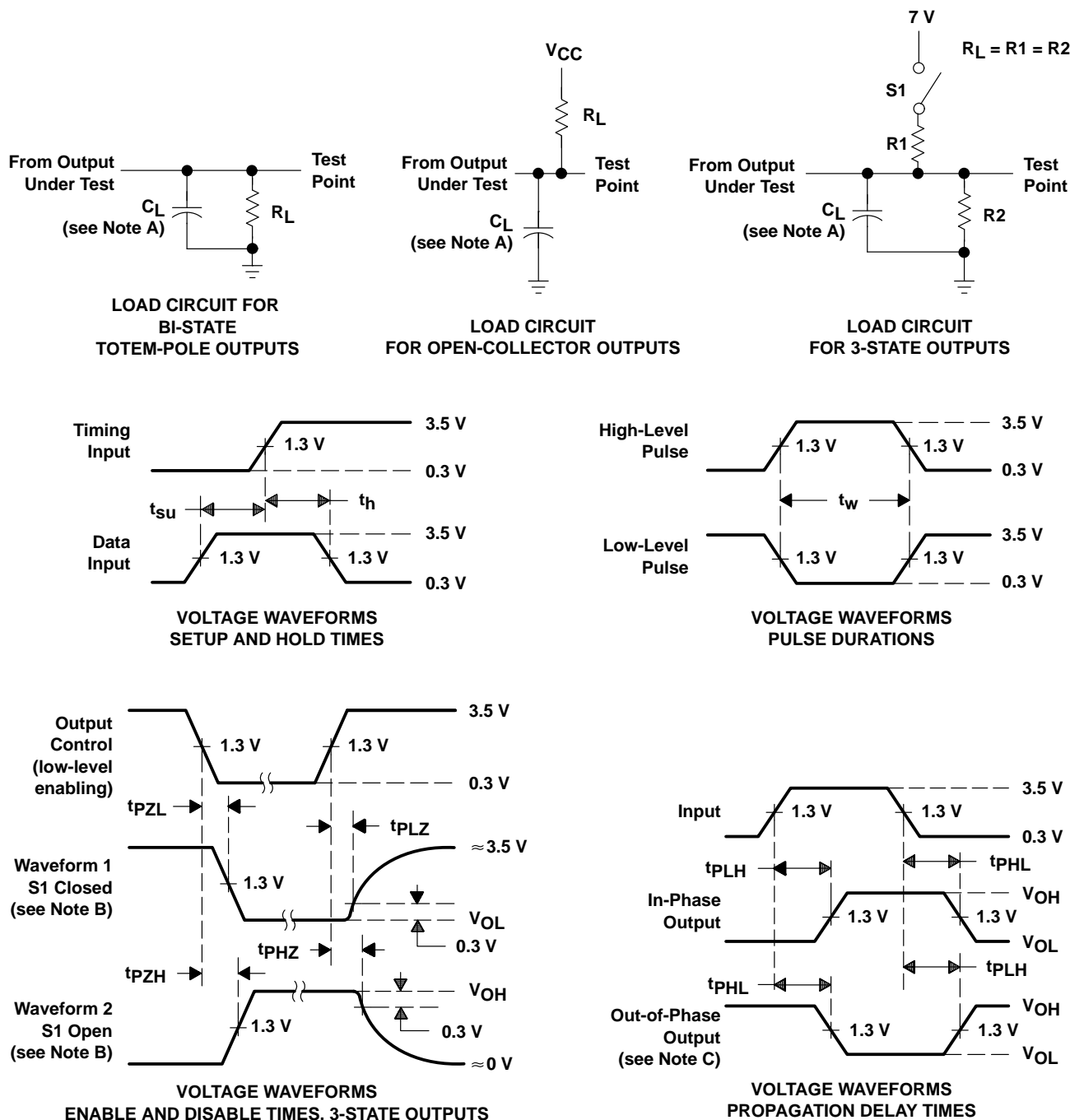
† t<sub>pd</sub> = t<sub>PLH</sub> or t<sub>PHL</sub>, t<sub>en</sub> = t<sub>PZH</sub> or t<sub>PZL</sub>, t<sub>dis</sub> = t<sub>PHZ</sub> or t<sub>PLZ</sub>

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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