

# SN54AS866, SN74AS866A 8-BIT MAGNITUDE COMPARATORS

SDAS183A – DECEMBER 1982 – REVISED JUNE 1990

- Package Options Include Plastic Small Outline Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic DIPs
- Input and Output Latches with Active-High Enables
- Fast Compare to Zero
- Arithmetic and Logical Comparison
- Open-Collector P = Q Output

## description

These Advanced Schottky devices are capable of performing high-speed arithmetic or logical comparisons on two 8-bit binary or two's complement words. Three fully decoded decisions about words P and Q are externally available at the outputs. These devices are fully expandable to any word length by connecting the totem pole P>Q and P<Q outputs of each stage to the P>Q and P<Q inputs of the next higher-order stage. The cascading paths are implemented with only a two-gate-level delay to reduce overall comparison times for long words. The open-collector P=Q output may be wire-ANDed together.

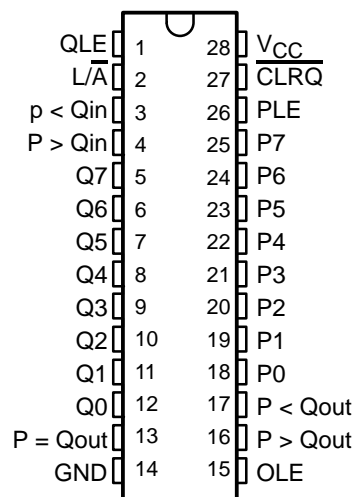
Both input words P and Q plus all three outputs (P>Q, P<Q, and P = Q) are equipped with latches to provide the designer with temporary data storage for avoiding race conditions. The enable circuitry is implemented with minimal delay times to enhance performance when the devices are cascaded for longer word lengths. Each latch is transparent when the appropriate latch enable, PLE, QLE, or OLE is high.

The enable inputs PLE and QLE and data inputs P and Q utilize pnp input transistors to reduce the low-level input current requirement to typically -0.25 mA, which minimizes loading effects.

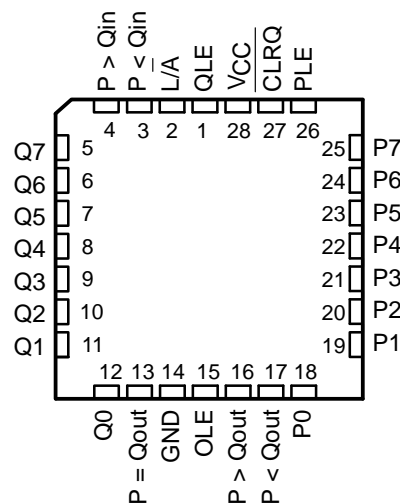
The Q register may be cleared to zero for a fast comparison of the P word to zero.

The SN54AS866 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74AS866A is characterized for operation from 0°C to 70°C.

SN54AS866 . . . JD PACKAGE  
SN74AS866A . . . N PACKAGE  
(TOP VIEW)



SN54AS866 . . . FK PACKAGE  
SN74AS866A . . . FN PACKAGE  
(TOP VIEW)



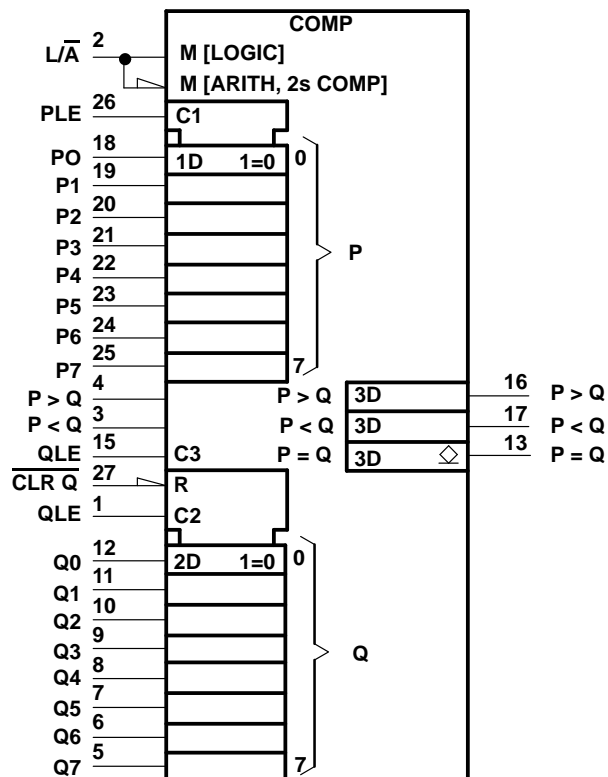


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## 8-BIT MAGNITUDE COMPARATORS

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logic symbol†



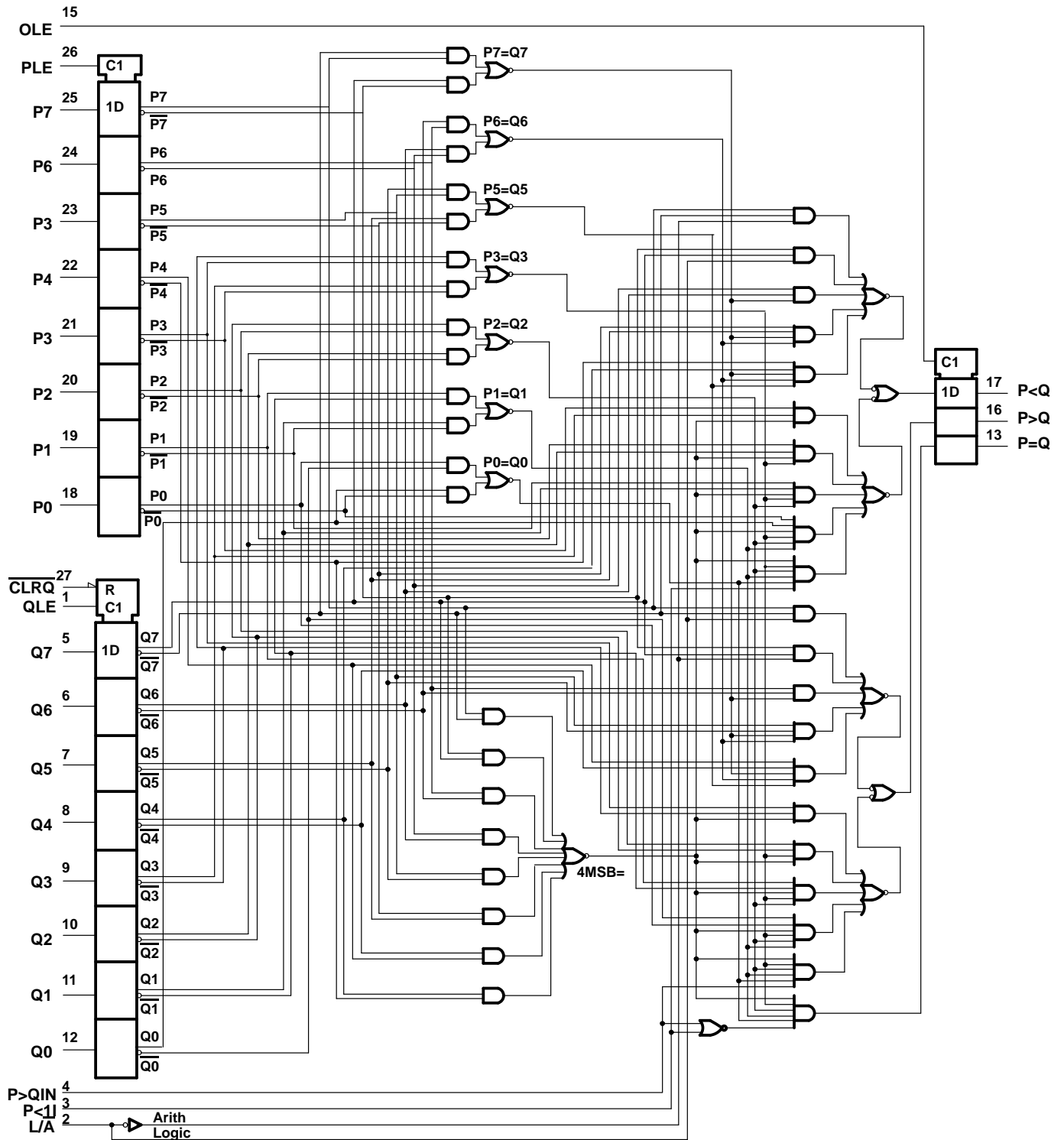
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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## logic diagram (positive logic)





# SN54AS866, SN74AS866A

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FUNCTION TABLE

COMPARISON	$L/\bar{A}$	DATA INPUTS P0–P7, Q0–Q7	INPUTS		OUTPUTS		
			P>Q	P<Q	P>Q	P<Q	P=Q
Logical	H	P>Q	X	X	H	L	L
Logical	H	P<Q	X	X	L	H	L
Logical	H	P=Q	L	L	L	L	H
Logical	H	P=Q	L	H	L	H	L
Logical	H	P=Q	H	L	H	L	L
Logical	H	P=Q	H	H	H	H	L
Arithmetic	L	P AG Q	X	X	H	L	L
Arithmetic	L	Q AG P	X	X	L	H	L
Arithmetic	L	P=Q	L	L	L	L	H
Arithmetic	L	P=Q	L	H	L	H	L
Arithmetic	L	P=Q	H	L	H	L	L
Arithmetic	L	P=Q	H	H	H	H	L

AG = arithmetically greater than

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$	7 V
Input voltage	7 V
Off-state output voltage, P = Q output	7 V
Operating free-air temperature range: SN54AS866	–55°C to 125°C
SN74AS866A	0°C to 70°C
Storage temperature range	–65°C to 150°C

### recommended operating conditions

	SN54AS866			SN74AS866A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.8			0.8	V
$I_{OH}$ High-level output current, all outputs except P=Q			–2			–2	mA
$V_{OH}$ High-level output voltage, P=Q output			5.5			5.5	V
$I_{OL}$ Low-level output current			20			20	mA
$t_{su}$ Setup time to PLE, OLE, OLE↓	2			2			ns
$t_h$ Hold time after PLE, QLE, OLE↓	4			4			
$t_A$ Operating free-air temperature	–55		125	0	70		°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS866		SN74AS866A		UNIT		
				MIN	TYP†	MAX	MIN		TYP†	MAX
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = −18 mA	−1.2		−1.2		V		
V <sub>OH</sub>	P>Q, P<Q	V <sub>CC</sub> = 4.5 V to 5.5 V,	I <sub>OH</sub> = −2 mA	V <sub>CC</sub> −2		V <sub>CC</sub> −2				
I <sub>OH</sub>	P=Q only	V <sub>CC</sub> = 4.5 V,	V <sub>OH</sub> = 5.5 V	0.25		0.25		mA		
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 20 mA	0.35	0.5	0.35	0.5	V		
I <sub>I</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 7 V	0.1		0.1		mA		
I <sub>IH</sub>	L/A, OLE	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V	40		40		μA		
	Others			20		20				
I <sub>IL</sub>	L/A, OLE, P>Q <sub>in</sub> , P<Q <sub>in</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V	−4		−4		mA		
	CLRQ			−2		−2				
	P, Q, PLE, QLE			−0.25		−1			−0.25	
I <sub>O</sub> ‡		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	−20	−112	−20	−112	mA		
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V,	See Note 1	160	240	160	240	mA		

NOTE 1:  $I_{CC}$  is measured with all inputs high except L/A, which is low.

## switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX§						UNIT
			SN54AS866			SN74AS866A			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t <sub>PLH</sub>	L/ $\bar{A}$	P<Q, P>Q	1	8.5	14	1	8.5	19	ns
t <sub>PHL</sub>			1	7.5	14	1	7	13	
t <sub>PLH</sub>	P<Q, P>Q		1	5	10	1	5	8	ns
t <sub>PHL</sub>			1	5.5	10	1	5.5	8	
t <sub>PLH</sub>	Any P or Q Data Input		1	13.5	21	1	13.5	17.5	ns
t <sub>PHL</sub>			1	10	17	1	10	15	
t <sub>PLH</sub>	CLRQ		1	16	21	1	16	20	ns
t <sub>PHL</sub>			1	12	17	1	12	16	

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 280 Ω, T <sub>A</sub> = MIN to MAX§						UNIT
			SN54AS866			SN74AS866A			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t <sub>PLH</sub>	P<Q,	P=Q	1	6.5	12	1	6.5	16	ns
t <sub>PHL</sub>	P>Q		1	8	14	1	8	14	
t <sub>PLH</sub>	Any P or Q Data Input	P=Q	1	10	15	1	10	17	ns
t <sub>PHL</sub>			1	9	14	1	9	14	
t <sub>PLH</sub>	CLRQ	P=Q	1	12	17	1	12	24	ns
t <sub>PHL</sub>			1	13	18	1	13	21	

† All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit,  $I_{OS}$ .

§ For conditions shown MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuit and voltage waveforms are shown in Section 1 of the *ALS/AS Logic Data Book*, 1986.

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### TYPICAL APPLICATION DATA

This sequence of comparisons illustrates how the  $\overline{\text{CLRQ}}$  function can be used to perform dual comparisons of the varying P terms (P0, P1, etc.). When  $\overline{\text{CLRQ}}$  is high, the P term is compared to the Q term. When  $\overline{\text{CLRQ}}$  is taken low, the P term is compared to zero. This or similar sequences can enhance performance and reduce package count to perform value range checks.

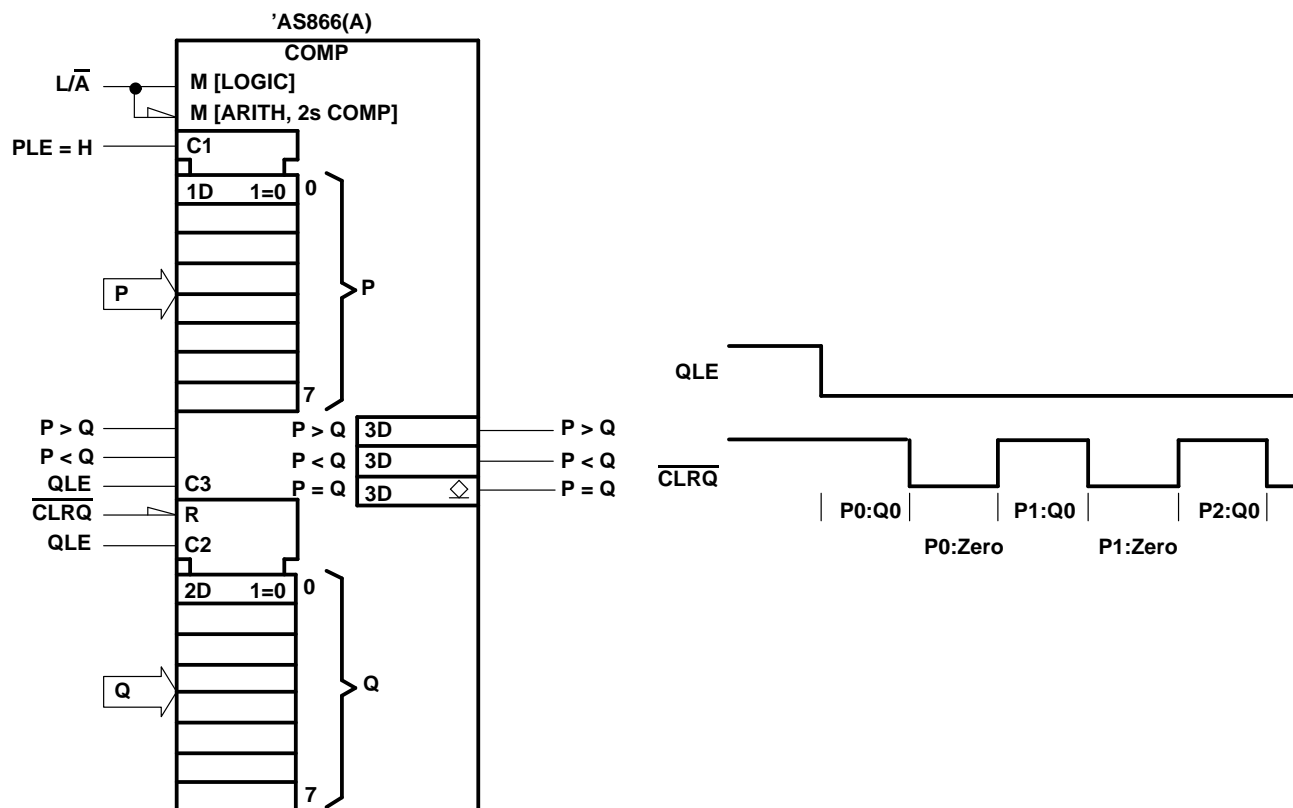


Figure 1. Magnitude Comparisons Combined With Quick Comparisons to Zero (Range Verifications)



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