

# SN54ALS114A, SN74ALS114A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

SDAS201 – D2661, DECEMBER 1982 – REVISED MAY 1986

- Fully Buffered to Offer Maximum isolation from External Disturbance
- Package Options include Plastic Small Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Typical Maximum Clock Frequency 30 MHz
- Typical Power Dissipation per Flip-Flop 6 mW
- Dependable Texas Instruments Quality and Reliability

## description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

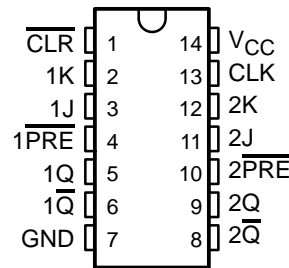
The SN54ALS114A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS114A is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE

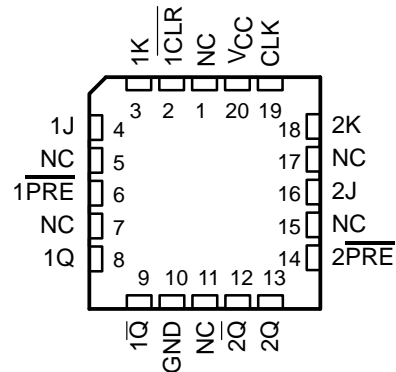
INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H	↓	L	L	Q <sub>0</sub>	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q <sub>0</sub>	$\bar{Q}_0$

<sup>†</sup> The output levels in this configuration are not guaranteed to meet the minimum levels for  $V_{OH}$  if the lows at Preset and Clear are near  $V_{IL}$  maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

SN54ALS114A ... J PACKAGE  
SN74ALS114A ... D OR N PACKAGE  
(TOP VIEW)

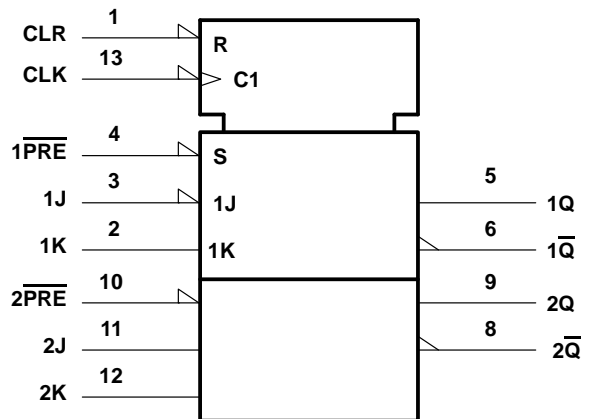


SN54ALS114A ... FK PACKAGE  
(TOP VIEW)



NC—No internal connection

## logic symbol<sup>‡</sup>



<sup>‡</sup> This symbol is in accordance with ANSI/IEEE Std 911-1984 and IEC Publication 617-12.

Pin numbers are for D, J, and N packages.

## SDAS201 = D2661. DECEMBER 1982 = REVISED MAY 1986

The diagram illustrates the internal logic of a J-K flip-flop, which is composed of two cross-coupled SR flip-flops. The inputs are J, K, PRE (active-low), and CLK. The outputs are Q and Q-bar. The logic involves several AND gates, OR gates, and NAND gates, along with inverters and a cross-coupled feedback loop. The PRE input is active-low, and the CLK input is a clock signal. The output Q is connected to the Q-bar input of the second SR flip-flop, and vice versa, forming a cross-coupled structure. The J and K inputs are connected to the J and K inputs of the two SR flip-flops, respectively. The PRE input is connected to the PRE inputs of both SR flip-flops. The CLK input is connected to the CLK inputs of both SR flip-flops. The output Q is connected to the Q-bar input of the second SR flip-flop, and vice versa, forming a cross-coupled structure. The J and K inputs are connected to the J and K inputs of the two SR flip-flops, respectively. The PRE input is connected to the PRE inputs of both SR flip-flops. The CLK input is connected to the CLK inputs of both SR flip-flops.

Supply voltage, $V_{CC}$	7 V
Input voltage	7 V
Operating free-air temperature range: SN54ALS114A	-55°C to 125°C
SN74ALS114A	0°C to 70°C
Storage temperature range	-65°C to 150°C

			SN54ALS114A			SN74ALS114A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage		2			2			V
V <sub>IL</sub>	Low-level input voltage				0.7			0.8	V
I <sub>OH</sub>	High-level output current				−0.4			−0.4	mA
I <sub>OL</sub>	Low-level output current				4			8	mA
f <sub>clock</sub>	Clock frequency		0		25	0		30	mHz
t <sub>w</sub>	Pulse duration	PRE or CLR low	20			10			ns
		CLK high	20			16.5			
		CLK low	20			16.5			
t <sub>su</sub>	Setup time before CLK↓	Data	25			22			ns
		PRE or CLR inactive	25			20			
t <sub>h</sub>	Hold time, data after CLK↓		0			0			ns
T <sub>A</sub>	Operating free-air temperature		−55		125	0		70	°C

**SN54ALS114A, SN74ALS114A**  
**DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS**  
**WITH PRESET, COMMON CLEAR, AND COMMON CLOCK**

SDAS201 – D2661, DECEMBER 1982 – REVISED MAY 1986

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		SN54ALS114A			SN74ALS114A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = −18 mA	−1.5			−1.5			V
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V to 5.5 V,	I <sub>OH</sub> = −0.4 mA	V <sub>CC</sub> −2			V <sub>CC</sub> −2			V
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 4 mA	0.25 0.4						V
		V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 8 mA				0.35 0.5			
I <sub>I</sub>	J, K, or CLK	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 7 V	0.1			0.1			mA
	PRE or CLR			0.2			0.2			
I <sub>IH</sub>	J, K, or CLK	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V	20			20			μA
	PRE or CLR			40			40			
I <sub>IL</sub>	J, K, or CLK	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V	−0.2			−0.2			mA
	PRE or CLR			−0.4			−0.4			
I <sub>O</sub> ‡		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	−30	−112		−30	−112		mA
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V,	See Note 1	2.5	4.5		2.5	4.5		mA

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

NOTE 1:  $I_{CC}$  is measured with J, K, CLK, and PRE grounded, then with J, K, CLK, and CLR grounded.

**switching characteristics (see Note 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX				UNIT
			SN54ALS114A		SN74ALS114A		
			MIN	MAX	MIN	MAX	
f <sub>max</sub>			25		30		MHz
t <sub>PLH</sub>	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	3	29	3	15	ns
t <sub>PHL</sub>			4	30	4	18	
t <sub>PLH</sub>	CLK	Q or $\overline{\text{Q}}$	3	28	3	15	ns
t <sub>PHI</sub>			5	31	5	19	

NOTE 2: Load circuit and Voltage waveforms are shown in Section 1.

## **IMPORTANT NOTICE**

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

**TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.**

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.