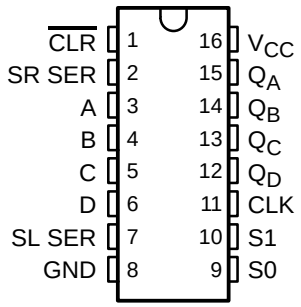
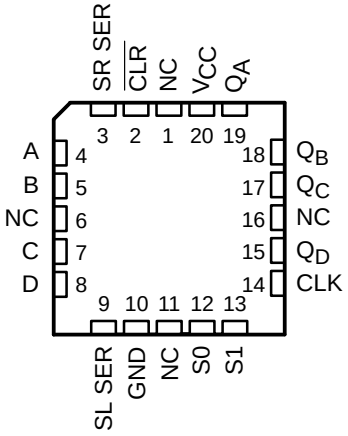
- **Parallel-to-Serial, Serial-to-Parallel Conversions**
- **Left or Right Shifts**
- **Parallel Synchronous Loading**
- **Direct Overriding Clear**
- **Temporary Data-Latching Capability**
- **Package Options Include Plastic Small-Outline Packages (D), Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AS194 . . . J PACKAGE
SN74AS194 . . . D OR N PACKAGE
(TOP VIEW)



SN54AS194 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These 4-bit bidirectional universal shift registers feature parallel outputs, right-shift and left-shift serial (SR SER, SL SER) inputs, operating-mode-control (S0, S1) inputs, and a direct overriding clear ($\overline{CLR}$) line. The registers have four distinct modes of operation:

- Inhibit clock (temporary data latch/do nothing)
- Shift right (in the direction Q_A toward Q_D)
- Shift left (in the direction Q_D toward Q_A)
- Parallel (broadside) load

Parallel synchronous loading is accomplished by applying the four bits of data and taking both S0 and S1 high. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock (CLK) input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial inputs. Clocking of the flip-flop is inhibited when both mode-control inputs are low.

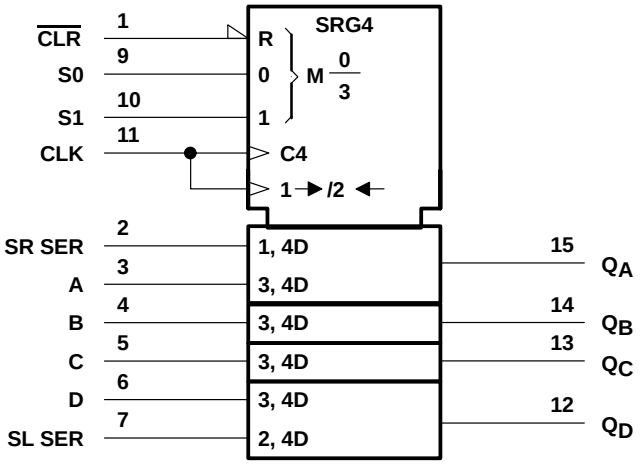
The SN54AS194 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AS194 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS										OUTPUTS			
$\overline{CLR}$	MODE		CLK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

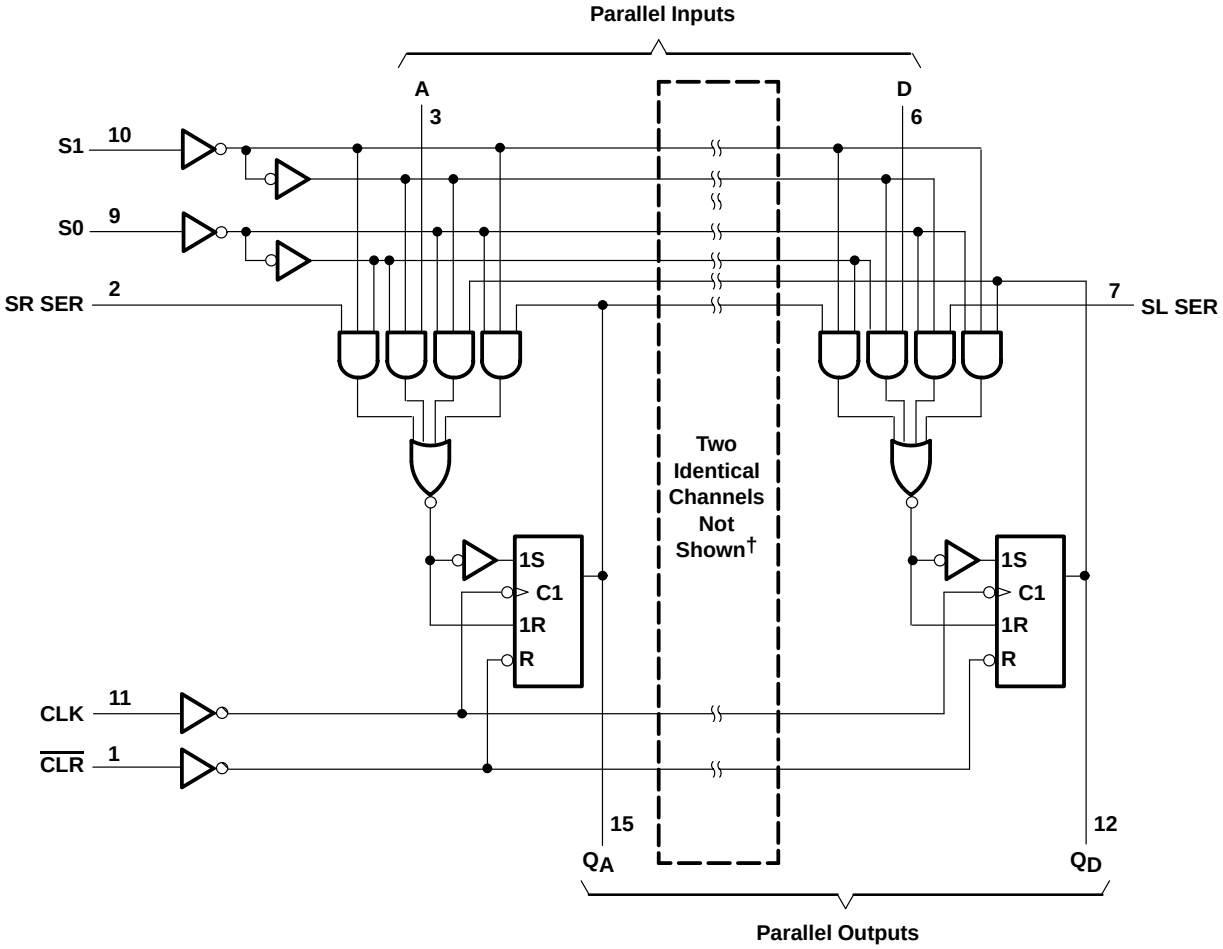
H = high level (steady state); L = low level (steady state); X = irrelevant (any input, including transitions); ↑ = transition from low to high level; a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively; Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established; Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, respectively, before the most recent ↑ transition of the clock.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



† I/O ports not shown: Q_B (14) and Q_C (13)
Pin numbers shown are for the D, J, and N packages.

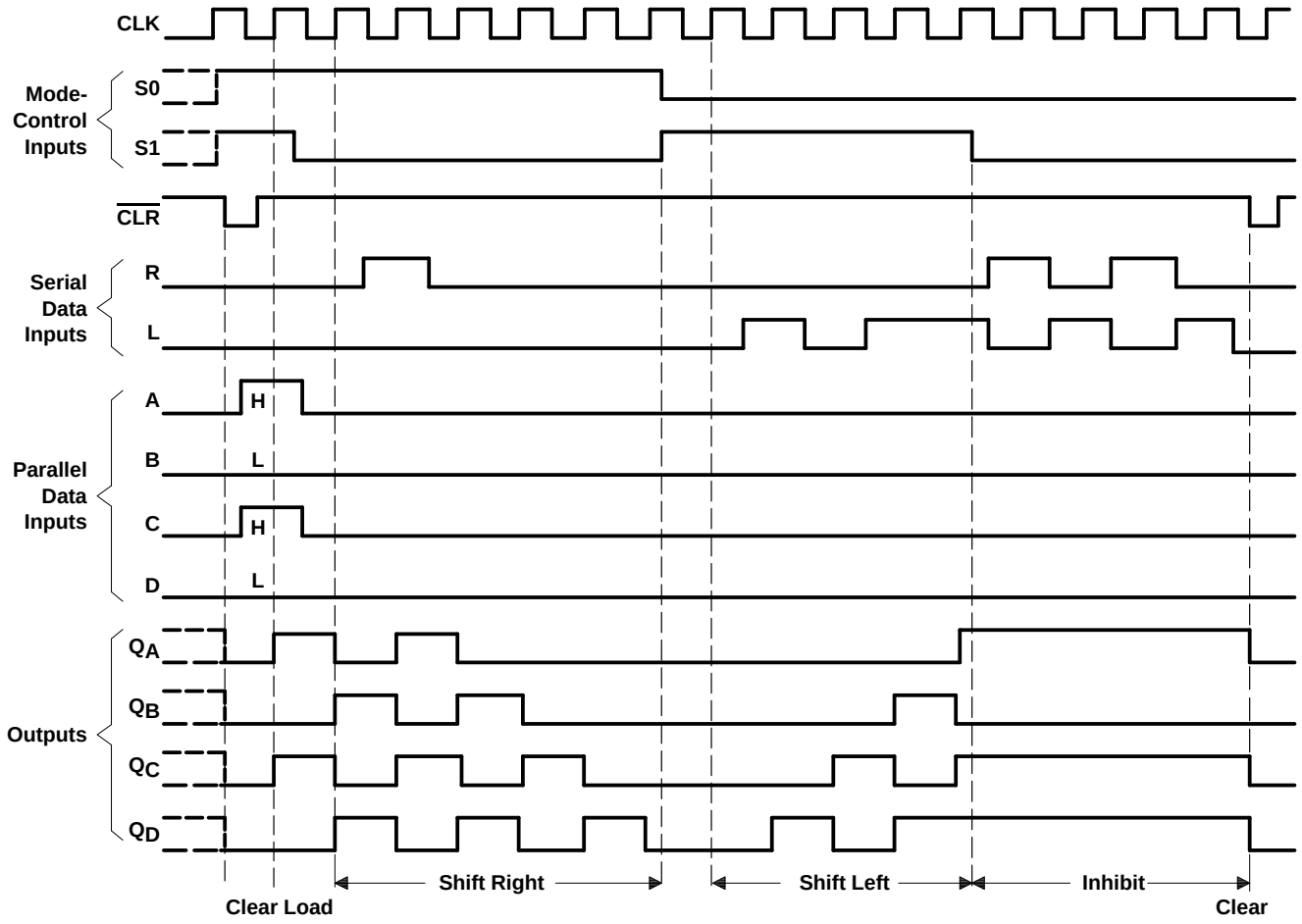


Figure 1. Typical Clear, Load, Right-Shift, and Clear Sequences

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Operating free-air temperature range, T_A: SN54AS194 . . . . . –55°C to 125°C
SN74AS194 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54AS194			SN74AS194			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				–2			–2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}*	Clock frequency		0		75	0		80	MHz
t_w*	Pulse duration	$\overline{CLR}$	4			4.5			ns
		CLK high	4			4			
		CLK low	6			7			
t_{su}*	Setup time before CLK↑	Select	9			9.5			ns
		Data	3.5			4			
		Clear inactive state	6			6			
t_h*	Hold time, data after CLK↑		0.5			0.5			ns
T_A	Operating free-air temperature		–55		125	0		70	°C

* On products compliant to MIL-STD-883, Class B, these parameters are based on characterization data, but are not production tested.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS194			SN74AS194			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –2 mA	V_{CC}–2			V_{CC}–2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	Data, CLK, $\overline{CLR}$	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	Mode, SL, SR					0.2			0.2	
I_{IH}	Data, CLK, $\overline{CLR}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
	Mode, SL, SR					40			40	
I_{IL}	Data, CLK, $\overline{CLR}$	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.5			–0.5	mA
	Mode, SL, SR					–1			–1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	–30		–112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		30	49		30	43	mA
			Outputs low		38	60		38	53	

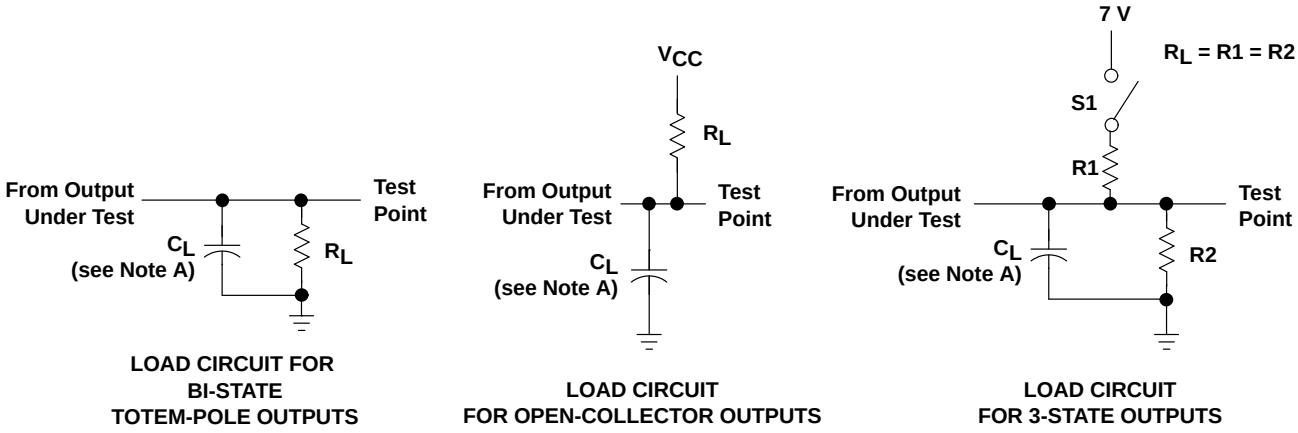
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†				UNIT
			SN54AS194		SN74AS194		
			MIN	MAX	MIN	MAX	
f_{max}*			75		80		MHz
t_{PLH}	CLK	Any Q	2.5	8	3	7	ns
t_{PHL}			2.5	8	3	7	
t_{PHL}	$\overline{CLR}$	Any Q	3.5	13	4	12	ns

* On products compliant to MIL-STD-883, Class B, these parameters are based on characterization data, but are not production tested.
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

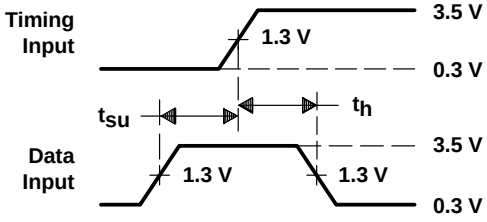
PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



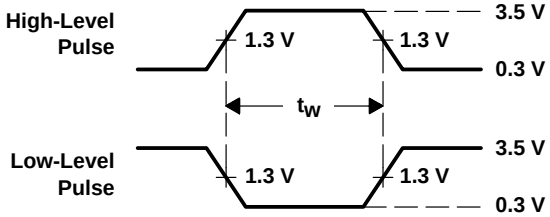
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

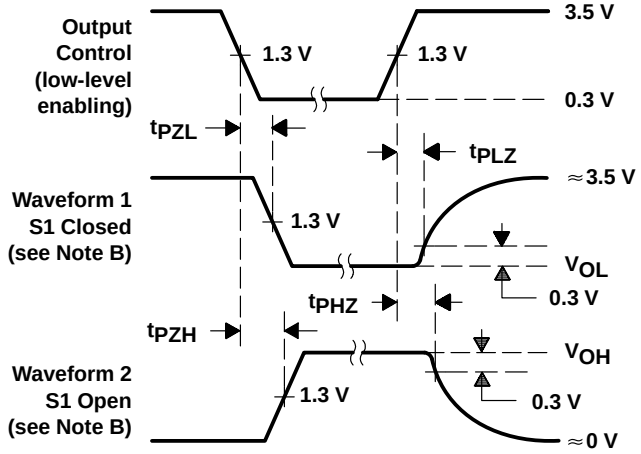
LOAD CIRCUIT FOR 3-STATE OUTPUTS



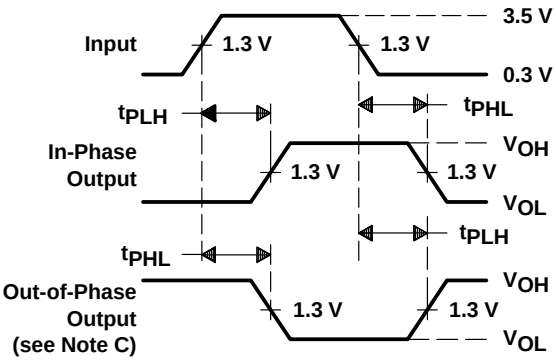
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

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