

SN54ALS259, SN74ALS259 8-BIT ADDRESSABLE LATCHES

SDAS217A – DECEMBER 1982 – REVISED DECEMBER 1994

- **8-Bit Parallel-Out Storage Register**
Performs Serial-to-Parallel Conversion With Storage
- **Asynchronous Parallel Clear**
- **Active-High Decoder**
- **Enable/Disable Input Simplifies Expansion**
- **Expandable for n-Bit Applications**
- **Four Distinct Functional Modes**
- **Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

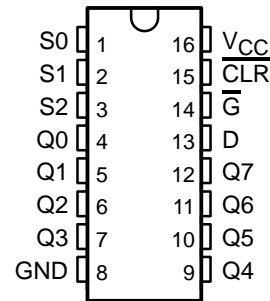
description

These 8-bit addressable latches are designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches and being a 1-of-8 decoder or demultiplexer with active-high outputs.

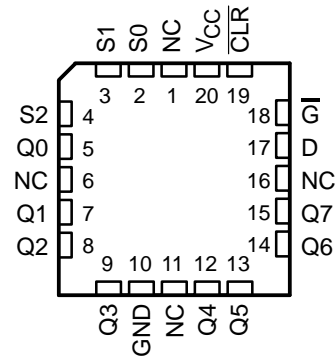
Four distinct modes of operation are selectable by controlling the clear ($\overline{\text{CLR}}$) and enable ($\overline{\text{G}}$) inputs as shown in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch follows the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, $\overline{\text{G}}$ should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output follows the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

The SN54ALS259 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS259 is characterized for operation from 0°C to 70°C .

SN54ALS259 . . . J PACKAGE
SN74ALS259 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS259 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

Function Tables

FUNCTION

INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
$\overline{\text{CLR}}$	$\overline{\text{G}}$			
H	L	D	Q_{iO}	Addressable latch
H	H	Q_{iO}	Q_{iO}	Memory
L	L	D	L	8-line demultiplexer
L	H	L	L	Clear

D = the level at the data input.

Q_{iO} = the level of Q_i ($i = Q, 1, \dots, 7$ as appropriate) before the indicated steady-state input conditions were established.

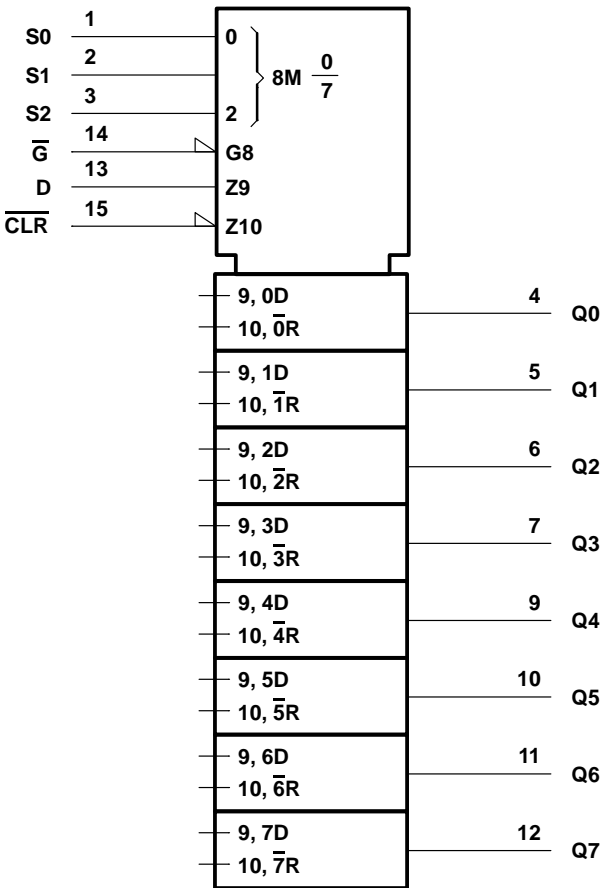
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Function Tables (Continued)

LATCH SELECTION			
SELECT INPUTS			LATCH ADDRESSED
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

logic symbol†

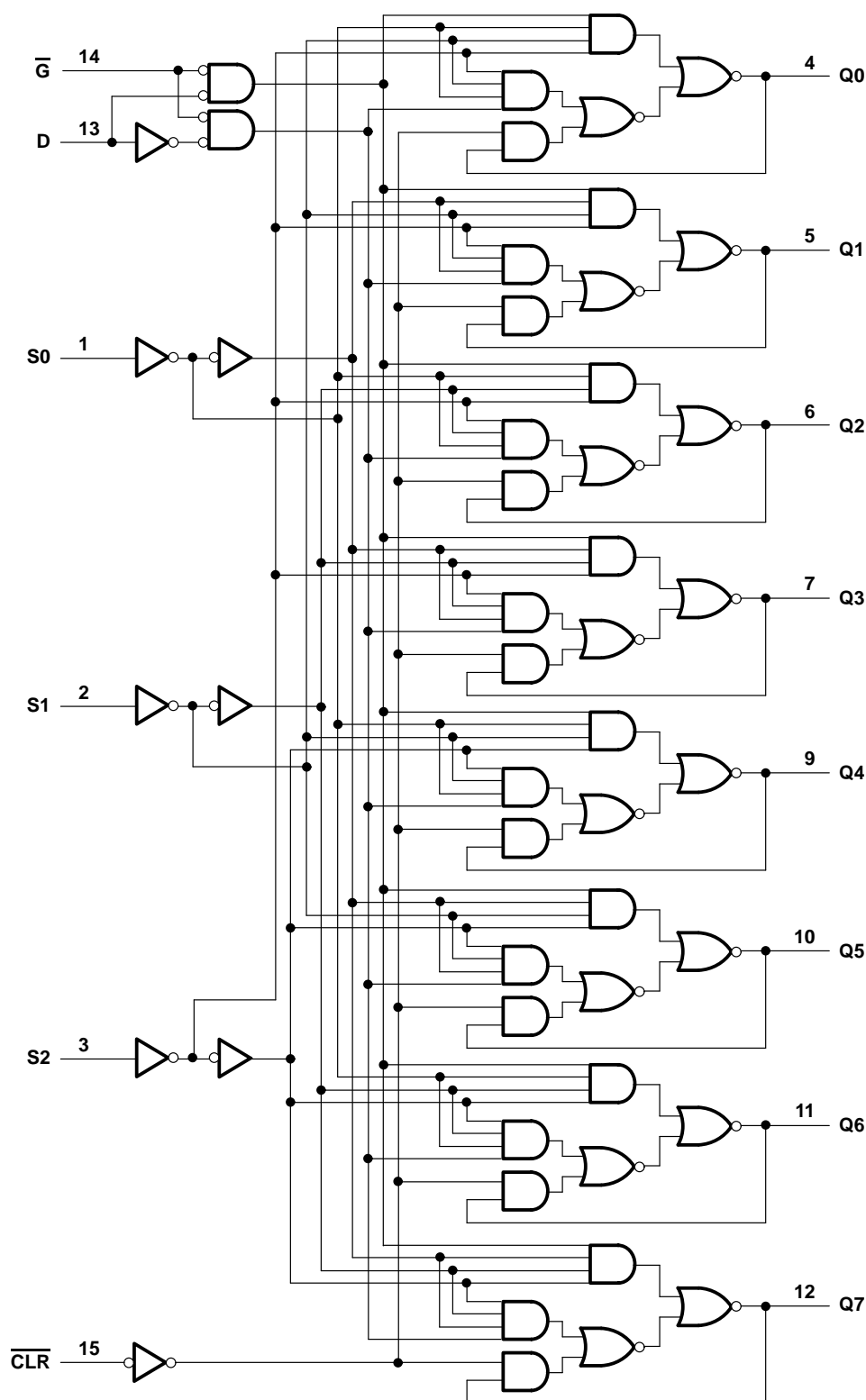


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

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logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Operating free-air temperature range, T_A : SN54ALS259	–55°C to 125°C
SN74ALS259	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54ALS259			SN74ALS259			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage		0.7			0.8			V
I _{OH}	High-level output current		−0.4			−0.4			mA
I _{OL}	Low-level output current		4			8			mA
t _w	Pulse duration	\overline{G} low	20			15			ns
		\overline{CLR} low	10			10			
t _{su}	Setup time	Data before $\overline{G}\uparrow$	20			15			ns
		Address before $\overline{G}\uparrow$	20			15			
t _h	Hold time	Data after $\overline{G}\uparrow$	0			0			ns
		Address after $\overline{G}\uparrow$	0			0			
T _A	Operating free-air temperature		−55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS259			SN74ALS259			UNIT
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IK}	$V_{CC} = 4.5$ V,	$I_I = -18$ mA			–1.5			–1.5	V
V_{OH}	$V_{CC} = 4.5$ V to 5.5 V,	$I_{OH} = -0.4$ mA	$V_{CC} - 2$			$V_{CC} - 2$			V
V_{OL}	$V_{CC} = 4.5$ V	$I_{OL} = 4$ mA		0.25	0.4		0.25	0.4	V
		$I_{OL} = 8$ mA					0.35	0.5	
I_I	$V_{CC} = 5.5$ V,	$V_I = 7$ V			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			20			20	μA
I_{IL}	$V_{CC} = 5.5$ V,	$V_I = 0.4$ V			–0.1			–0.1	mA
$I_{O\text{§}}$	$V_{CC} = 5.5$ V,	$V_O = 2.25$ V	–20		–112	–30		–112	mA
I_{CC}	$V_{CC} = 5.5$ V			14	22		14	22	mA

[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .



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switching characteristics (see Figure 1)

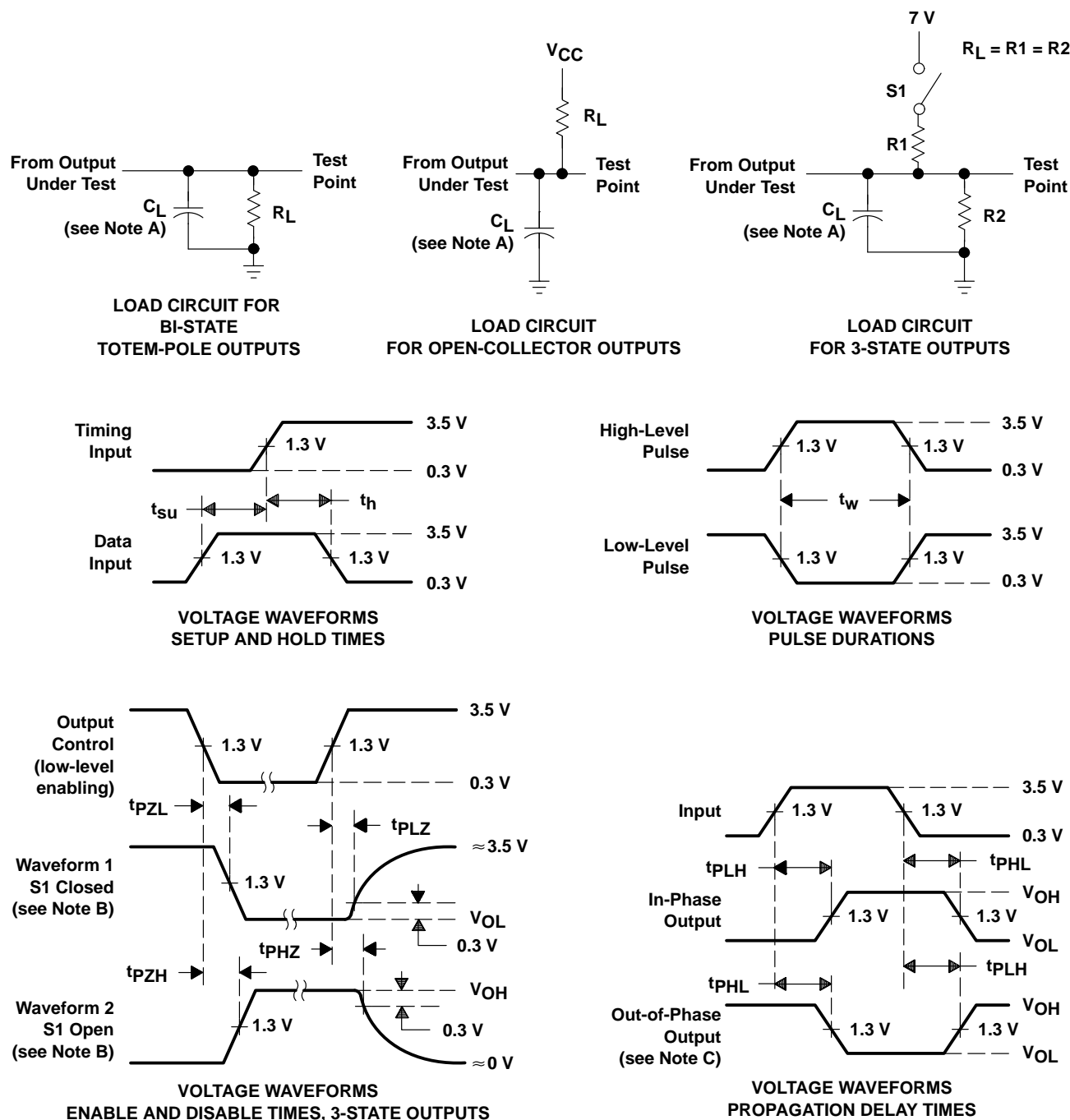
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX†				UNIT
			SN54ALS259		SN74ALS259		
			MIN	MAX	MIN	MAX	
t _{PHL}	CLR	Any Q	2	15	2	12	ns
t _{PLH}	Data	Any Q	4	22	4	19	ns
t _{PHL}			2	15	2	12	
t _{PLH}	Address	Any Q	4	26	4	22	ns
t _{PHL}			2	15	2	12	
t _{PLH}	Execute	Any Q	4	22	4	20	ns
t _{PHI}			2	16	2	13	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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