

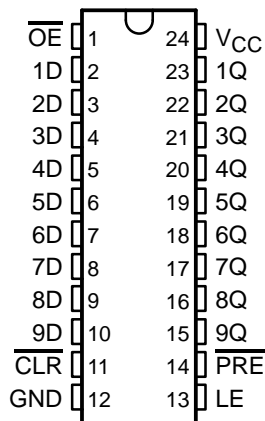
SN74ALS843

9-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SDAS232A – DECEMBER 1983 – REVISED JANUARY 1995

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Provides Extra Bus-Driving Latches Necessary for Wider Address/Data Paths or Buses With Parity
- Buffered Control Inputs to Reduce dc Loading Effects
- Power-Up High-Impedance State
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs

DW OR NT PACKAGE
(TOP VIEW)



description

This 9-bit bus-interface D-type latch features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The nine latches are transparent D-type latches with noninverting data (D) inputs.

A buffered output-enable (\overline{OE}) input places the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

\overline{OE} does not affect the internal operation of the latches. Previously stored data can be retained or new data can be entered while the outputs are off.

The SN74ALS843 is characterized for operation from 0°C to 70°C.

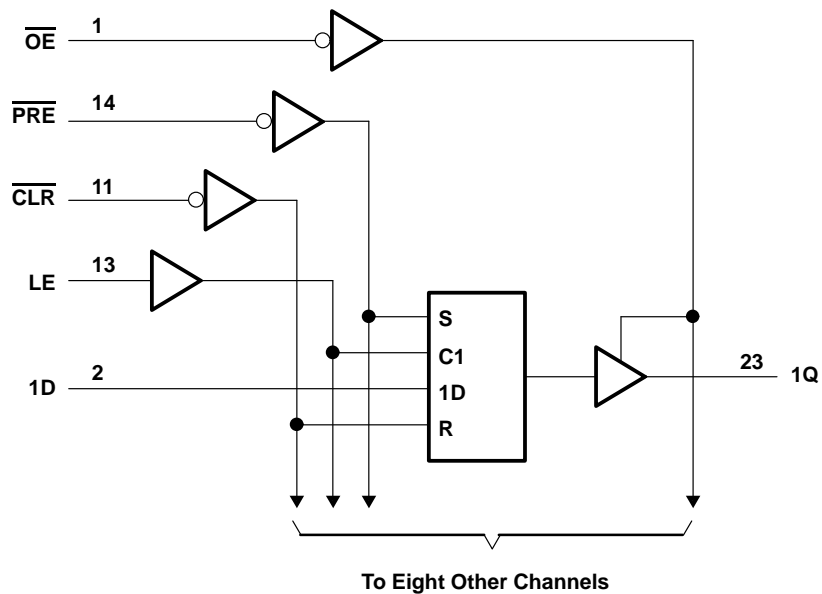
FUNCTION TABLE

INPUTS					OUTPUT Q
\overline{PRE}	\overline{CLR}	\overline{OE}	LE	D	
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q_0
X	X	H	X	X	Z

SDAS232A – DECEMBER 1983 – REVISED JANUARY 1995

Pin diagram of the 74VHC163 3-bit binary counter. The diagram shows a 16-pin package with pins 1 through 16. Pins 1, 14, 11, and 13 are control inputs: OE (pin 1), PRE (pin 14), CLR (pin 11), and LE (pin 13). Pins 2 and 10 are inputs to the EN (pin 2) and C1 (pin 10) inputs. Pins 3 through 10 are data inputs: 1D (pin 3), 2D (pin 4), 3D (pin 5), 4D (pin 6), 5D (pin 7), 6D (pin 8), 7D (pin 9), and 8D (pin 10). Pins 15 and 16 are outputs: 1Q (pin 15) and 2Q (pin 16). Pins 17 through 23 are data outputs: 3Q (pin 17), 4Q (pin 18), 5Q (pin 19), 6Q (pin 20), 7Q (pin 21), 8Q (pin 22), and 9Q (pin 23). The diagram also shows the internal logic of the counter, including the EN, S2, R, and C1 inputs, and the 1D and 2D inputs.

logic diagram (positive logic)



SN74ALS843
9-BIT BUS-INTERFACE D-TYPE LATCH
WITH 3-STATE OUTPUTS

SDAS232A – DECEMBER 1983 – REVISED JANUARY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–2.6	mA
I_{OL}	Low-level output current			24	mA
t_w	Pulse duration	\overline{CLR} or \overline{PRE} low		35	ns
		LE high		20	
t_{su}	Setup time, data before LE↓	10			ns
t_h	Hold time, data after LE↓	5			ns
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA			–1.2	V
V_{OH}	$V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -0.4$ mA	$V_{CC} - 2$			V
	$V_{CC} = 4.5$ V, $I_{OH} = -2.6$ mA	2.4	3.2		
V_{OL}	$V_{CC} = 4.5$ V	$I_{OL} = 12$ mA		0.25	V
		$I_{OL} = 24$ mA		0.35	
I_{OZH}	$V_{CC} = 5.5$ V, $V_O = 2.7$ V			20	μA
I_{OZL}	$V_{CC} = 5.5$ V, $V_O = 0.4$ V			–20	μA
I_I	$V_{CC} = 5.5$ V, $V_I = 7$ V			0.1	mA
I_{IH}	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20	μA
I_{IL}	$V_{CC} = 5.5$ V, $V_I = 0.4$ V			–0.1	mA
$I_{O\$}$	$V_{CC} = 5.5$ V, $V_O = 2.25$ V	–30		–112	mA
I_{CC}	$V_{CC} = 5.5$ V	Outputs high		21	mA
		Outputs low		41	
		Outputs disabled		25	

‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN74ALS843

9-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

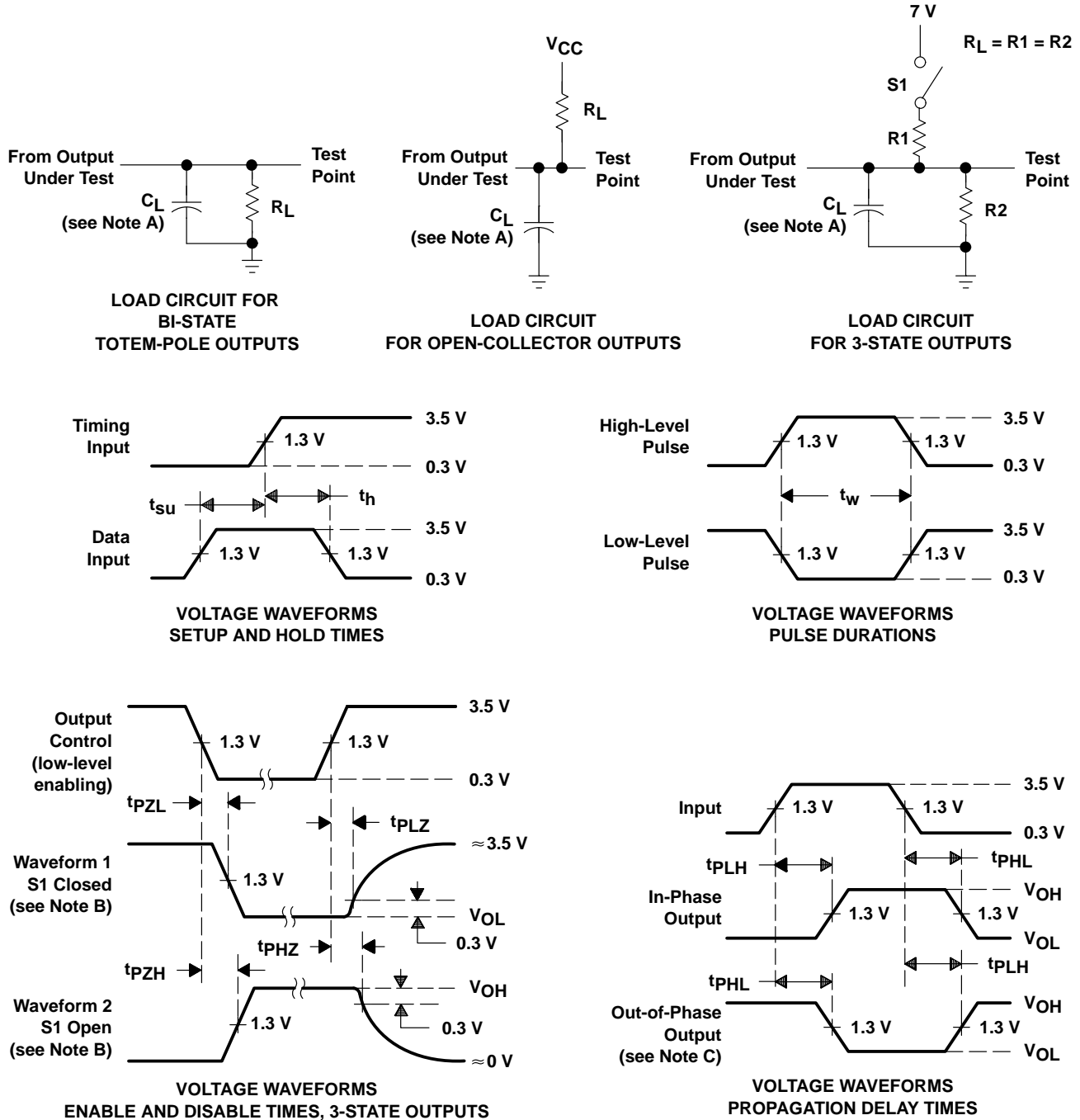
SDAS232A – DECEMBER 1983 – REVISED JANUARY 1995

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX†		UNIT
			MIN	MAX	
t _{PLH}	D	Q	2	13	ns
t _{PHL}			4	18	
t _{PLH}	LE	Q	5	21	ns
t _{PHL}			8	26	
t _{PLH}	$\overline{\text{PRE}}$	Q	5	22	ns
t _{PHL}	$\overline{\text{CLR}}$		6	23	
t _{PZH}	$\overline{\text{OE}}$	Q	2	12	ns
t _{PZL}			4	14	
t _{PHZ}	$\overline{\text{OE}}$	Q	2	10	ns
t _{PLZ}			2	12	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.