

SN54F175, SN74F175 QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

SDFS058A – D2932, MARCH 1987 – REVISED OCTOBER 1993

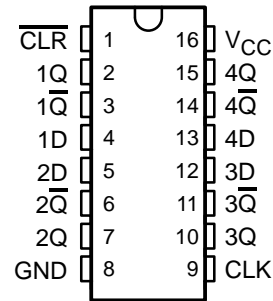
- Contain Four Flip-Flops With Double-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Applications Include:
Buffer/Storage Registers
Shift Registers
Pattern Generators
- Package Options Include Plastic
Small-Outline Packages, Ceramic Chip
Carriers, and Standard Plastic and Ceramic
300-mil DIPs

description

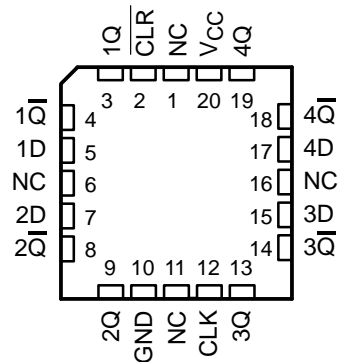
These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear ($\overline{\text{CLR}}$) input. Information at the data (D) inputs meeting setup time requirements is transferred to outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

The SN54F175 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74F175 is characterized for operation from 0°C to 70°C .

SN54F175 . . . J PACKAGE
SN74F175 . . . D OR N PACKAGE
(TOP VIEW)



SN54F175 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

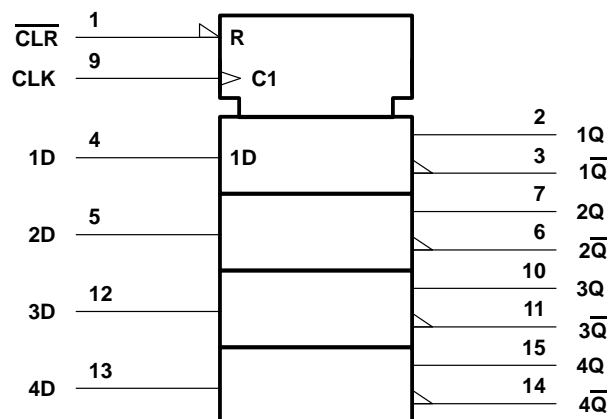
FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	X	X	L	H
H	\uparrow	H	H	L
H	\uparrow	L	L	H
H	L	X	Q_0	$\overline{\text{Q}}_0$

SN54F175, SN74F175 QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

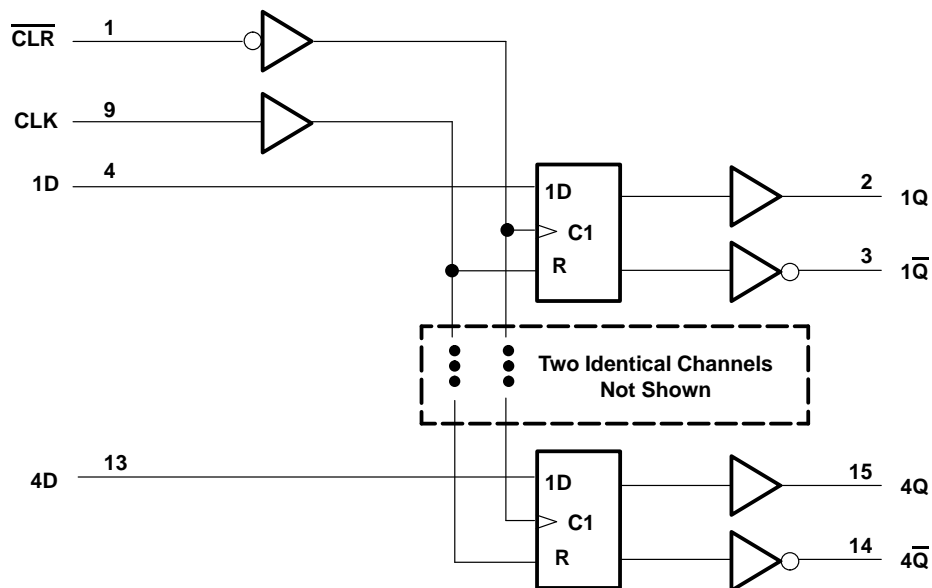
SDFS058A – D2932, MARCH 1987 – REVISED OCTOBER 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

SN54F175, SN74F175 QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

SDFS058A – D2932, MARCH 1987 – REVISED OCTOBER 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–1.2 V to 7 V
Input current range	–30 mA to 5 mA
Voltage range applied to any output in the high state	–0.5 V to V_{CC}
Current into any output in the low state	40 mA
Operating free-air temperature range: SN54F175	–55°C to 125°C
SN74F175	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F175			SN74F175			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			–18			–18	mA
I_{OH}	High-level output current			–1			–1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54F175			SN74F175			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA			–1.2			–1.2	V
V_{OH}	$V_{CC} = 4.5$ V, $I_{OH} = -1$ mA	2.5	3.4		2.5	3.4		V
	$V_{CC} = 4.75$ V, $I_{OH} = -1$ mA				2.7			
V_{OL}	$V_{CC} = 4.5$ V, $I_{OL} = 20$ mA	0.3	0.5		0.3	0.5		V
I_I	$V_{CC} = 5.5$ V, $V_I = 7$ V		0.1			0.1		mA
I_{IH}	$V_{CC} = 5.5$ V, $V_I = 2.7$ V		20			20		μA
I_{IL}	$V_{CC} = 5.5$ V, $V_I = 0.5$ V		–0.6			–0.6		mA
I_{OS}^{\S}	$V_{CC} = 5.5$ V, $V_O = 0$	–60		–150	–60		–150	mA
I_{CC}	$V_{CC} = 5.5$ V, See Note 2	22.5		34	22.5		34	mA

‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: I_{CC} is measured with outputs open with 4.5 V applied to all data inputs after a momentary ground followed by 4.5 V applied to CLK.



SN54F175, SN74F175

QUADRUPLE D-TYPE FLIP-FLOPS

WITH CLEAR

SDFS058A – D2932, MARCH 1987 – REVISED OCTOBER 1993

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} = 5 V, T _A = 25°C		SN54F175		SN74F175		UNIT
			'F175						
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		0	100	0	100	0	100	MHz
t _w	Pulse duration		CLK high	4	4	4	ns		
			CLK low	5	5	5			
			CLR low	5	5	5			
t _{su}	Setup time, data before CLK↑	High or low	3	3	3	ns			
	Setup time, inactive state, data before CLK↑†	CLR high	5	5	5				
t _h	Hold time, data after CLK↑		High or low	1	1	1	ns		

[†] Inactive-state setup time is also referred to as recovery time.

switching characteristics (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R _L = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX‡				UNIT
			'F175			SN54F175		SN74F175		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			100	140		100		100		MHz
t _{PLH}	CLK	Q or \overline{Q}	3.2	4.6	6.5	2.7	8.5	3.2	7.5	ns
t _{PHL}			3.2	6.1	8.5	3.2	10.5	3.2	9.5	
t _{PLH}	$\overline{\text{CLR}}$	\overline{Q}	3.2	6.1	8.5	3.2	10	3.2	9	ns
t _{PHL}		Q	3.7	8.6	11.5	3.7	15	3.7	13	

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.